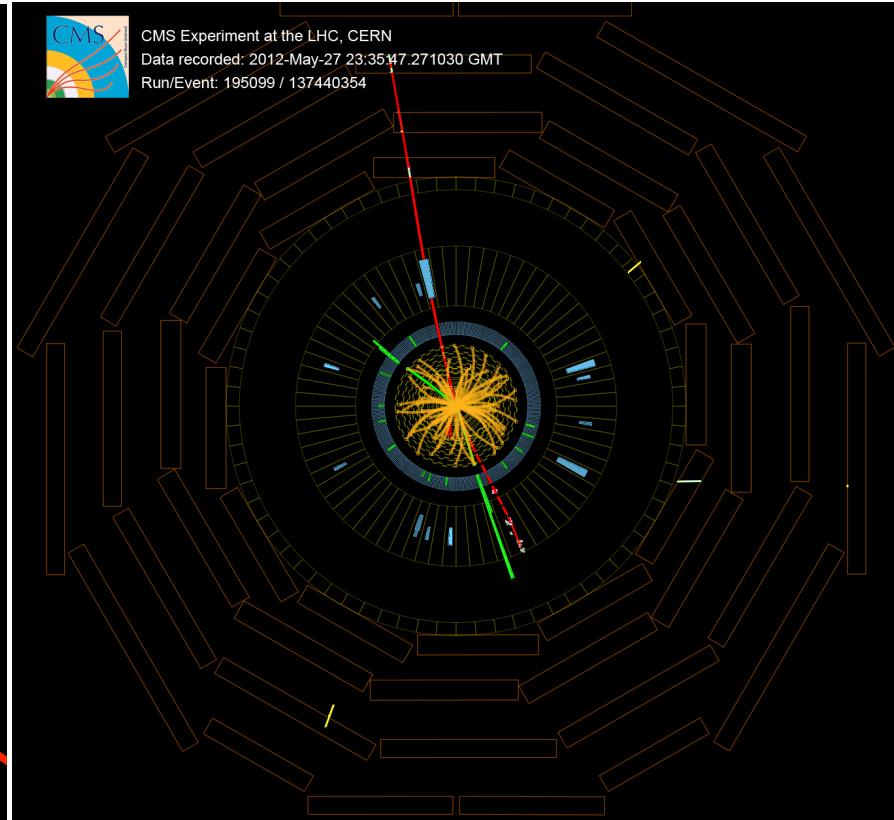
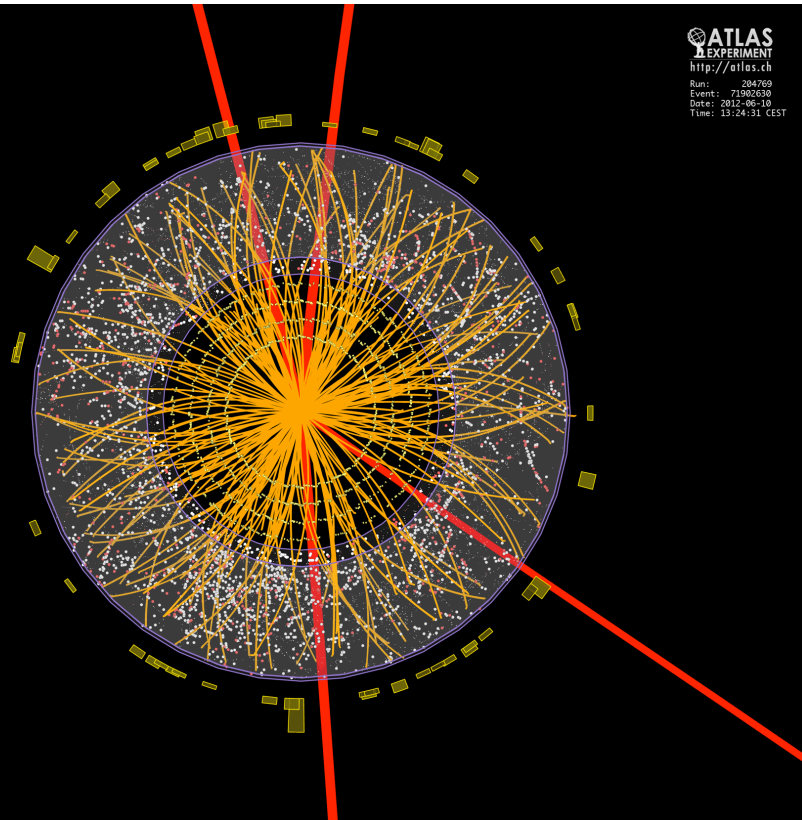


# ACES2014

## Common ATLAS-CMS Electronics Workshop for LHC Upgrades

### Wrap-Up Session Introduction



# Some General Comments

- ▶ There were about 150 registrations but we have not seen everybody at the same time in the room
  - ▶ Significant changes in attendance (who is attending what) with the sessions
  - ▶ Might limit the goal of having large exchange between people...
- ▶ ACES has been (is still being) webcasted
  - ▶ Statistics for days 1 and 2 (total connections/simultaneous connections):
    - ▶ 71/30 and 57/42
  - ▶ A good fraction from inside CERN
- ▶ We got a complete overview of the on-going developments
  - ▶ We also saw from the ATLAS and CMS overall plans that the upgrade program is very ambitious

# Points of Concerns

## *As Identified by the Organising Committee*

- ▶ High speed low power links
- ▶ IC technos availability and 65 nm plans
- ▶ Radiation qualification
- ▶ TTC
- ▶ Schedule
- ▶ Concurrent developments
- ▶ Power
- ▶ Level-1 rates and Latency
- ▶ Tracking trigger

# High Speed – Low Power Links (1)

- ▶ Current GBT version
  - ▶ Development reaching an end
  - ▶ Production schedule still to be finalised
    - ▶ MPW or direct ER (see Paulo's slides)
    - ▶ Impact on CMS HCAL HE upgrades to be clarified
  - ▶ VTXx ready for production
- ▶ Both ATLAS and CMS require a new version
  - ▶ Low Power and High Speed version
  - ▶ Plan for a single development is attracting
  - ▶ Specifications to be defined and frozen this year
    - ▶ With the two experiments
  - ▶ CERN to secure resources

# High Speed – Low Power Links (2)

- ▶ Versatile link current version
  - ▶ Ready for production
- ▶ New low profile up to 4 channels proposal
  - ▶ See François' slides
  - ▶ Could be available within 3 years
    - ▶ Meaning usable for phase-1
- ▶ Other developments on-going
  - ▶ Amount of R&D and qualification work not to be underestimated
    - ▶ ATLAS had “experiences” in the past

# IC Technologies and 65 nm

- ▶ Cannot do so much with respect to techno availability
  - ▶ Keep our eyes opened
  - ▶ Try to have back-up solutions if possible
    - ▶ Knowing that a change of techno is not for free in terms of work
  
- ▶ 65 nm
  - ▶ Developments starting and frame contract almost in place
  - ▶ Radiation hardness should not be taken as granted
    - ▶ Still some qualification work and studies to understand and overcome weakness to be done

# Radiation Qualification

- ▶ Although not so much addressed during the workshop we now have a much better understanding of the radiation levels in the detector
  - ▶ Meaning safety factors can be reduced
- ▶ Could we define a common testing/qualification procedure?
- ▶ Dealing with SEE at different stages (ASIC, FPGA, systems) addressed differently in sub-detectors
  - ▶ Would benefit from sharing experience

- ▶ Question during ACES: why is ATLAS not upgrading its TTC system now as is CMS doing?
  - ▶ TTC techno unchanged
  - ▶ CMS needed more partitions and flexibility
  - ▶ ATLAS is introducing during LS1 additional “global partitions”
- ▶ **TTC-PON project made some progress**
  - ▶ Project to go on but experiments encouraged to study the proposal and communicate their needs/requirements



- ▶ Still a bit fuzzy as usual
- ▶ Not clear whether the production schedules for phase 2 are similar for ATLAS and CMS
  - ▶ It would be good to have a look at that as this has implications on the schedule of common devices

# Concurrent Developments

- ▶ We always complain about lack of resources but still we have concurrent developments of very similar devices
- ▶ A few examples:
  - ▶ 3 ADC 12-bit 40 MHz developments in ATLAS
  - ▶ Several xxx7 boards in CMS
  - ▶ Variant of optical links
- ▶ Always a delicate subject as we have to find a working space for everyone but it might be really good to coordinate (including with industry participation) in view of getting better devices
  - ▶ Such as a 14-16 bit ADC with 11-12 ENOB to avoid multigain systems
  - ▶ One or 2 FPGA platforms with a good framework for the firmware development

# Non-concurrent Developments

- ▶ Several time we heard about using devices developed by others for other purposes
  - ▶ Meaning it's feasible
  - ▶ Examples: MP7 in CMS, calorimeter back-end electronics for muon
- ▶ RD53 is a good example of possible successful collaboration

- ▶ Rad-hard and magnetic tolerant POL
  - ▶ Development for phase-1 reaching an end
  - ▶ Delivery of complete DC-DC modules or of components and expertise for adhoc integration
  - ▶ Need improvement on radiation hardness for phase 2 trackers
    - ▶ Very likely adhoc integration needed
- ▶ Commercial POLs
  - ▶ We see a number of tests going on with commercial devices
  - ▶ An inventory of the target needs and of the results would be useful
- ▶ Not yet addressed but the power schemes require also “bulk” DC-DC delivering 12, 24 or 48 V
  - ▶ Collaboration with industry necessary
  - ▶ It took a lot of time for the current detectors so we should start looking at it with 2 – 3 years (?)
  - ▶ Need to have finalised power schemes

# L0/L1 , L1 rates and latencies

- ▶ It appeared clearly that these numbers are still not final
  - ▶ Huge impact on the readout designs
- ▶ Discrepancies between ATLAS and CMS
  - ▶ Wesley discussed them
  - ▶ 20 years ago when we were defining the experiments readout systems we had identical numbers
- ▶ **What are the maximum reachable latencies?**
  - ▶ We squeeze ourselves in difficult corners because of legacy FE electronics we hope (dream) will be running smoothly until 2035 – 2040
  - ▶ Limit for tracker front-ends because of power consumption

# Tracking Triggers

- ▶ Two different philosophies in trigger scheme and how to integrate tracking
- ▶ ATLAS put a bit of confusion in mentioning wish or need for at least some self-seeded trigger
  - ▶ The detector layout is not adapted to this
  - ▶ The impact on FE electronics is huge
- ▶ Off-detector track finding
  - ▶ The proposed schemes need to be demonstrated with a small scale system
    - ▶ Note that ATLAS FTK is certainly a good demonstrator for the associative memory scheme
  - ▶ Would be good to understand how the available latency impact the complexity and cost of this system

# Time for discussion...

- ▶ ... or potatoes to fly
  
- ▶ Before you start we would like to thank you again for your participation