Phase 1 CMS Muon Trigger Upgrade

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Overview

- Expect substantial increase in LHC performance after LS1:
  - Pile-up of ~ 50 regardless of BX spacing (25 or 50 ns)
  - Inst. luminosity up to $2 \times 10^{34}$ cm$^{-2}$s$^{-1}$
  - Exceed the design performance (number of pile-up exceeded during 2012)

- L1 trigger output rate limited to 100 kHz by readout bandwidth

- Without upgrade, likely to exceed L1 bandwidth

- Design outlined in Level-1 Trigger Upgrade TDR (August 2013)

- Electronics Design Review in Nov 2013, received very useful feedback
Muon Trigger Upgrade Goals, Strategy

- Improve hardware and algorithms to reduce the rate without significantly affecting the efficiency
- Move the redundancy of the three muon detection systems earlier into the trigger processing chain
- Upgrade in parallel to operating current trigger system
Phase 1 Muon Trigger Upgrade Schematic

Diagram showing the flow of information through various components of the muon trigger system, including Splitters, CSC, DT, RPC, Mezz, New SC & fan-out, OFCu, CSCTF, DTTF, PAC, RPC Sorters, CSC Sorter, DT Sorters, Global Muon Trigger, Global Trigger, and µTF Layer.
Trigger Regions

Barrel

Overlap

Endcap

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DT Trigger Primitives

- No schedule interference for achieving validation tests
- Backward compatible with old SC links

Schedule:
2015 – validation on a slice: 6 sectors bottom part of YB-2 and YB-1
2016 – full deployment
DT Parallel Commissioning Scheme

Diagram showing the DT Parallel Commissioning Scheme with nodes labeled as DT Mini Crate, DT Cu OF, DT Collector, sector Collector, DT OF Cu, TwinMux, DTTF, Barrel MTF, and Overlap MTF. Connections are made through MPO-MPO splitters, 12-fiber MPO cables, and LC-MPO fan-outs.
**RPC Trigger Primitives**

- **Barrel MTF**
  - 300 links from barrel
  - 144 from current endcaps
  - 48 for new Station-4 RPC chambers

- **Overlap MTF**
  - Total: $492 \times 1.6$ Gb/s optical links

- **Endcap MTF**
  - Does not include planned high-eta upgrades
  - Before any splitting for upgrades

Each oval is one GOL link @1.6 Gb/s

- It transmits data from:
  - Barrel: 2 or 3 RPC rolls (eta partitions)
  - Endcap: 3 chambers
### RPC Parallel Commissioning

- Use legacy RPC splitter boards to split signals.
- One copy sent to legacy RPC system.
- Other copy sent to upgraded trigger being commissioned.
CSC Trigger Primitives

- MPC card:
  - in peripheral crate on detector
  - concentrates data from 6 chambers

- New mezzanine card with Spartan-6 FPGA and additional optical link

- Sends separate copy of primitives to upgrade system, legacy path stays same

- Plan to install all MPC mezzanine upgrades by the end of LS1

- First production mezzanines are at CERN, working on getting them installed at Pt 5
Barrel Region Trigger Overview

- Use same track finding algorithm as employed in Run I
- 12×30° sectors, data sharing to both neighboring sectors
- port of track finding firmware well under way
- I/O tests so far successful
- $p_T$ resolution improvements:
  - from improved trigger primitives
  - use of more information in algorithm
Barrel Region $p_T$ Assignment

- $p_T$ measured from muon segment direction at innermost station
- additional handles are available
  - deflection angle between two stations
  - RPC hits to correct position, timing

Tail reduction by $\times 2-3!$
Platform: MP7 Processor Card

- Multi-purpose μTCA processor card
- Originally designed within calorimeter trigger effort
- 1.8Tb/s optical signal processor:
  - 72Tx+72Rx links at 12.5Gbps
  - Xilinx Virtex-7 FPGA: XC7VX485T or XC7VX690T
  - On-board firmware repository
  - 2×144Mbit 550MHz QDR RAM
- Full detail tomorrow: talk by Andrew Rose
- Region currently richest with muon hit information: DT, RPC, CSC all contribute
- Most potential for improvement from combining information from multiple detectors
- Difficulties: combining different detector geometries, varying B field – need flexible approach / algorithm
Overlap Region Algorithm

For simplicity only RPC PDFs are shown

\[
LLH(\text{ref strip}) = 2 \cdot \log(\text{PDF}_{\text{RPC}}^{\text{MB3}}) + 2 \cdot \log(\text{PDF}_{\text{DT}_{\text{pos}}}^{\text{MB3}}) + 2 \cdot \log(\text{PDF}_{\text{DT}_{\text{dir}}}^{\text{MB3}}) + 2 \cdot \log(\text{PDF}_{\text{DT}_{\text{pos}}}^{\text{MB2}}) + 2 \cdot \log(\text{PDF}_{\text{DT}_{\text{dir}}}^{\text{MB2}}) + 2 \cdot \log(\text{PDF}_{\text{RPC}_{\text{in}}}^{\text{MB2}}) + 2 \cdot \log(10^{-6}) \text{ (outside PDF}_{\text{RPC}_{\text{out}}}^{\text{MB2}}) + 2 \cdot \log(\text{PDF}_{\text{DT}_{\text{pos}}}^{\text{MB1}}) + 2 \cdot \log(\text{PDF}_{\text{DT}_{\text{dir}}}^{\text{MB1}}) + 0 \text{ (missing hit ignored)}
\]
- Low-$p_T$ tails decimated, $\times 2$ lower rate for same plateau efficiency

- Working on optimizing pattern information to fit in FPGA comfortably
CSC covers across entire $|\eta|$ region, partial RPC coverage

New muon detectors will be added during LS2: GEM, RPCG ..
[full details in Gilles De Lentdecker’s talk, later in this session]

Most variation in B field, very diverse geometries

Need platform and solution that can be expanded to transparently include new primitives as they become available
- Run 1: likelihood fit to 2 $\phi$-deflection angles to determine $p_T$
- Fit results $\rightarrow$ LUT [non-linear sampling of phase space]
- Investigated remaining rate reduction power in data using BDT's
- Factor 2 rate reduction found with little eff. loss
- Strategy similar to Run1, use BDT to determine $p_T$ offline – many variables available [large LUT]
Performance of LUT approach ultimately limited by LUT memory size

Muon Track Finder with Virtex-7 (MTF7):
- Maximize data input for merging information from many sources
- Provide large random access LUT
- Modular design - features can be further optimized as needed
MTF7 Processor, at a glance

- Optimized for maximum input from muon detectors

- Optical board tested with Virtex-6 prototype:
  - 84 10-Gbps input links [tested @ 1.6-10 Gbps]
  - 24 10-Gbps output links [tested @ 10 Gbps]

- 1 GB of RLDRAM for LUT [tested, ok]

- Virtex-7 base board prototype tested, all 84 transmitters and 24 receivers working at 10 Gbps:
  - IPBus, PCIExpress communication demonstrated with Virtex-6 prototype

- Double-wide µTCA card [backplane connector, tested at 10 Gbps]

- CERN test-stand prototype undergoing final tests, will arrive at CERN within a few days
MTF7 Base Board

Custom backplane connector

Core logic FPGA

Control FPGA

μTCA connector

1Gb FLASH Main FPGA firmware storage

FPGA JTAG Core & Ctrl

PT LUT module connector

MMC JTAG

MMC CPU

SD card connector

MMC USB console
MTF7 Optical Board and Backplane

Harting connector  
Same as used in μTCA backplanes

Custom backplane connector

Backplane redrivers

μTCA connector

MMC

Optical transmitters (2 out of 3 installed)

Optical receivers (2 out of 7 installed)

Samtec connector  
for SP12 Virtex-6 board  
Two Hartings for Virtex-7

Ivan Furić, March 19th 2013

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MTF7 $p_T$ LUT Memory Mezzanine

- Base board connector
- Clock synthesis and distribution
- Glue logic FPGA (Spartan-6)
- RLDRAM3 memory
  - 16 chips, 8 on each side (clamshell topology)
  - Total size: 1 G x 9 bits
  - Upgrade possible to 2 G x 9 bits (no board redesign)

DC-DC converters

Ivan Furić, March 19th 2013
ACES 2014 Workshop, CERN
Upgraded Global Muon Trigger

- **Tasks of the µGMT**
  - Sorting, including the regional sorting layer into the µGMT (optimizes latency)
  - Ghost busting between track-finder $|\eta|$ regions and wedge/sector boundaries
  - Muon isolation (depending on performance of upgraded TFs)

- **Platform: MP7 µTCA Processor**
  - First iteration of algorithm logic implemented
    - ~20% resources sorting + ghostbusting
    - est. additional ~18% resources for I/O, IPBus

- Well on schedule!
Concluding Remarks

- Phase 1 Muon Trigger Upgrade starting to germinate:
  - Promising $p_T$ assignment algorithms identified, currently being tuned
  - Hardware tests commencing

- Trigger division into $|\eta|$ regions allows tuning for region-specific challenges

- Side benefits to $|\eta|$ region division:
  - hardware designs back each other
  - we are learning from each other’s algorithms

- No obvious road blocks identified, but bulk of grunt work is still ahead of us

- Schedule drives us to start commissioning in Jan 2015, switch to new trigger in Jan 2016! [EDR: tight but doable]
Muon Trigger Optical Plant

- DT Mini Crate
- DT Cu OF
- 12-fiber cables
- DT TwinMux
- Fan-outs
- 12-fiber cables
- LC-MPO Fan-outs
- Barrel MTF
- RPC LB
- trunk cables
- RPC Splitter Boards
- LC-MPO Fan-outs
- Overlap MTF
- CSC MPC
- 8-fiber cables
- MPO-LC Fan-outs
- Optical Splitter
- LC-MPO Fan-outs
- Endcap MTF