The ATLAS New Small Wheel Trigger

Lorne Levinson
For the ATLAS NSW collaboration

ACES workshop, 19 March 2014

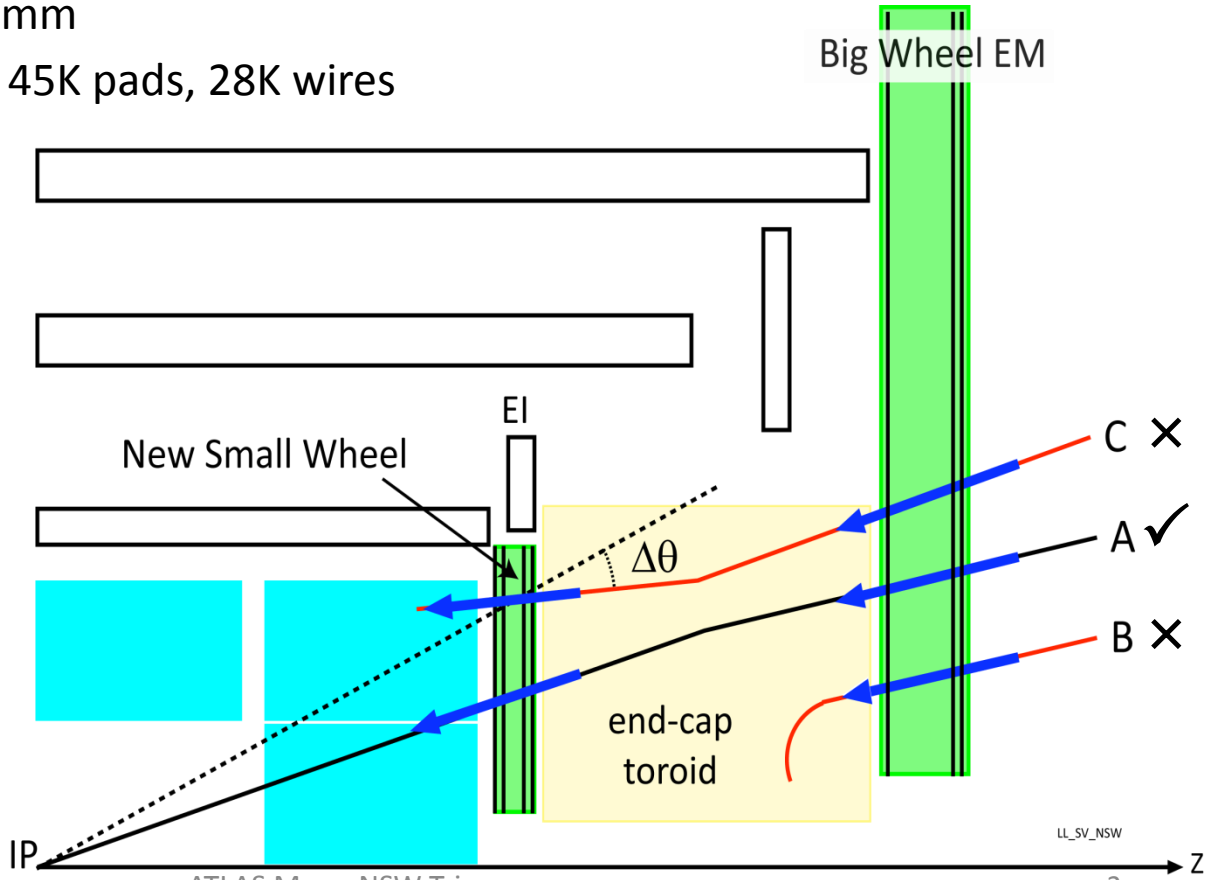
Thanks to my NSW colleagues for many slides

NSW trigger concept

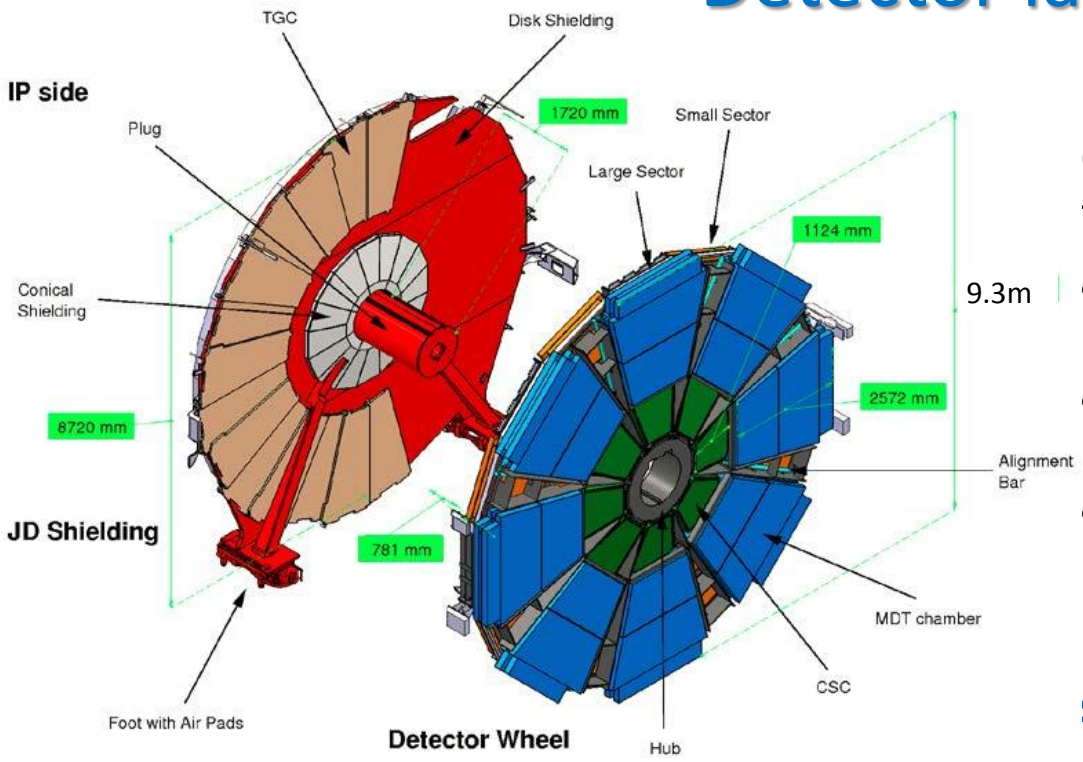
- Increased Phase I backgrounds, but must maintain existing trigger rate
- Filter “Big Wheel” muon candidates to remove tracks that are not from the IP
  Only track “A” should be a trigger candidate.
- Challenge is latency: 500nsec for electronics + 500ns fibres to be in time for Big Wheel
- Micromegas: 2M strips, 0.5mm
- sTGC: 280K strips (3.2mm), 45K pads, 28K wires
- sTGC, MM find candidates independently,
  list merged for Sector Logic
- Hit per layer:

  sTGC:
  hit is centroid of 3-5 strips

  Micromegas:
  hit is address of strip

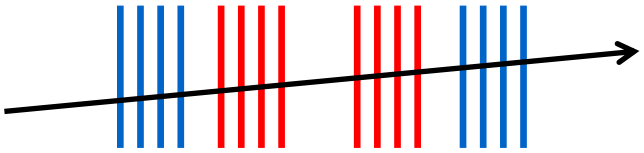


Detector layout



Present Small Wheel – defines basic layout and envelopes

- 16 detector layers in total
- 2 technologies, **MicroMegas** and **sTGC**



Micro-Mesh Gaseous detectors (Micromegas): primary precision tracker

- Space resolution < 100 µm independent of track incidence angle
- Good track separation due to small 0.5 mm readout granularity (strips)
- Excellent high rate capability due to small gas amplification region and small space charge effects

sTGCs: primary trigger detector

- Bunch ID with good timing resolution – additional suppression of fakes
- Good space resolution providing track vectors with < 1 mrad angular resolution
- Based on proven TGC technology; Pads & strips, instead of only strips as in current detector

Front end outputs for trigger path

sTGC strips: one output per channel

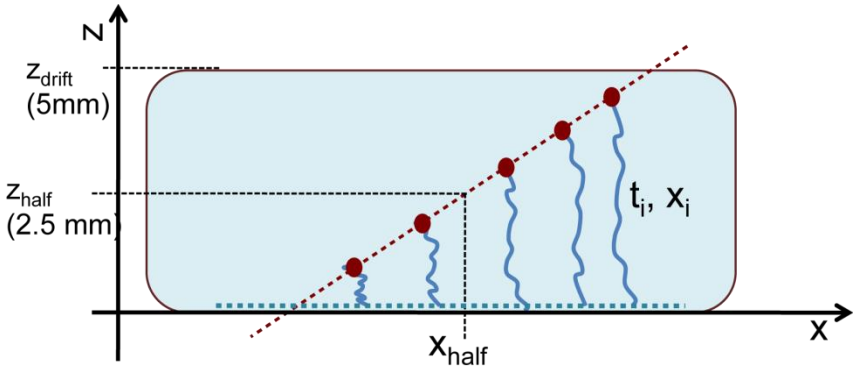
- 6-bit flash ADC of peak; serial output at 160Mb/s
- Centroid of 3 to 5 3.2mm strips gives track coordinate in a layer

sTGC pads: one output per channel

- 10nsec pulse at peak, or use leading edge of Time-over-Threshold
- Coincidence in 8-layer tower of pads chooses which strips to transfer to centroid finder

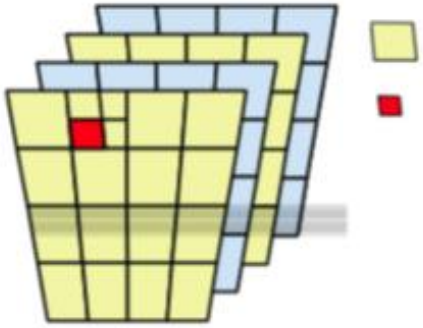
Micromegas: one output per 64-channel chip

- Address in Real Time (ART) of first (in time) strip hit in the BC per chip
- Address of 0.5mm strip gives track coordinate
- "μTPC" mode

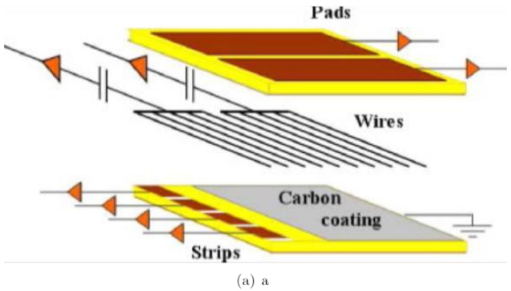


See preceding talk on the VMM Front-end ASIC by Gianluigi de Geronimo

sTGC trigger scheme



1/16th sector



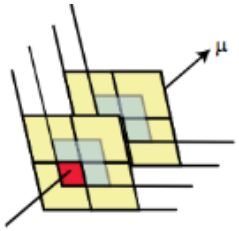
On Rim of NSW FPGAs

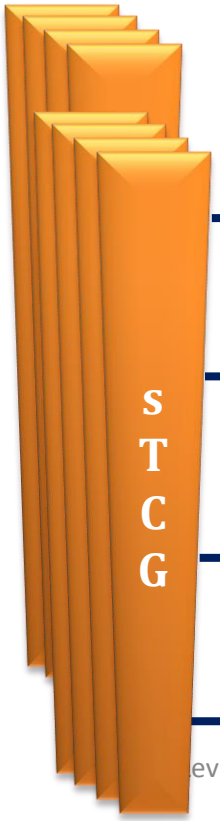
USA 15

Pad Trigger

Router

sTGC Trigger Processor





Pad VMM

Pad TDS

Strip VMM

Strip TDS

Strip VMM

Strip TDS

Only one Strip TDS chosen

On-chamber ASICS

Problem: no BW to read all strips

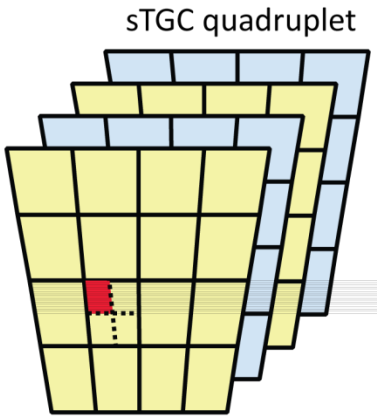
Pad trigger uses pad tower coincidence to choose ONLY the relevant band of strips.

Physical pads staggered by ½ pad in both directions

Logical pad-tower defined by projecting from 8 layer of staggered pad boundaries

Pad-tower coincidence =
2 × 3-out-4 overlapping pads

sTGC trigger: strip logic: one layer of one 1/16th



on chamber | on rim of small wheel

TTC and DCS via GBT

TTC & Config Distrib

sTGC

64 ASD 64 TDS 64 ASD 64 on-chamber

Pad trigger 3/4 & 3/4

Choose the band of strips under the tower

Selected band:
One 125-bit word per BC:
BCID, bandID, ϕ-ID, strip charges
⇒ 5.0 Gb/sec

router

opt lnk — Outer

opt lnk — Middle

opt lnk — Inner

in USA15

BC clock

8 layers — centroid finder and track extrapolator (Outer)

8 layers — centroid finder and track extrapolator (Middle)

8 layers — centroid finder and track extrapolator (Inner)

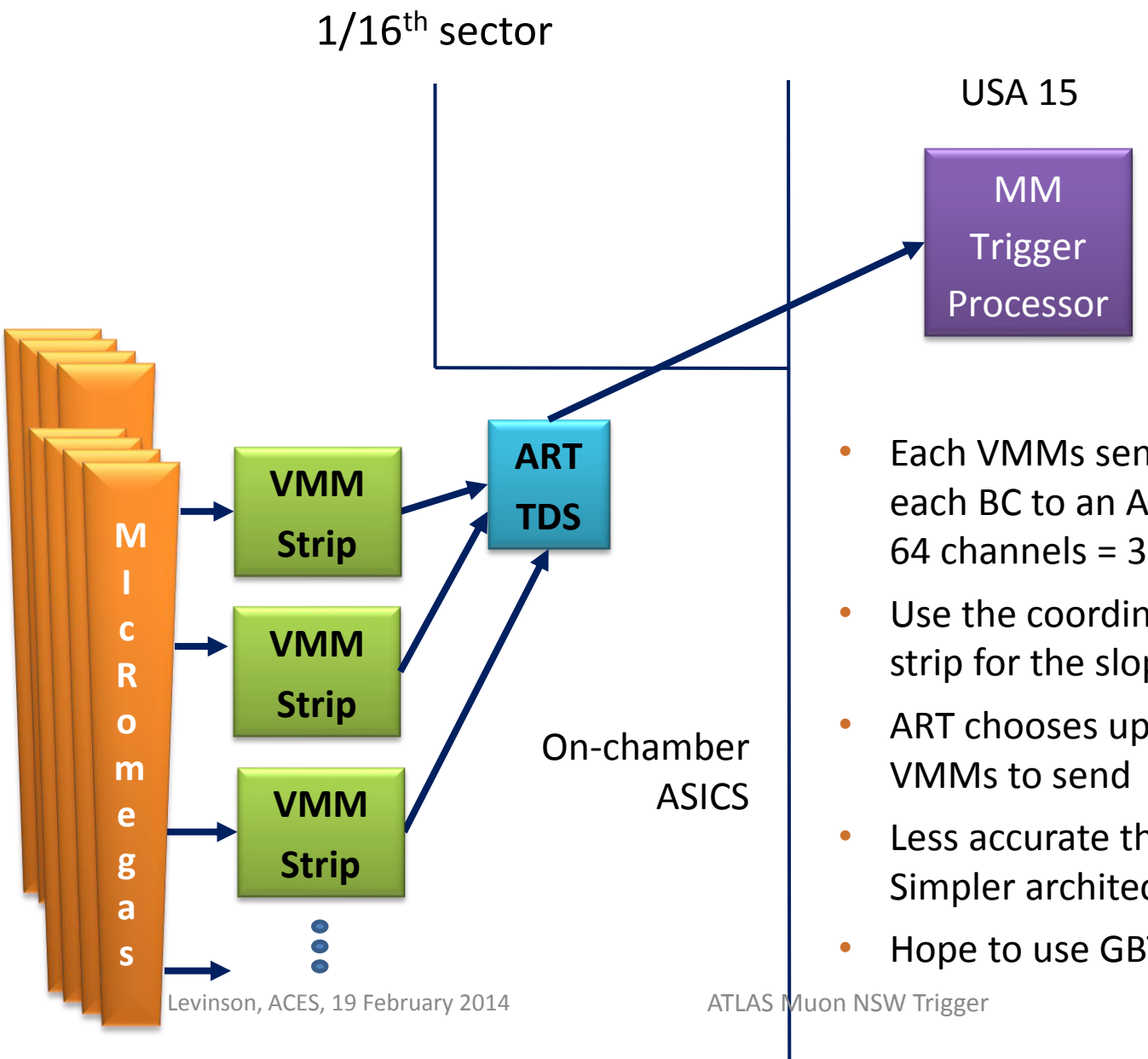
to sector logic
3 candidates per BC

in USA15

	strips	ASDs	TDS's	routers	links	centroid finders
Total:	~1030	18	9	1	3	3 (for 8 layers)

LL_sTGC_trigger_overview_V08

Micromegas trigger scheme

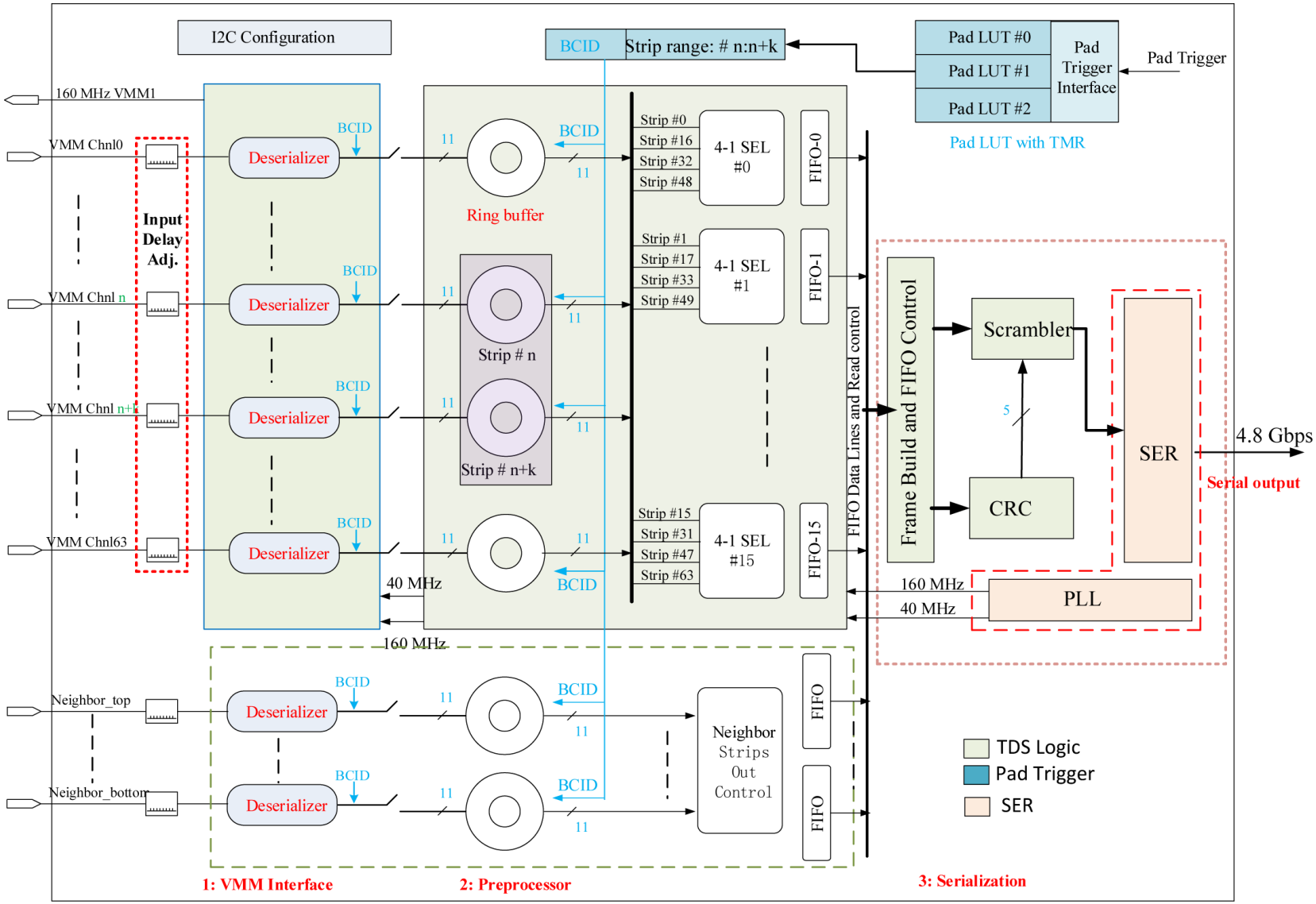


- Each VMMs send address of its first hit in each BC to an ART ASIC.
  64 channels = 3.2cm
- Use the coordinate of the center of the strip for the slope calculation
- ART chooses up to 6 addresses from 32 VMMs to send
- Less accurate than sTGC centroid
  Simpler architecture
- Hope to use GBT for transmission

Strip Trigger Data Serializer ASIC

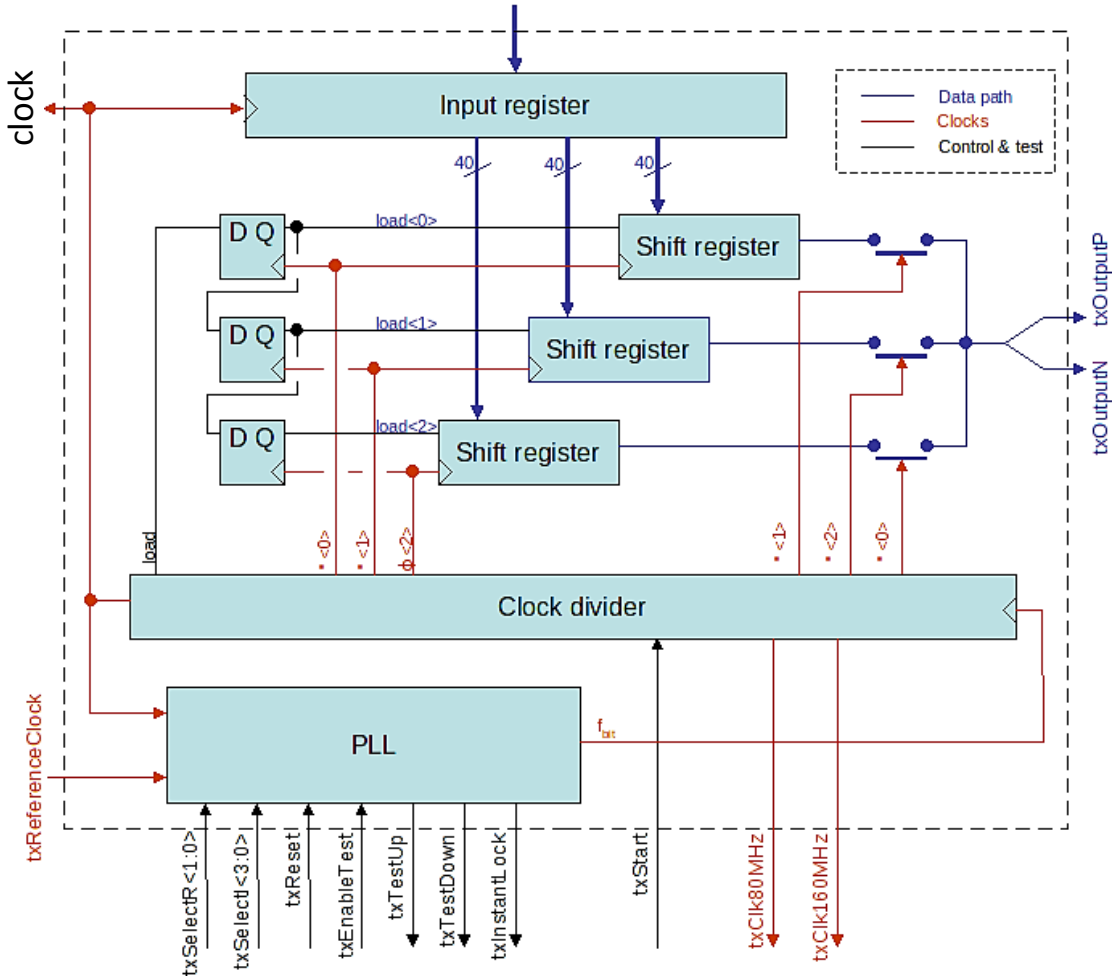
- Prepare strip trigger data to send to centroid finder:
  - match pad tower to a band of strips
  - serialize the FADC values of the band of strips for transmission to the Router board on the rim
- BCID, as determined by the Pad Trigger, is appended to the data
  ⇒ path to Trigger Processor has fixed latency, but is not sync'ed to BC at every step. Sync'ed to BC only on output to Sector Logic
- Rad tol, SEU mitigation, IBM 130nm
- Working on the 1st TDS prototype design
- Requires 5G serial output over twinax to Router
- Submitted Serializer core: ~1mm^2, 300 mW, 1.5 V, back 28 April

Strip Trigger Data Serializer ASIC



TDS output serializer

Input 30 bits @160 MHz
GBT: 120 bits @40MHz



GBT latency is too long for our trigger path.

Serializer requirements:

- Low latency: 70ns TX + RX
- Fast serialization speed (~5 Gb/s)
- Low power consumption
- Radiation tolerant
- Use the same clock frequency as used by the logic circuits

Modified the GBT serializer design:

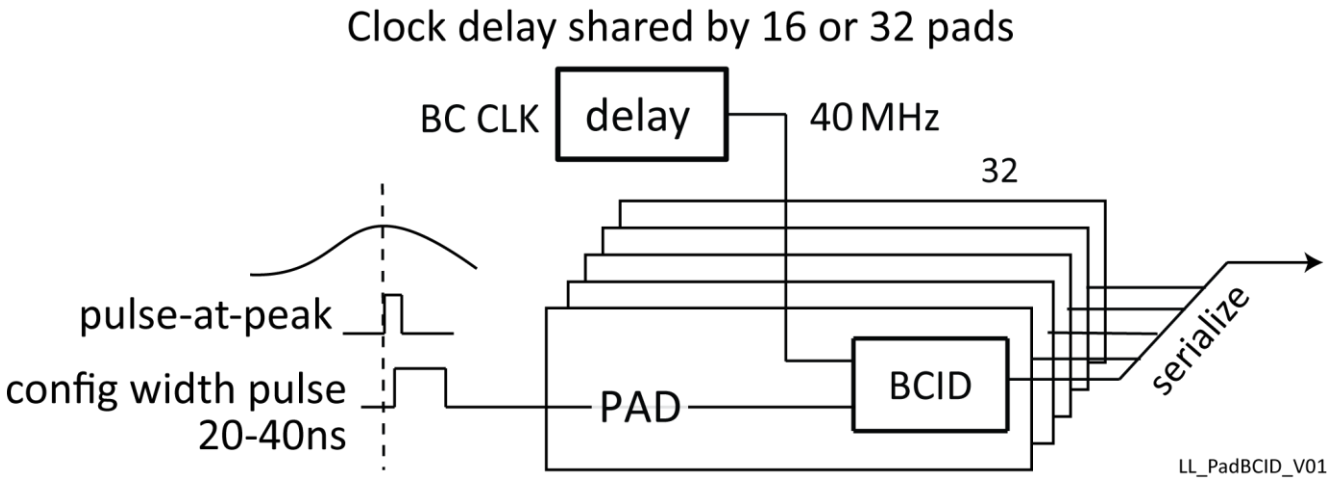
- Loading 30 bits at 160 MHz instead of loading 120 bits at 40 MHz (reduce the overall latency, seamless interface to logic running at 160 MHz)
- Convert IBM 8RF LM62 to DM323 (co-production with VMM)

Expect TDS to Router latency: ~65ns

sTGC Pad Trigger Data Serializer ASIC

- Assigns each pad signal to a bunch crossing
  - 1 bit per pad per BC
- Serialize and transmit in 1 BC to Pad Trigger on rim of wheel
- Rad tol, SEU mitigation, IBM 130nm
- Serialization under discussion:
  64 or 96 pads at 5G (using strip serializer), or
  32 pads at 1.6G, or 16 pads at 0.8G

  Depends on latency, number of deserializers in Pad Trigger FPGA, cables

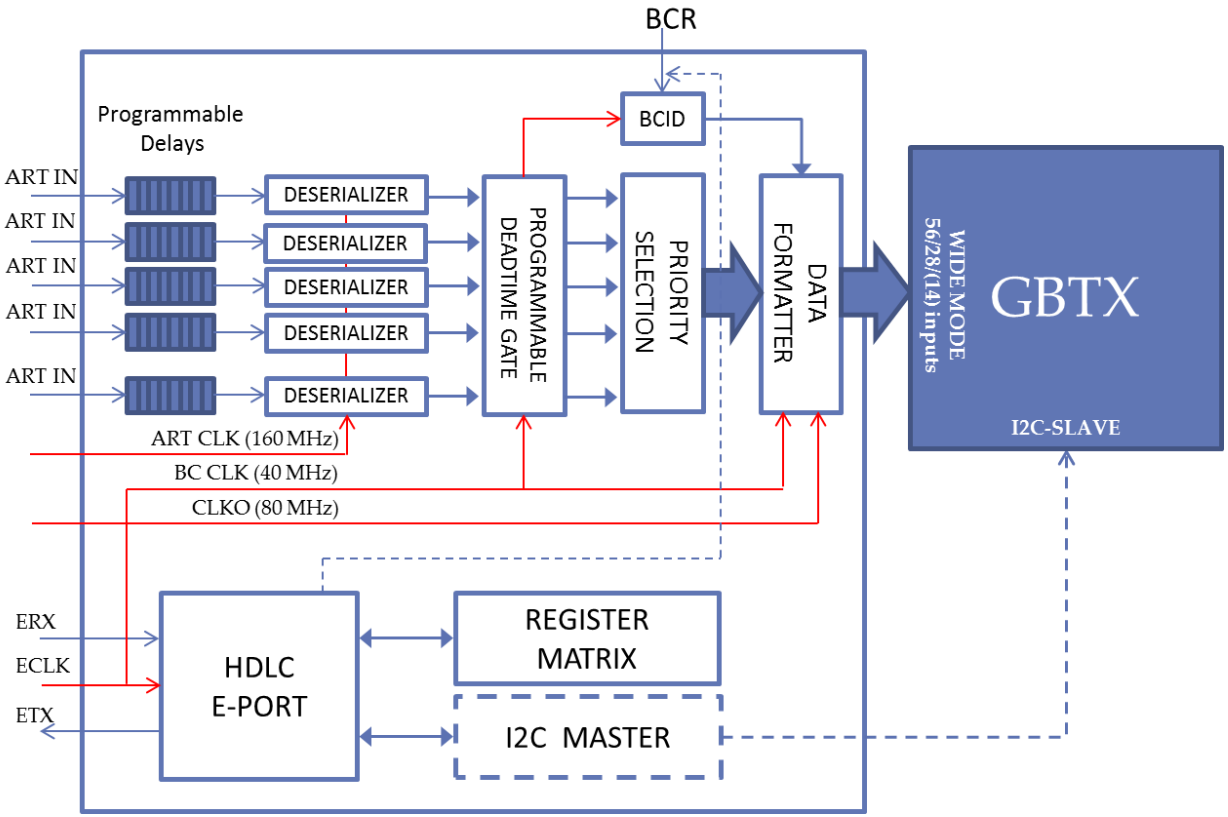


sTGC Pad trigger

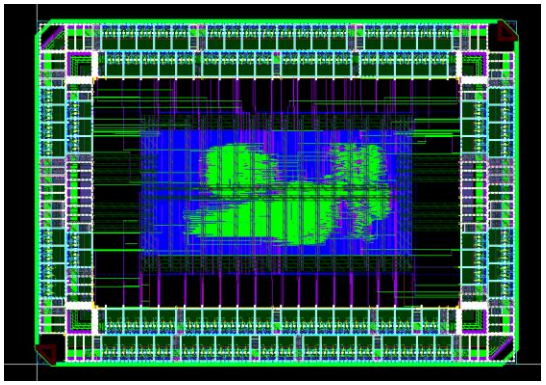
- One per 1/16th sector, on rim of wheel
- Receives: Pad signals synchronized to BC clock
- Builds tower coincidences from 3-out-4 coincidences in the two quads
- Identifies which bands of strips should be read out to the centroid logic
  - Priority encode bands so there is at most one coincidence per Outer/Middle/Inner region
  - Send band ID, ϕ-ID for each of O/M/I region to strip TDS
- Provides the BCID tagging of the strip trigger data
- FPGA, so it can be programmable, but
  On periphery of wheel, but SEU mitigation still required
- Readout on Level-1 Accept, but also must report monitoring of non-triggering BCs.
- Being prototyped with Xilinx Kintex

Micromegas trigger "ART" ASIC

- 32 serial ART inputs from 32 VMM front-end chips
  chooses up to 8 hits for transmission to Trigger Processor via GBT
- Rad tol, SEU mitigation, IBM 130nm
- 1st prototype expected end April, 4mm x 2.85 mm



1024 chips:
32 per 1/16th sector
4 per layer



sTGC Router

- Routes strip hits from strip TDS to Trigger Processor in USA15
- One Router per layer per sector
- 5G serial inputs from several TDS ASICs
- Assumes only one per radial region is actively sending data in each bunch crossing and routes that one to Trigger Processor in USA15
  - Up to 3 output fibres per Router to USA15
  - Will use Versatile opto-electronics, but not GBTx
- Reduces latency by discovering which inputs are active before the whole frame is received and sets up routing for that link ("cut-through routing")
- On periphery of wheel, but SEU mitigation still required
- Being prototyped with Xilinx Artix, ?? IGLOO2
- Option to 10G output using Multi-Rate Transceiver

On-chamber power and cooling

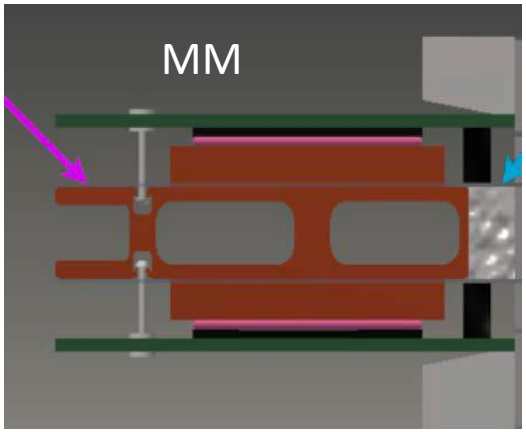
- 2 kW per 1/16th sector $\Rightarrow$ 64 KW at 1.2V
- Active cooling
- Point-of-Load DC-DC conversion
  24V (or 12V) to 1.5V on front-end boards
- Hope for rad-tol, mag-tol COTS DC-DC converters
  fall back is the CERN rad-tol POL DC-DC
- Can moderate demands on COTS by avoiding extreme areas

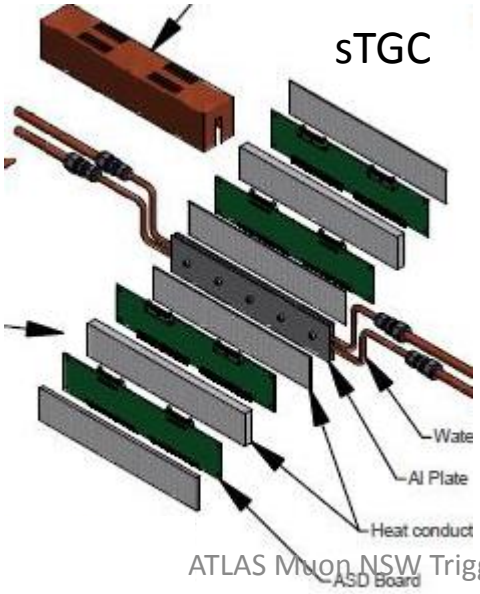
Rim:

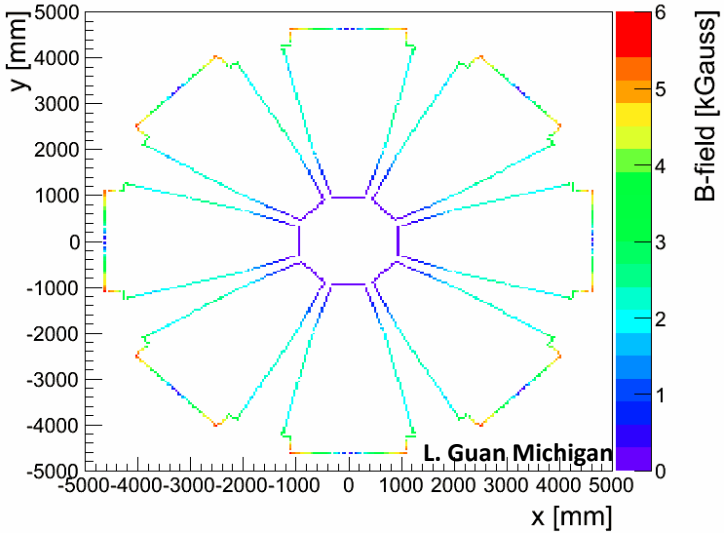
- TID: 9 kRad
  NIELS: 2E13/cm^2
  B: 6 kG

Inner:

- TID: 340 kRad
  NIELS: 8E14/cm^2
  B: <1 kG



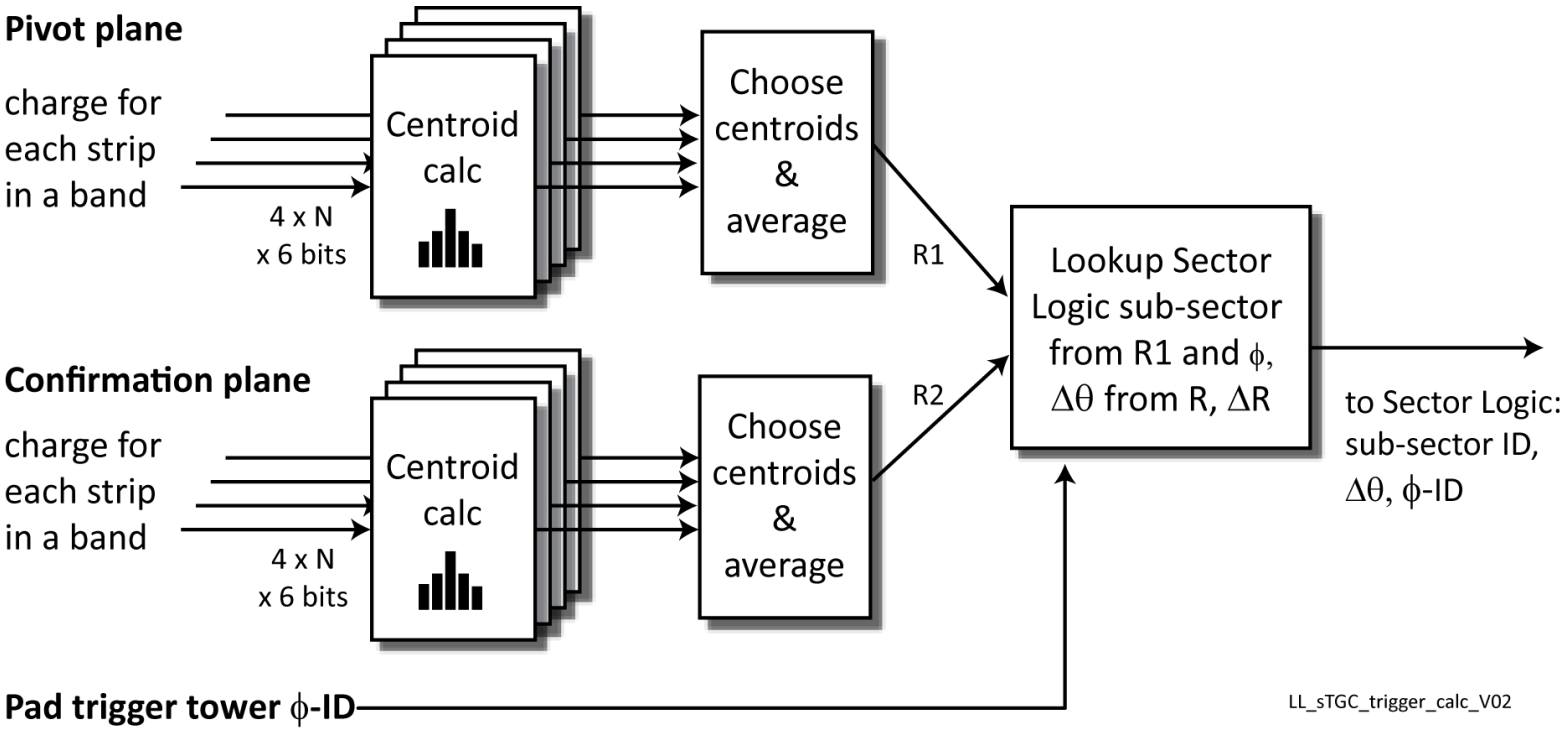




Optical links

- GBT used for readout, TTC, calibration, configuration and MM trigger
- GBT latency marginal for Micromegas, unacceptable for sTGC
  ⇒ custom links for sTGC from on-chamber ASICS to Router (5G twinax)
  and Router to USA15 trigger processor (5G or 10G fibre)
- Must preserve the redundancy of (16) detector layers
  - Perhaps yearly access to periphery
  - Extremely difficult to replace front-end boards
- No point of failure should disable more than one layer of a sector
  - Applies to trigger data sources, TTC distribution, power…
- Results in proliferation of optical links: each layer must have a link
  ⇒ very low link occupancy
  - 1024 Readout links: 512 bi-dir GBT links each for MM and sTGC
  - 1024 (MM) + 768 (sTGC) uni-dir trigger links

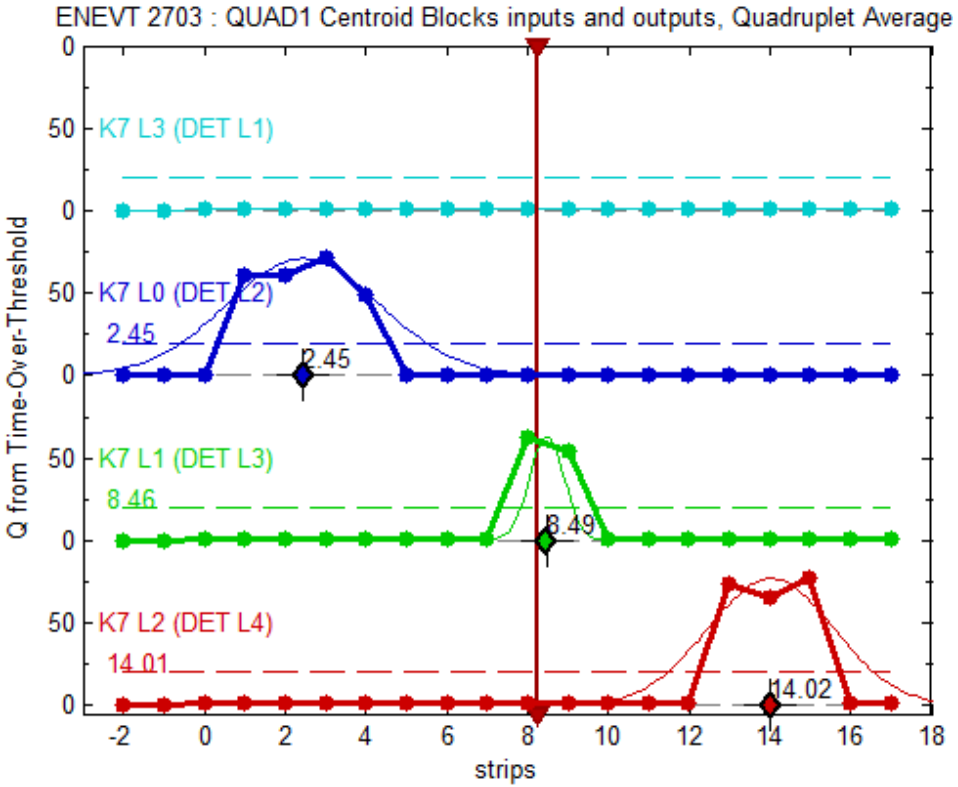
sTGC trigger algorithm



- Use average of centroids in each quad to define space points R1 & R2
- 1, 2, or even 3 of the 4 centroids of a quadruplet are omitted from averaging if:
  - δ-ray's: wide (>5 strips)
  - Neutrons: large charge or wide
  - Noise: single strip
  - Pileup, i.e. pulse in a component strip is active before the trigger

sTGC centroid finder demonstrator

- Cosmic ray test of one quadruplet
- Trigger demonstrator using Xilinx Virtex-6 evaluation board
- Custom mezzanine cards to accept the ToT signals from 8 (16-chan) FE VMMs, 4 strip + 4 pad layers:
  - Triggers on 3-out-of-4 pad layers
  - Calculates Time-over-Thresholds (VMM1 does not have 6-bit FADC)
  - Finds 4 centroids
  - Selects and averages centroids
  - Sends inputs and outputs to ethernet for recording, playback
- Latency of centroid calc: ~45ns

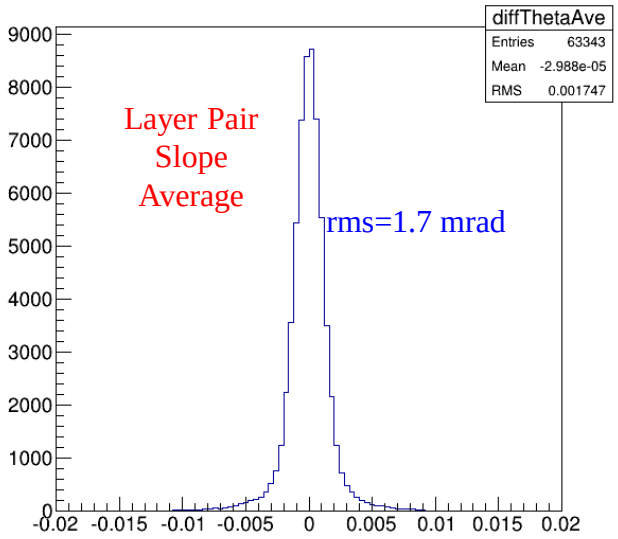


A cosmic ray passing at an angle thru' a quadruplet.

♦ are the centroids (values on the left)

Vertical line is the calculated average.

Micromegas trigger algorithm I



Theta Resolution at the entrance of the Muon System

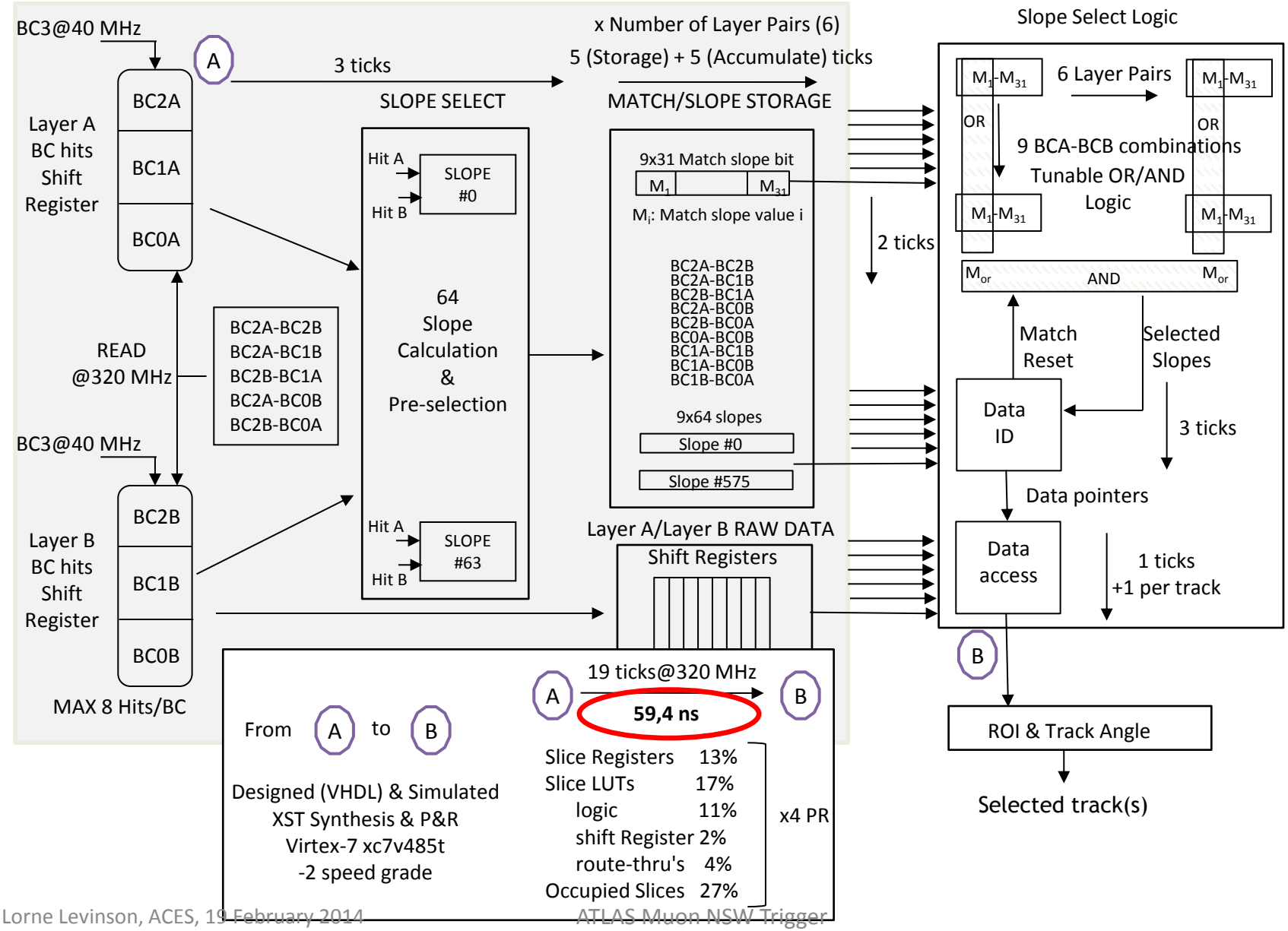
Local straight track selection based on strip number difference with strip precision

Local segment slopes calculation between hits of Layers belonging to the same Layer Pair over 3 BCs.

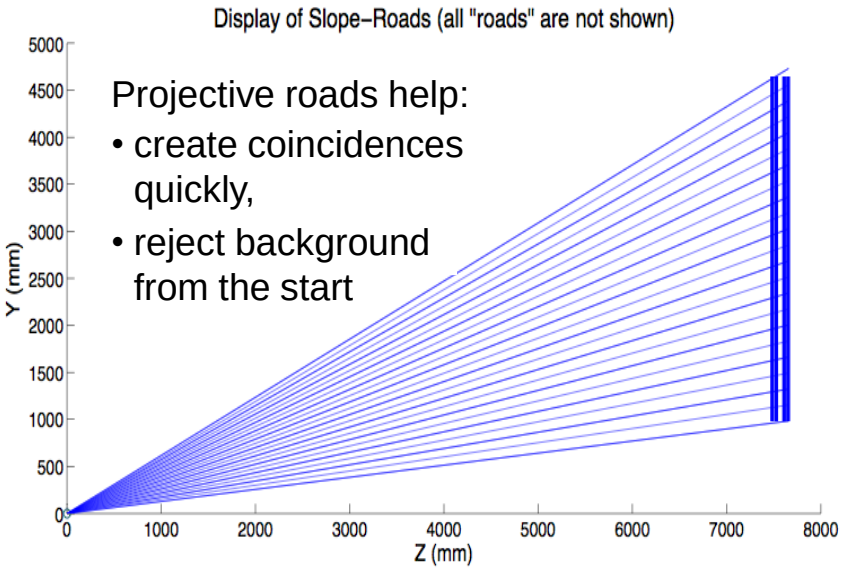
→ X_0 X_1 X_2 X_3 U V
Matching slope = track candidate

Contacts: samira.hassani@cea.fr, herve.le-provost@cea.fr

Implementation for 2048 strips x 8 Layers



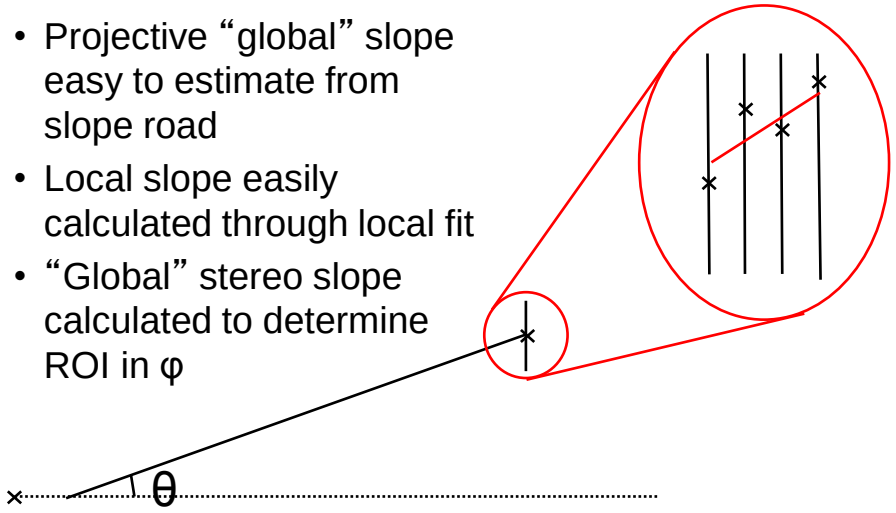
Micromegas trigger algorithm II



Projective roads help:

- create coincidences quickly,
- reject background from the start

- Projective "global" slope easy to estimate from slope road
- Local slope easily calculated through local fit
- "Global" stereo slope calculated to determine ROI in φ

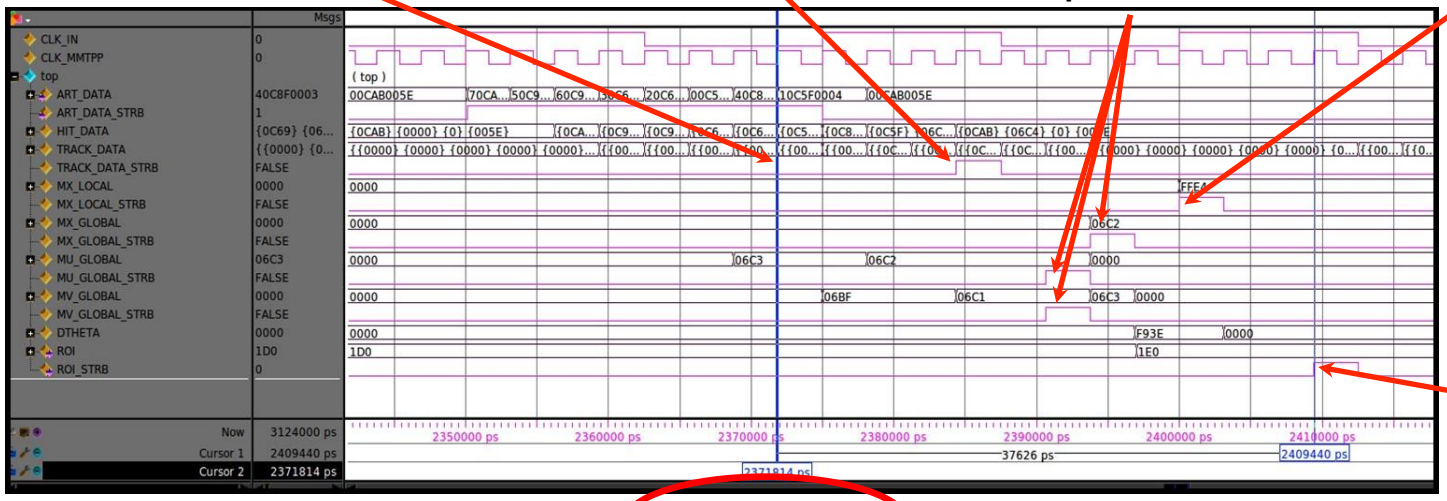


Arrival of the last hit on the GBT link

Coincidence candidate formed

Global horizontal/stereo slopes calculated

Local slope calculated

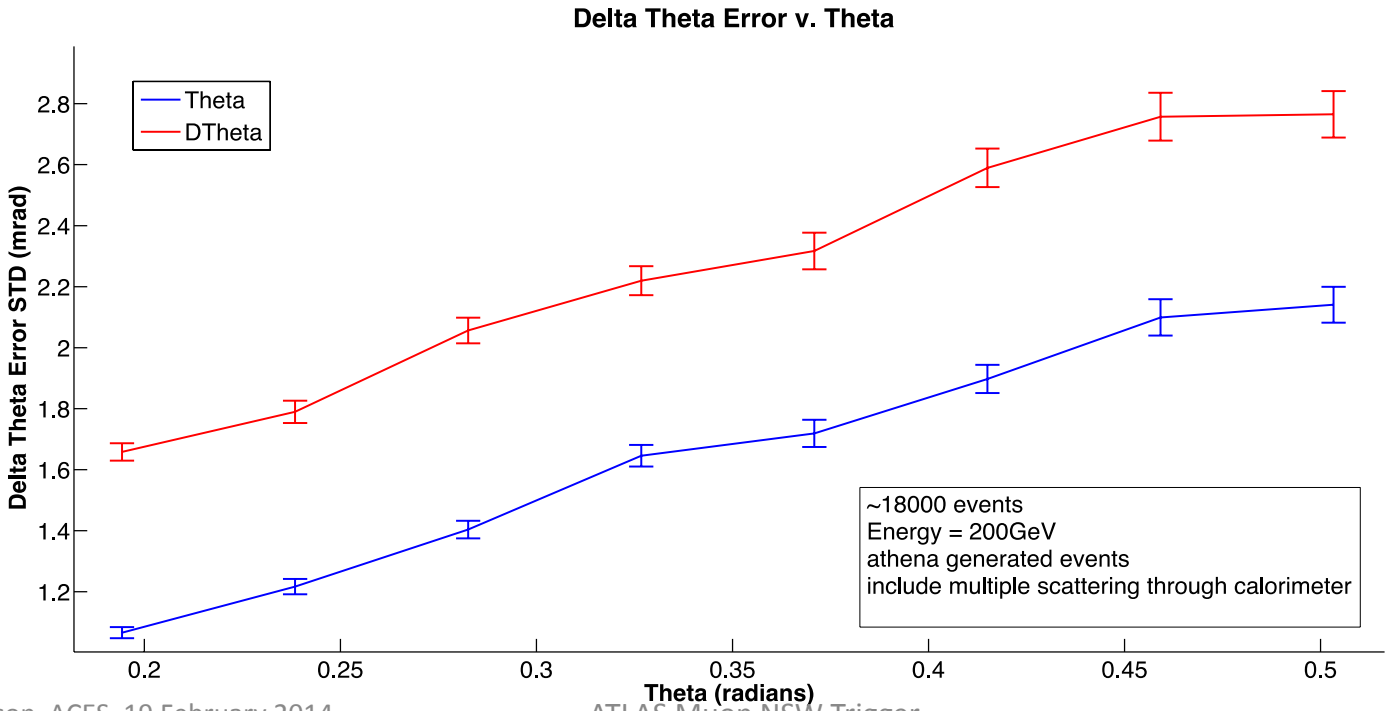


ROI determined

37 ns latency

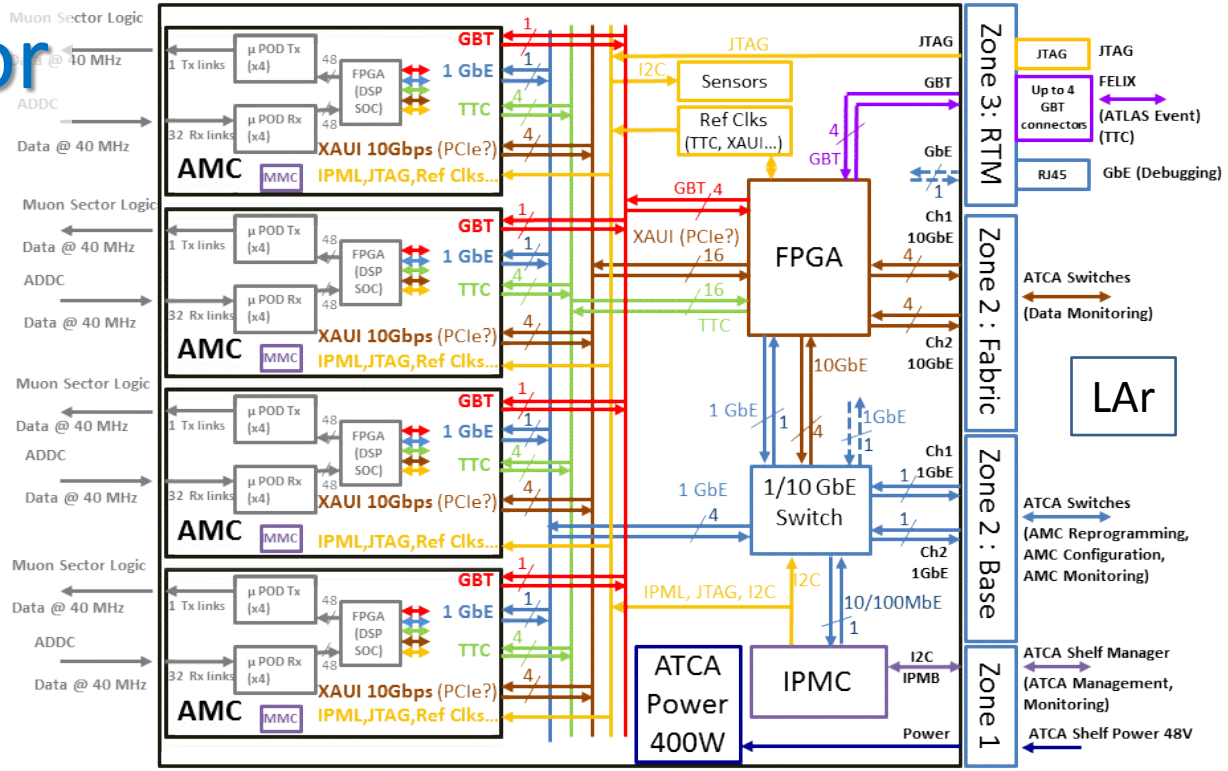
Performance summary -- algorithm II

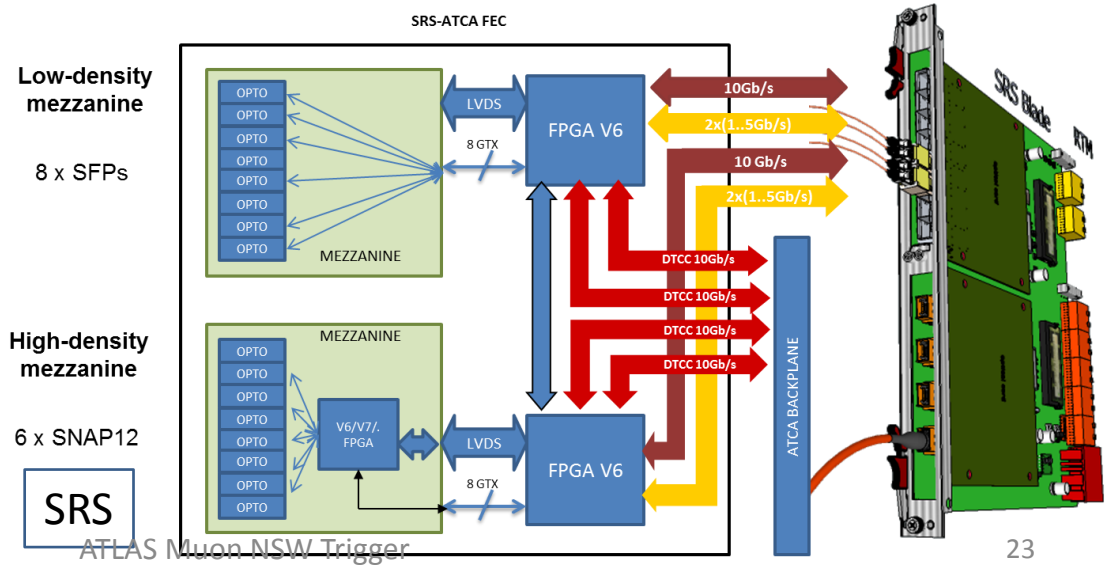
- Algorithm efficiency essentially 100%
- Inefficiencies related to hits with late raise times, detector gaps, low-ionization hits
- Inefficiencies caused by simulated incoherent backgrounds are small
- Irreducible inefficiencies due to muon brem @ 1 TeV at 5% from showering
- Algorithm intrinsic resolution of measurement of $\theta^{\text{local(@NSW)}} - \theta^{\text{global(@IP)}}$ is 1.33mrad but affected by multiple scattering in the calorimeter



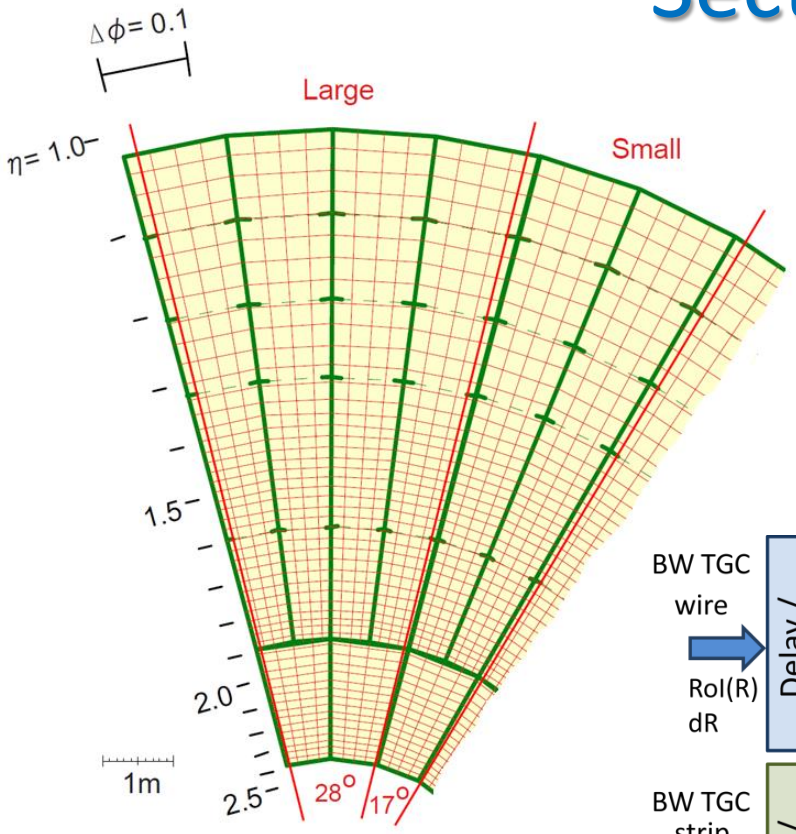
Trigger processor

- ATCA-based FPGA boards, one board per quadrant, 2 crates
- Input fibers per quadrant: MM: 128, sTGC: 96
- Separate MM & sTGC boards share candidates via ATCA backplane
- Try to avoid development of yet-another-ATCA-FPGA board
  Candidate carrier & mezz: LAr, SRS





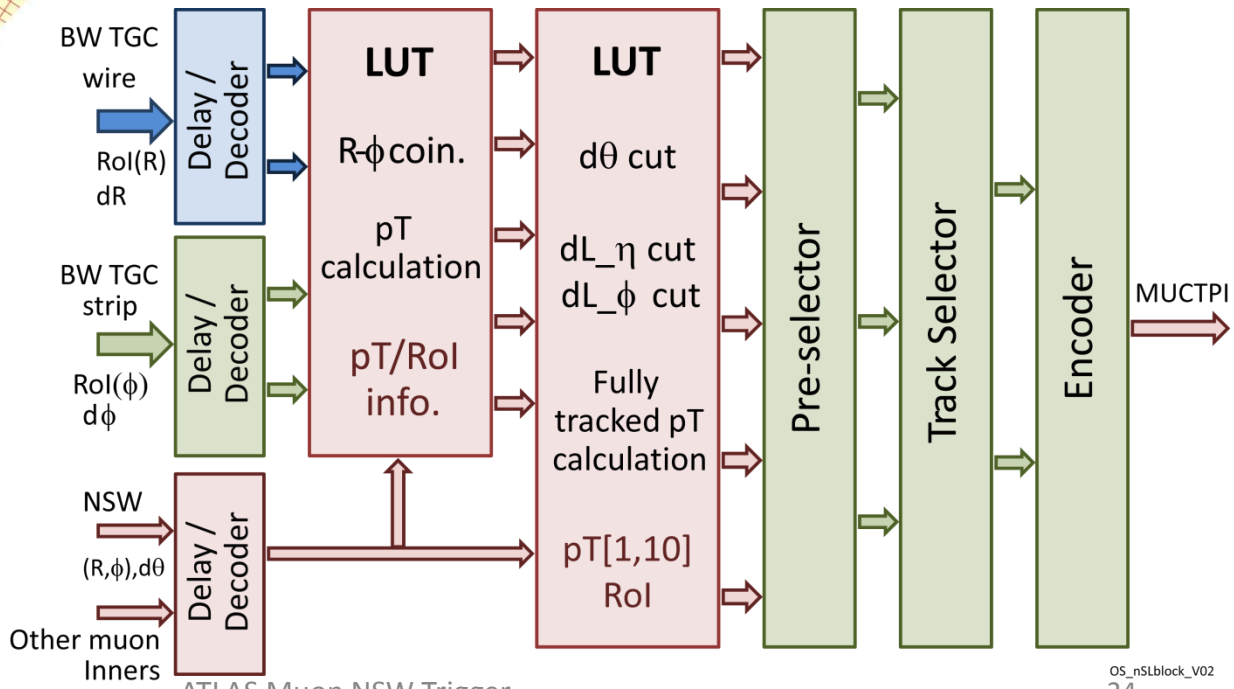
Sector Logic



- Finds candidates in R-ϕ, tagged by p_T
- Mismatch of NSW and BW detector boundaries
  $\Rightarrow$ fan-out to several modules

Big Wheel Regions-of-Interest to be confirmed by NSW.

Red lines are NSW sector boundaries.

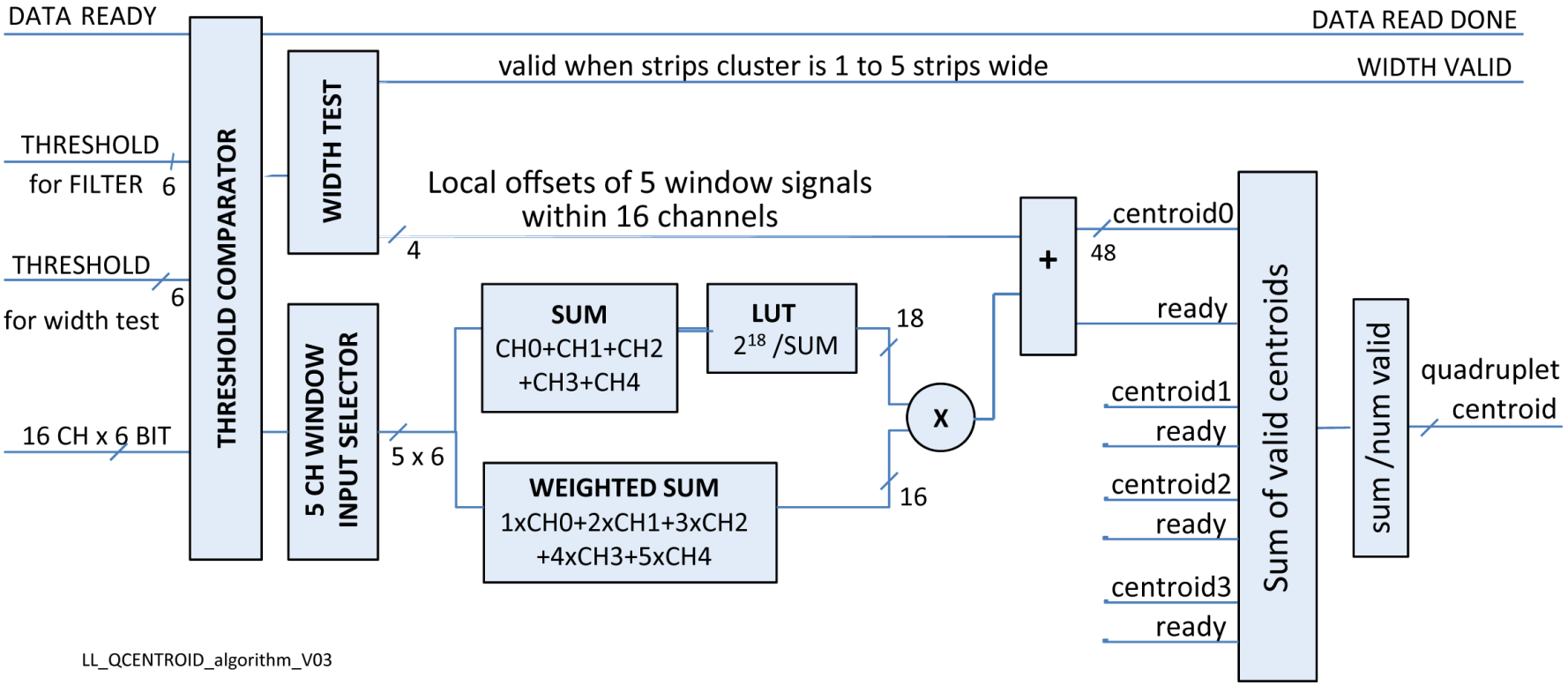


Other Phase 1 Muon upgrades

- Tile Muon trigger
- The new Sector Logic to MUCTPI interface board

Thank you

sTGC centroid calculation & averaging



LAr ATCA carrier and mezz board