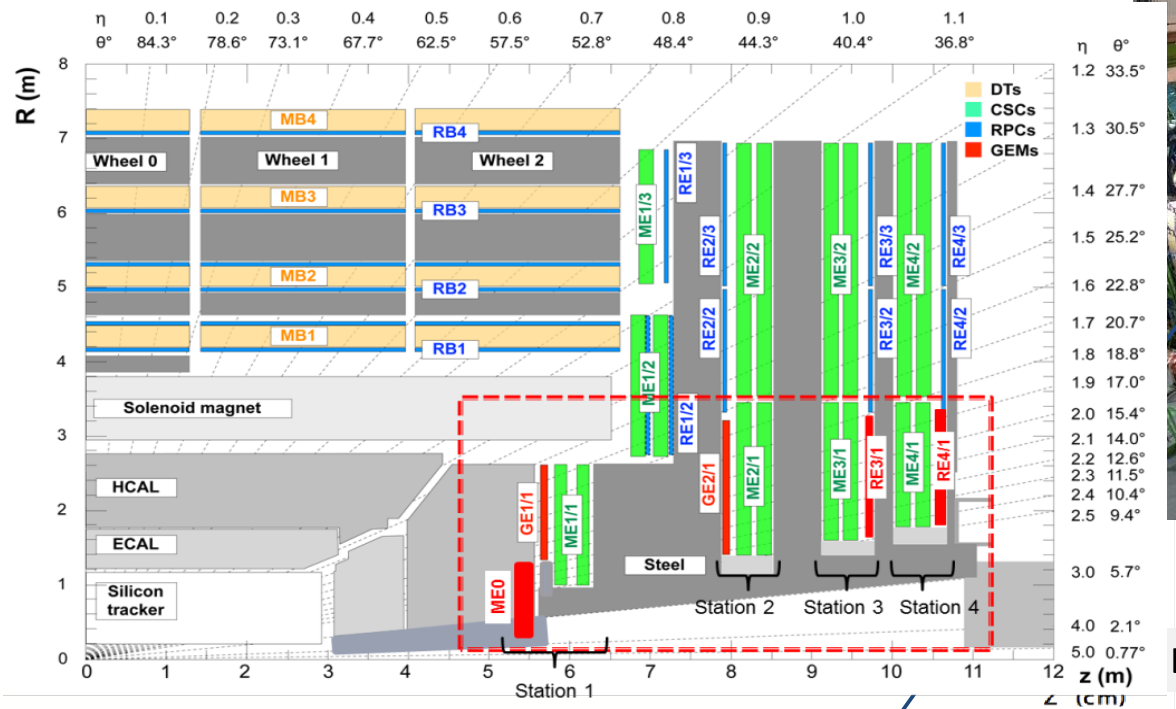
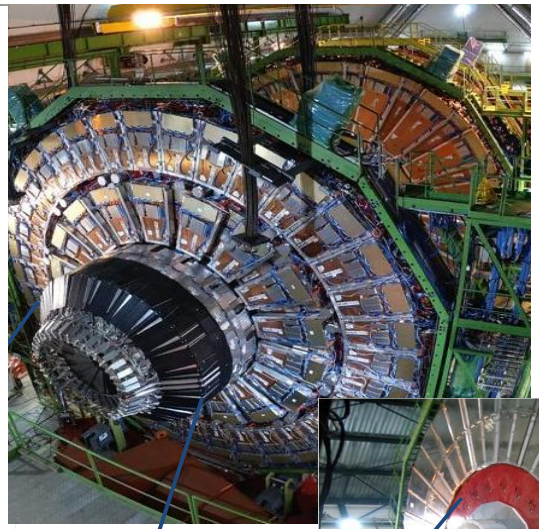
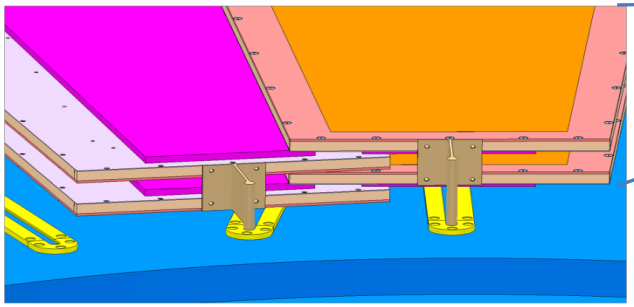
CMS GEMs – Electronics

Introduction: the CMS GEM Endcap system

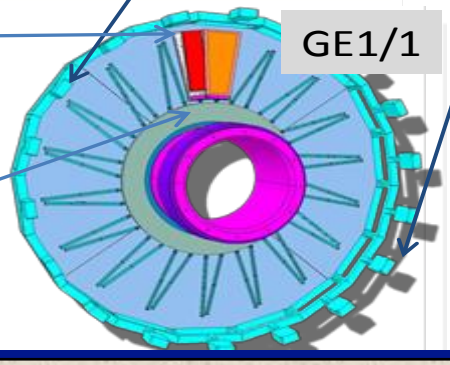


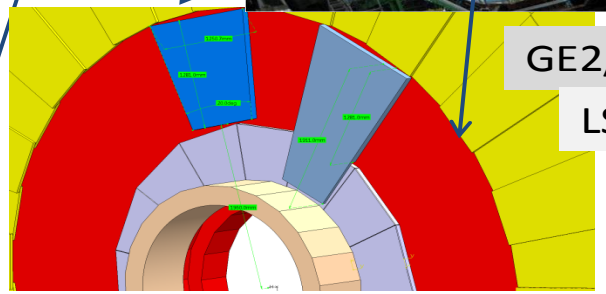


LS2



GE1/1

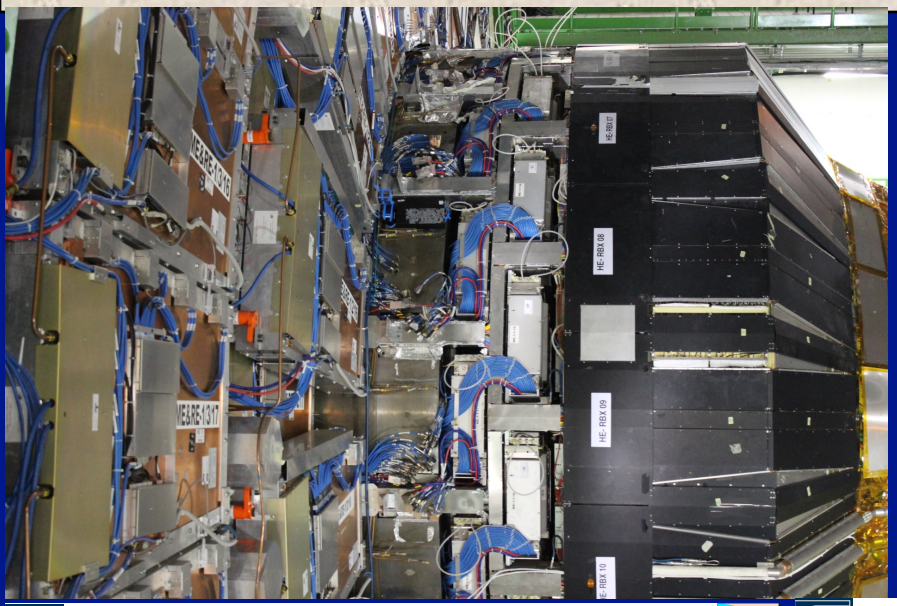


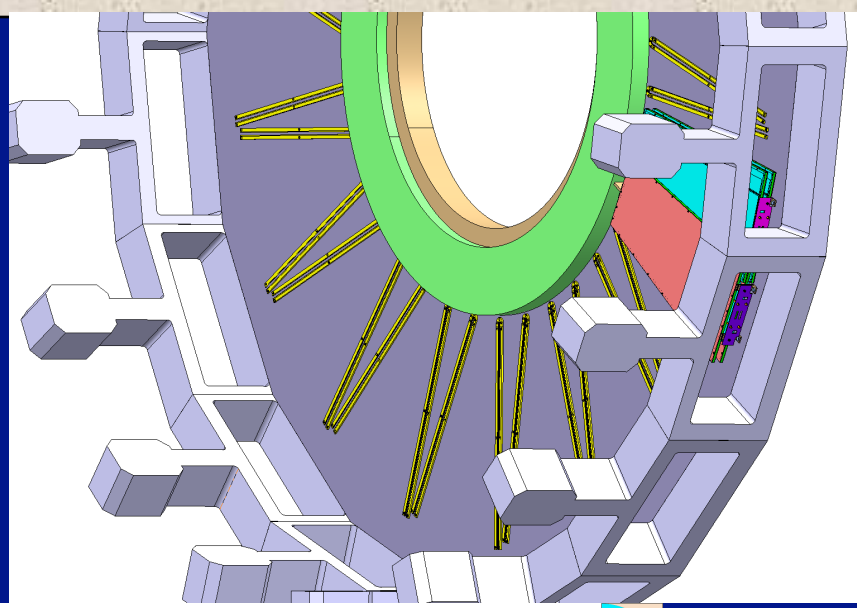


GE2/1

LS3?

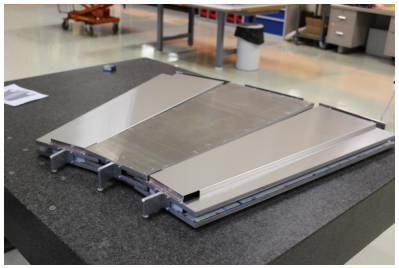
Installation Details : Detector Installation





GE1/1 Dummies

"Mounted" on the marble table



Excellent overlap. With 3mm clearance from each side.

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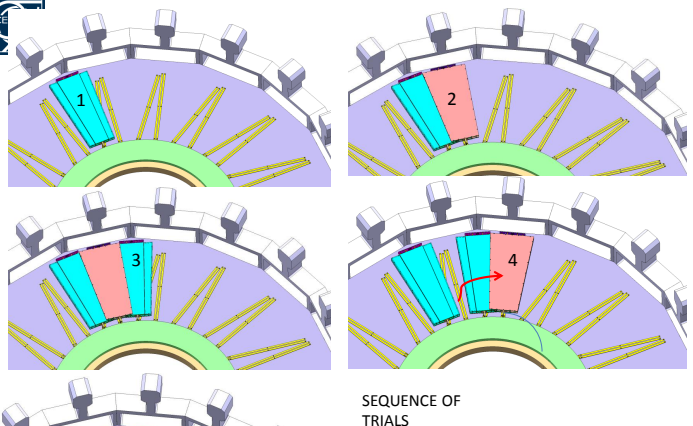

SEQUENCE OF
TRIALS
Depending on time available
All slots are desirable for no show stopper
In LS2
Tolerances of each slot could be slightly different

and so on…

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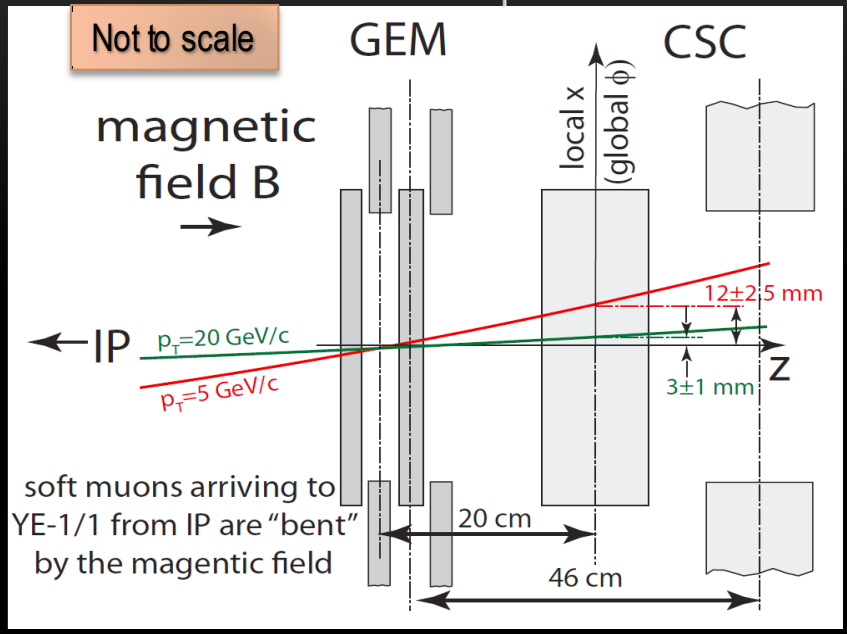
A Marinov
A Conde Garcia

A NEW KNOB: GEM-CSC "BENDING ANGLE"

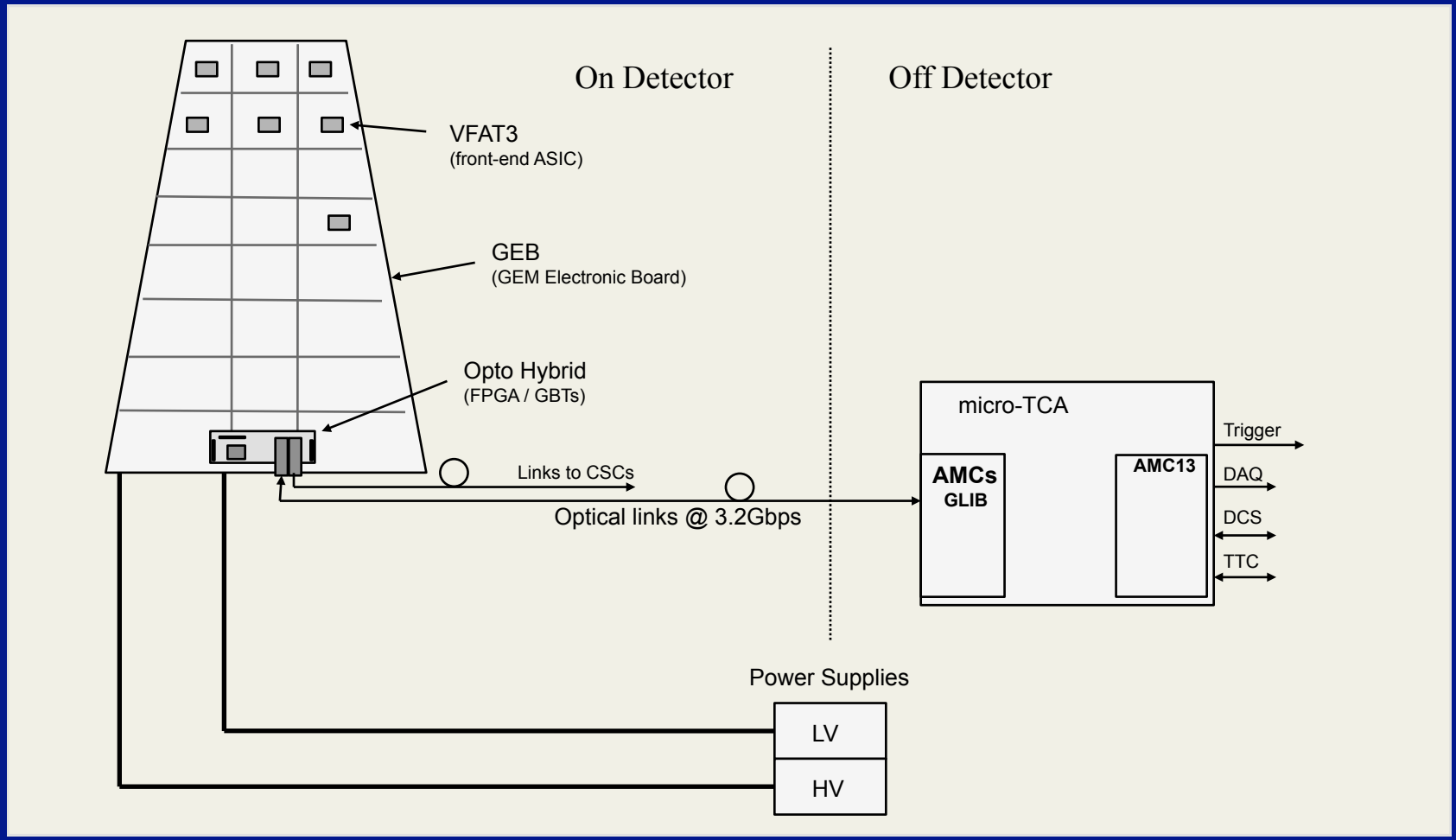
- L1 muon momentum resolution can be improved with a second detector:
  - Inner tracker tracks at L1 – best solution, but not available until LS3
- A second muon system could improve momentum resolution if one can measure the "bending angle"
  - Used in the Barrel; CSCs are too thin (~11 cm) to see the bend
- A new detector in YE-1/1 (the least affected by scattering, largest B)
  - Increase "lever arm" from 10 cm to Δz=30-50 cm (physical constraints)
  - Need ~2 mm or better trigger resolution to effectively discriminate 5 GeV muons from 20+ GeV ones



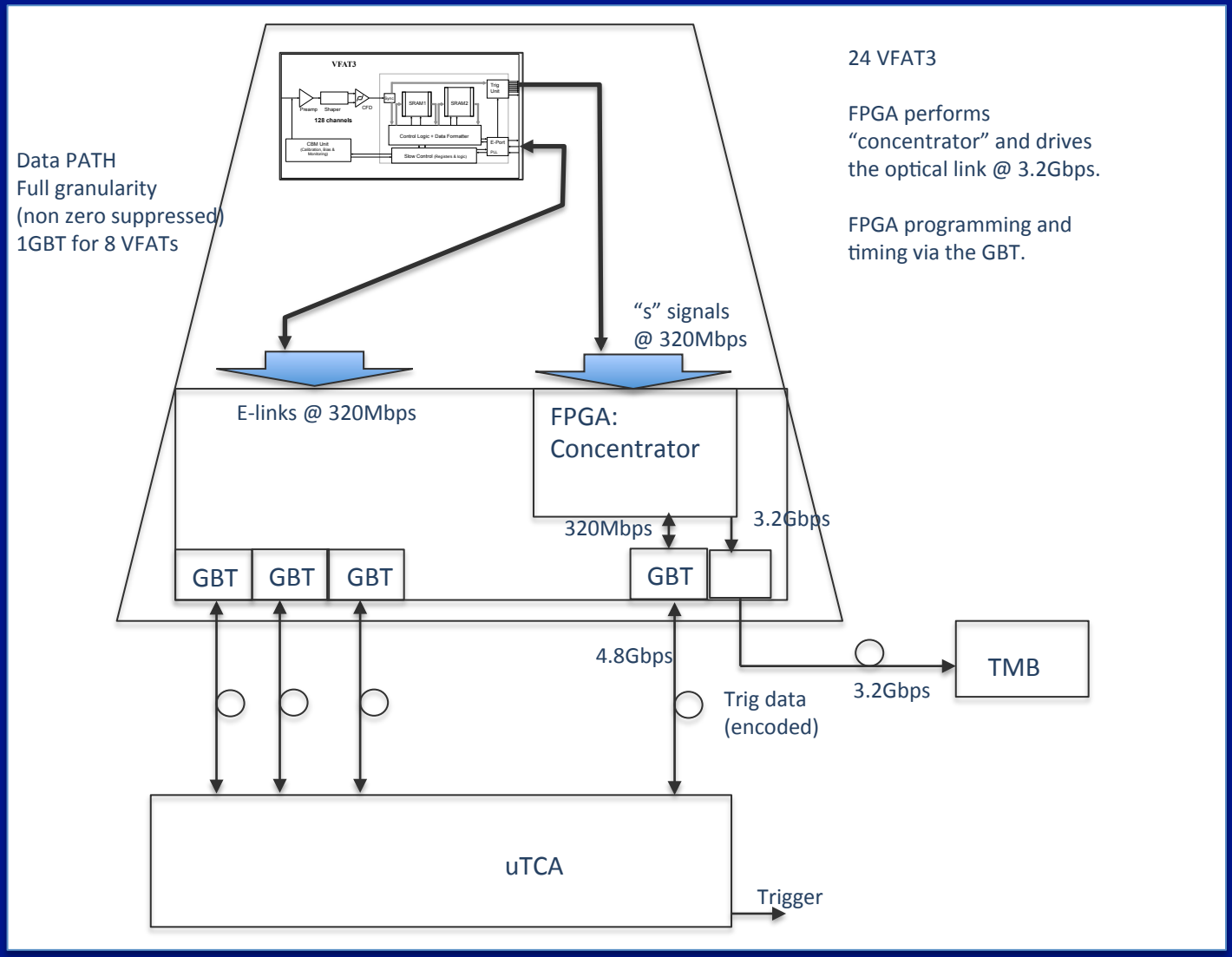
YE-1/1	p_T=5 GeV	p_T=20 GeV
$\Delta x_{\Delta z=30\ cm}$	12±3mm	3±1mm

Slide from : A. Safonov

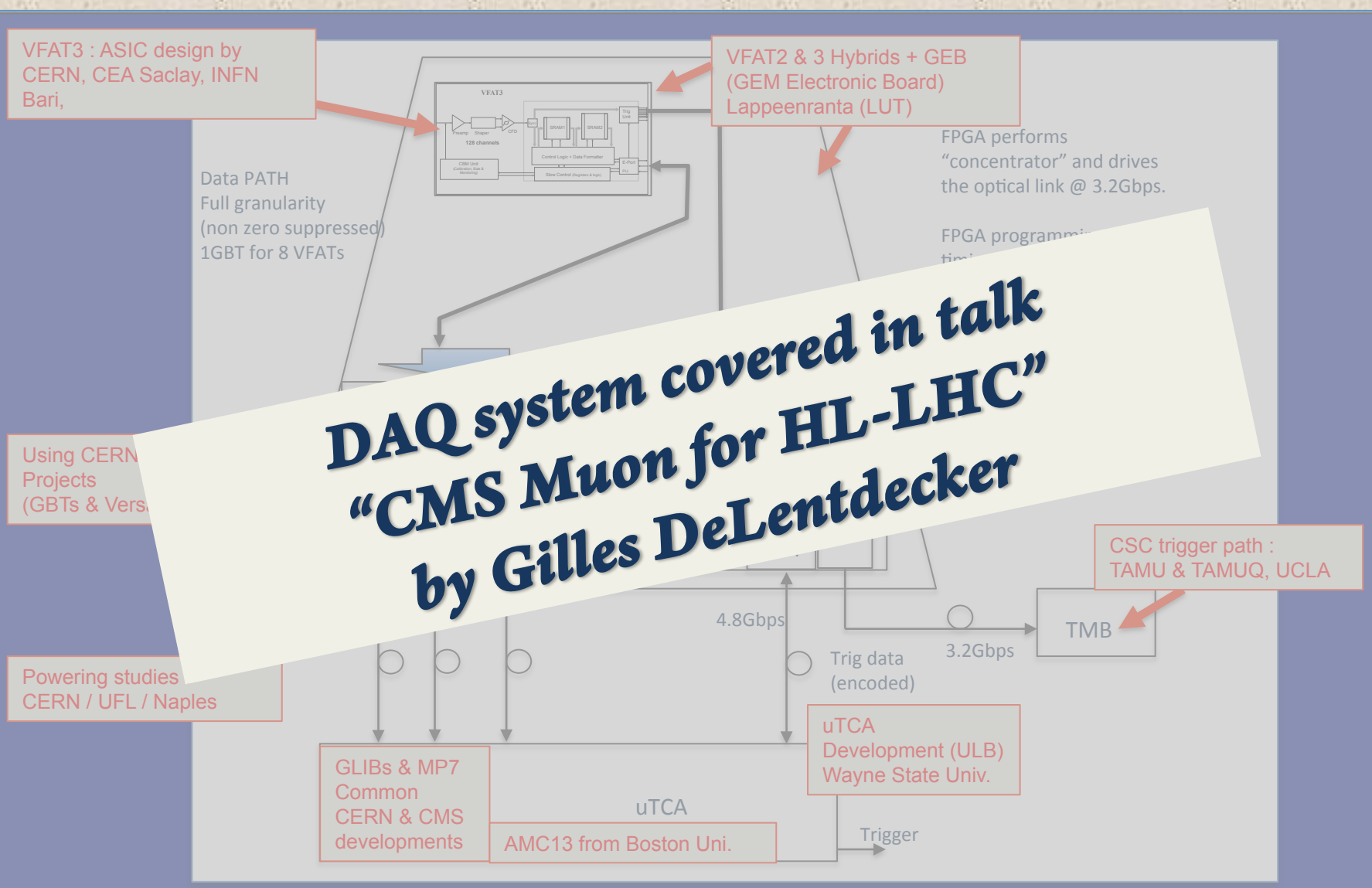
CMS GEM Electronics System



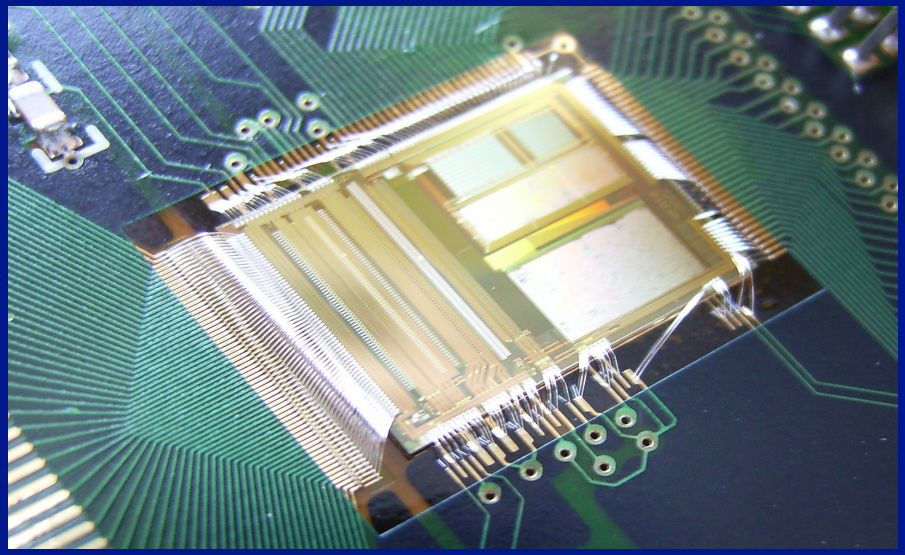
The Electronics System



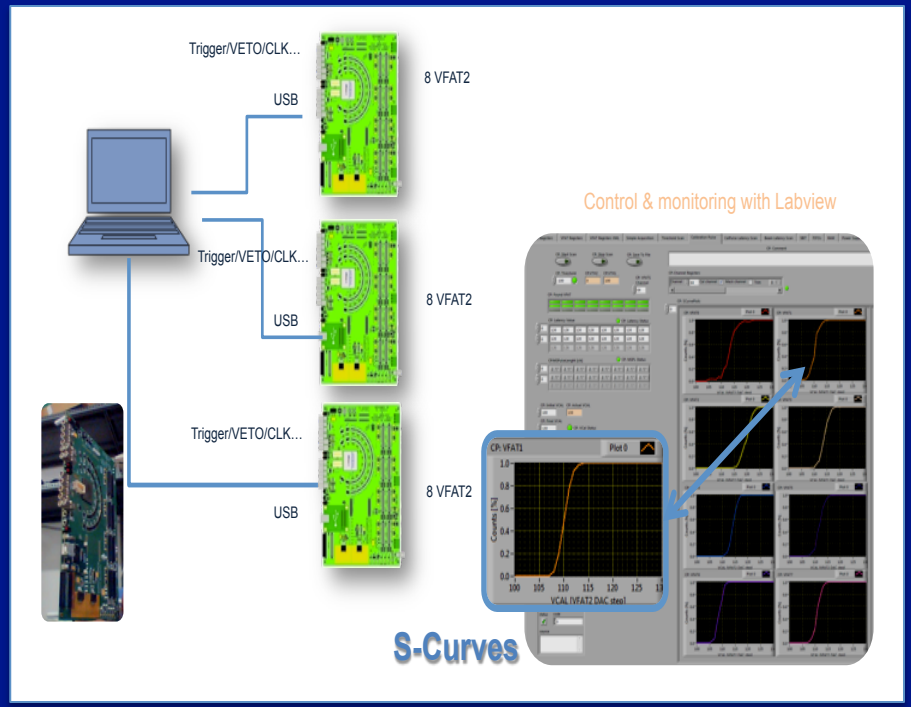
The Electronics System



Front end Electronics
Existing– VFAT2 + Turbo



- Initial system
- VFAT2 (developed for TOTEM)
- Totem T2 Hybrids
- Turbo readout board (Sienna)
- Used in beam tests & lab characterisation.
- Provides triggering and tracking



Main reasons to move from VFAT2 to VFAT3

- For both Trigger and Tracking we require binary hit data with channel location and time stamp accurate to one clock period.

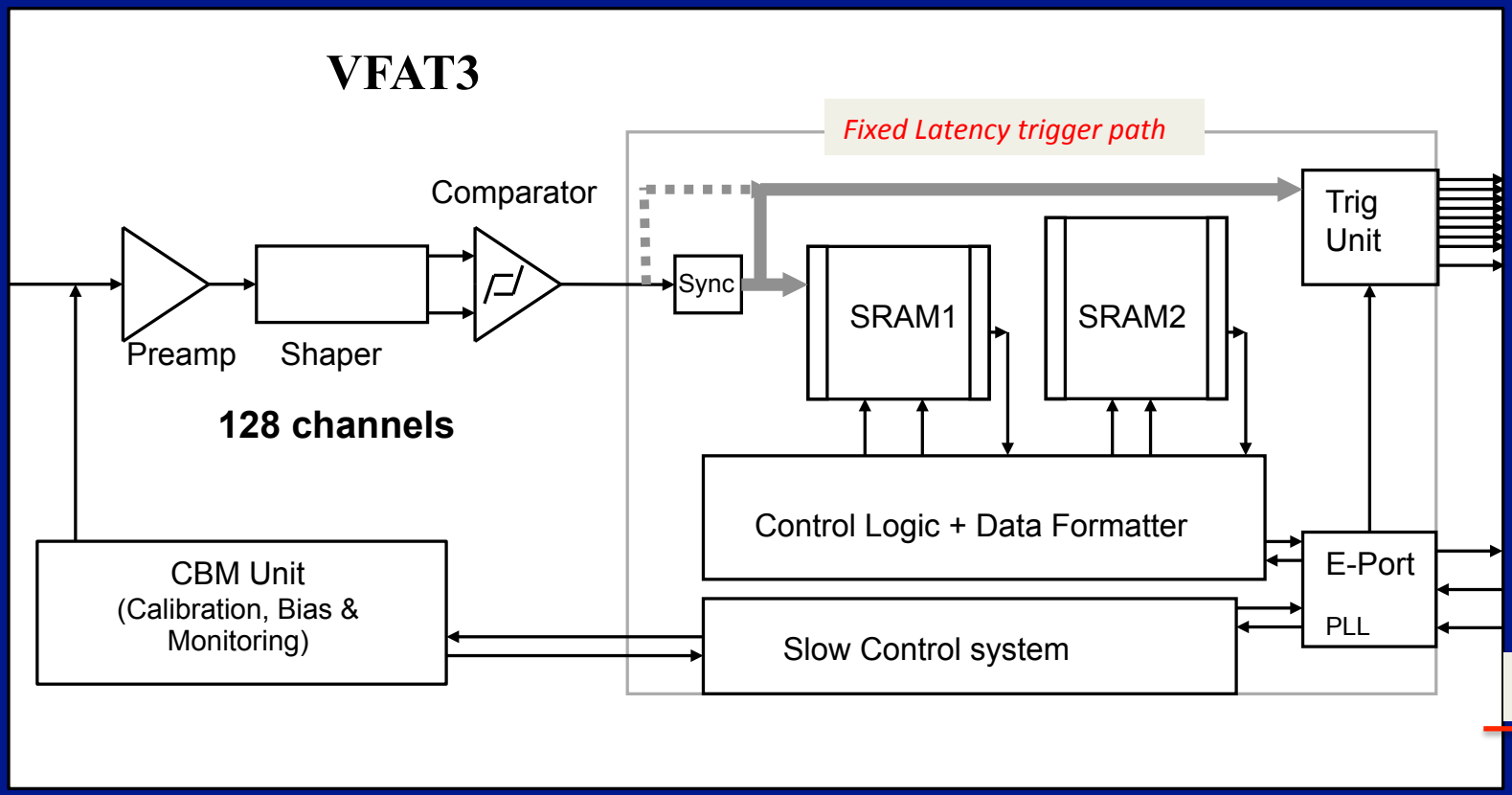
- VFAT2

- Maximum trigger granularity = 16 channels
- Fixed shaping time = 25ns
- Data output rate limited to 40MHz.
- Max LV1 latency = 6.4us (CMS=3.2uS)
- Max LV1 rate = 200 kHz (CMS=100kHz)

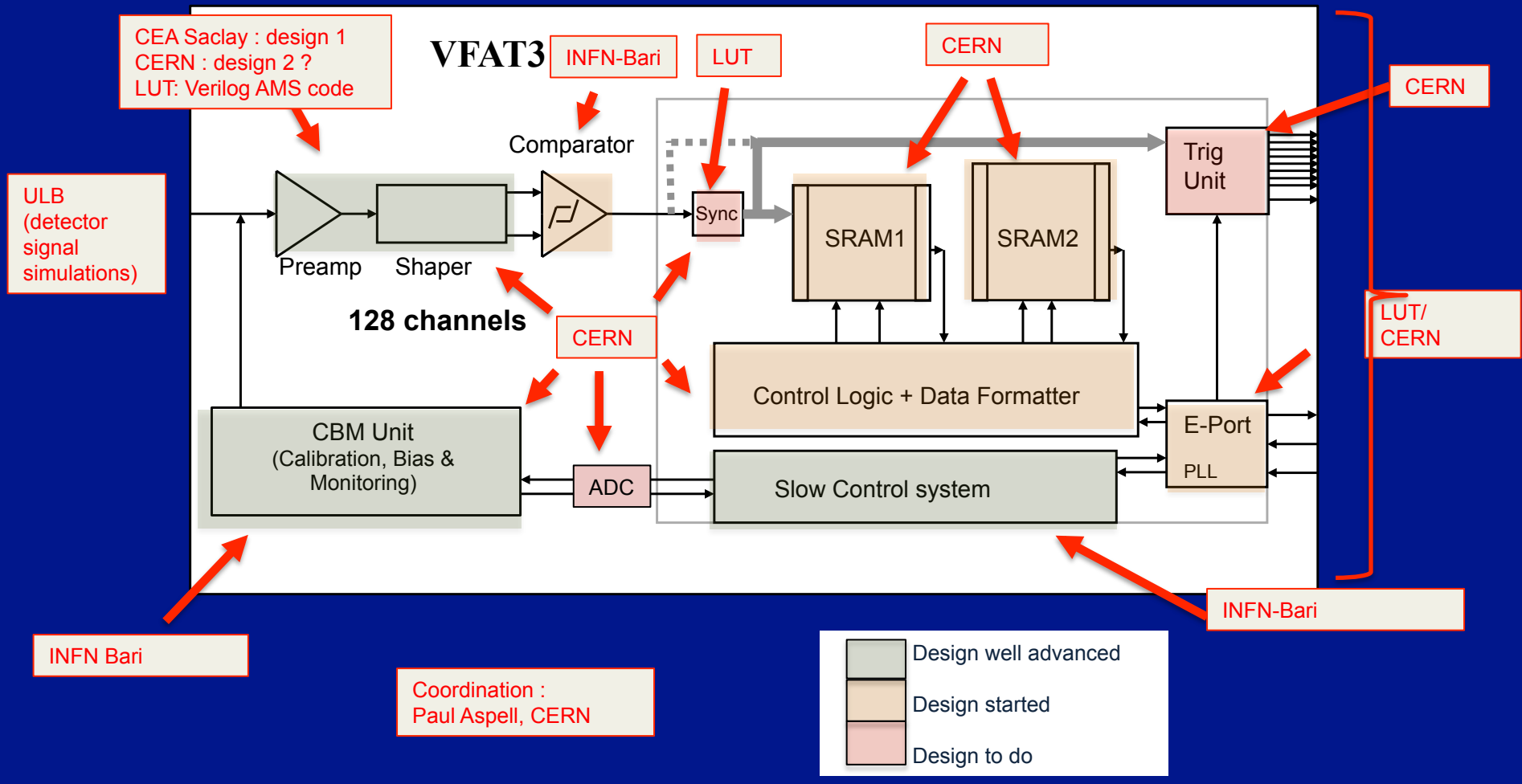
- Principle additional functionality required by new ASIC

- Increased granularity at trigger level.
- Programmable shaping time, avoid ballistic deficit and improve S/N whilst maintaining timing resolution.
- 320Mbps e-link for data output (compatible with GBT)
- Max LV1 latency > 20us
- Max LV1 rate > 1MHz

VFAT3


VFAT3
Fixed Latency trigger path
Comparator
Trig Unit
Sync
SRAM1
SRAM2
Preamp
Shaper
128 channels
Control Logic + Data Formatter
E-Port
PLL
CBM Unit
(Calibration, Bias & Monitoring)
Slow Control system
Tracking path After LV1

VFAT3 design institutes



Detector Studies & Timing Resolution

Timing resolution determined by detector.

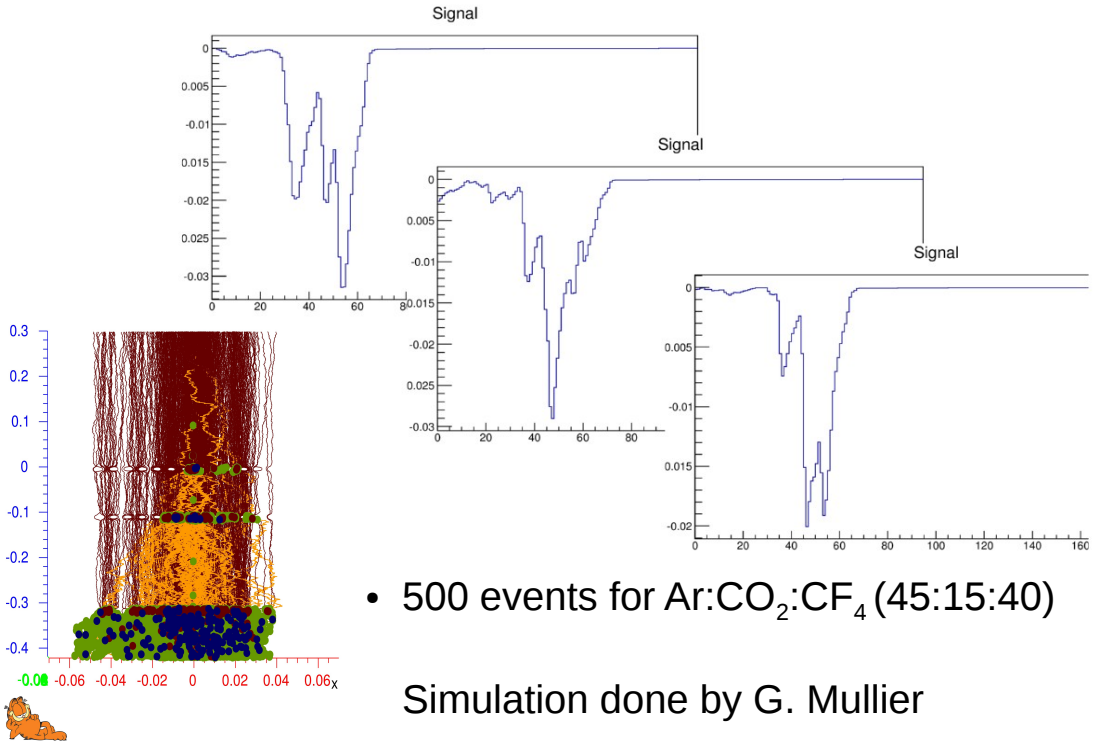
Fast shaping (as with VFAT2) give good timing resolution (<6ns) but bad signal to noise due to ballistic deficit.

Slower shaping times give better S/N but worse timing resolution due to time walk.

VFAT3 analog discriminator would use CFD or TOT to correct time walk and recover timing resolution.

ULB

GARFIELD simulations



- 500 events for Ar:CO_2:CF_4 (45:15:40)

Simulation done by G. Mullier

2

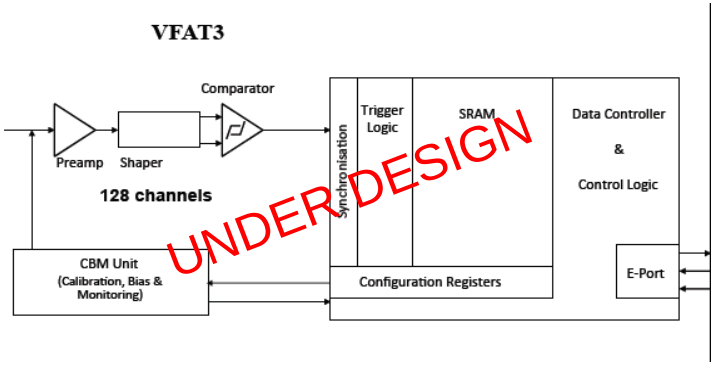
T.Maerschalk, ULB

Combining detector charge with front-end

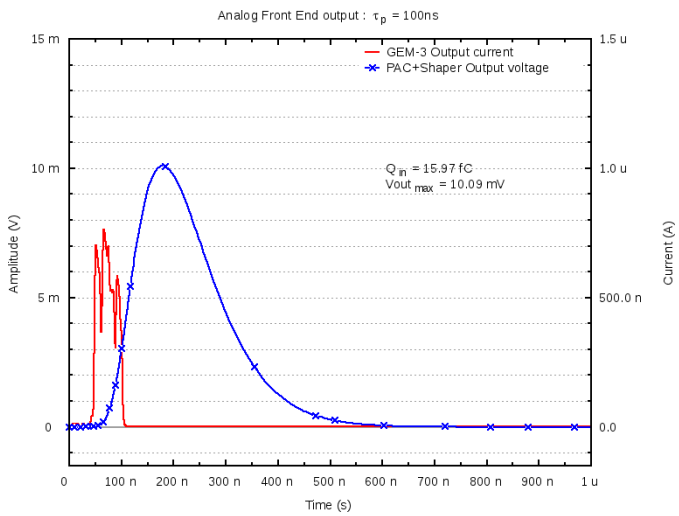
ULB

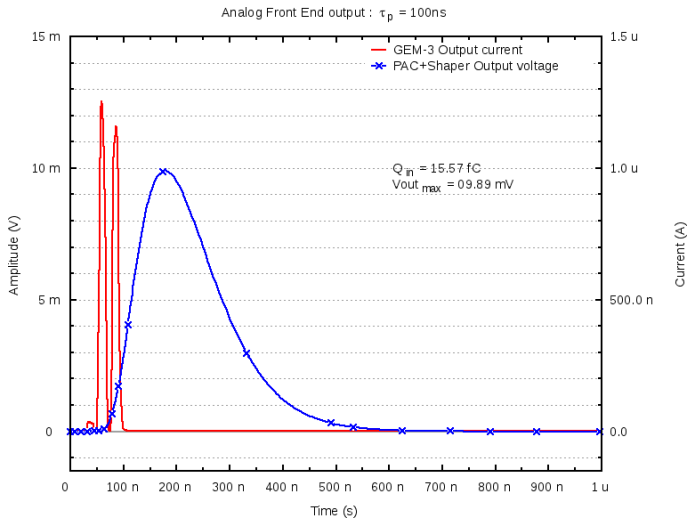
Electronics - VFAT3

Fabrice Guilloux



- "old" design :
  F(t) = (t/Tau)^n * exp(-n*t/Tau)
  n = 2
  Tau = 20, 50, 100, 250, 500 ns
- "new" design :
  F(t) = (t/Tau)^n * exp(-n*t/Tau)
  n = 3
  Tau = 1.1 * (25, 50, 75, 100, 200, 400 ns)



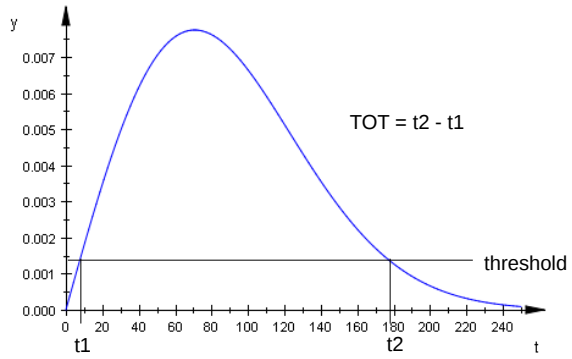


T.Maerschalk, ULB

Recovering Timing Resolution in VFAT3 TOT and CFD

ULB

Time Over Threshold (TOT)

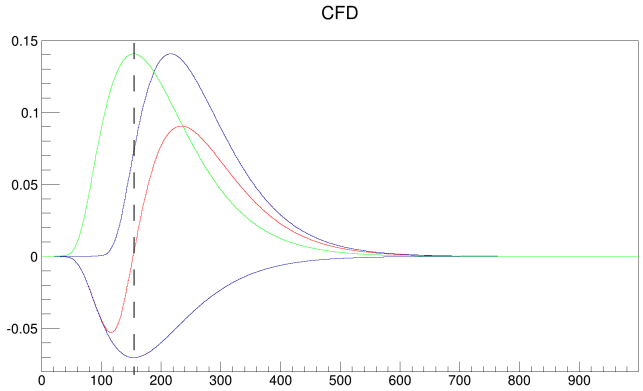


TOT → # clock cycles → Look Up Table (LUT) → T1
Compare T1 from LUT to real T1 of the signal

4

ULB

Constant Fraction Discriminator



The zero crossing and the signal maximum occur at the same time.

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Comparison of TOT (Time Over Threshold) and CFD (Constant Fraction Discriminator) techniques:

Goal : Allow long shaping times to boost S/N by reducing ballistic deficit and at the same time retain good timing resolution.

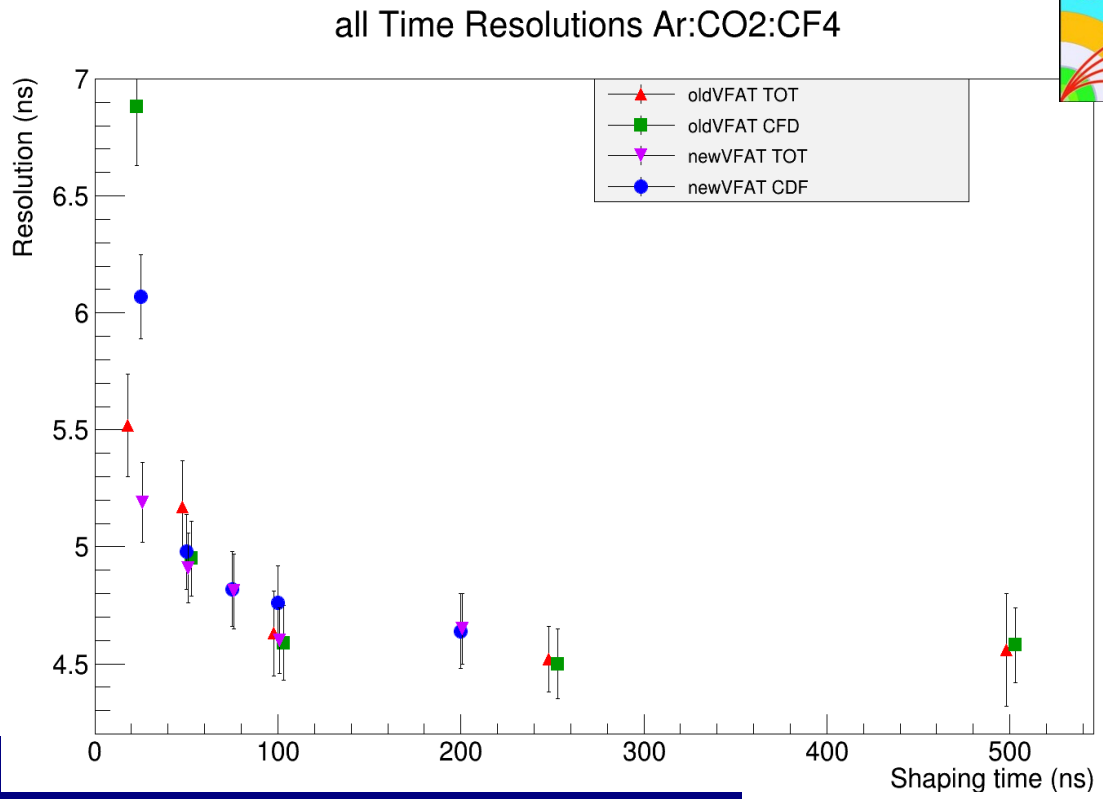
TOT maintains timing resolution by correcting time walk through a LUT (look up table).

CFD corrects time walk internally in the comparator.

T.Maerschalk, ULB

Recovering Timing Resolution in VFAT3 TOT and CFD

ULB



Old VFAT3

Shaping time (ns)	20	50	100	250	500
Resolution TOT (ns)	5.52 +/- 0.22	5.17 +/- 0.2	4.63 +/- 0.18	4.52 +/- 0.14	4.56 +/- 0.24
Resolution CFD (ns)	6.88 +/- 0.25	4.95 +/- 0.16	4.59 +/- 0.16	4.50 +/- 0.15	4.58 +/- 0.16

New VFAT3

Shaping time (ns)	25	50	75	100	200
Resolution TOT (ns)	5.19 +/- 0.17	4.91 +/- 0.15	4.81 +/- 0.16	4.60 +/- 0.14	4.65 +/- 0.15
Resolution CFD (ns)	6.07 +/- 0.18	4.98 +/- 0.16	4.82 +/- 0.16	4.76 +/- 0.16	4.64 +/- 0.16

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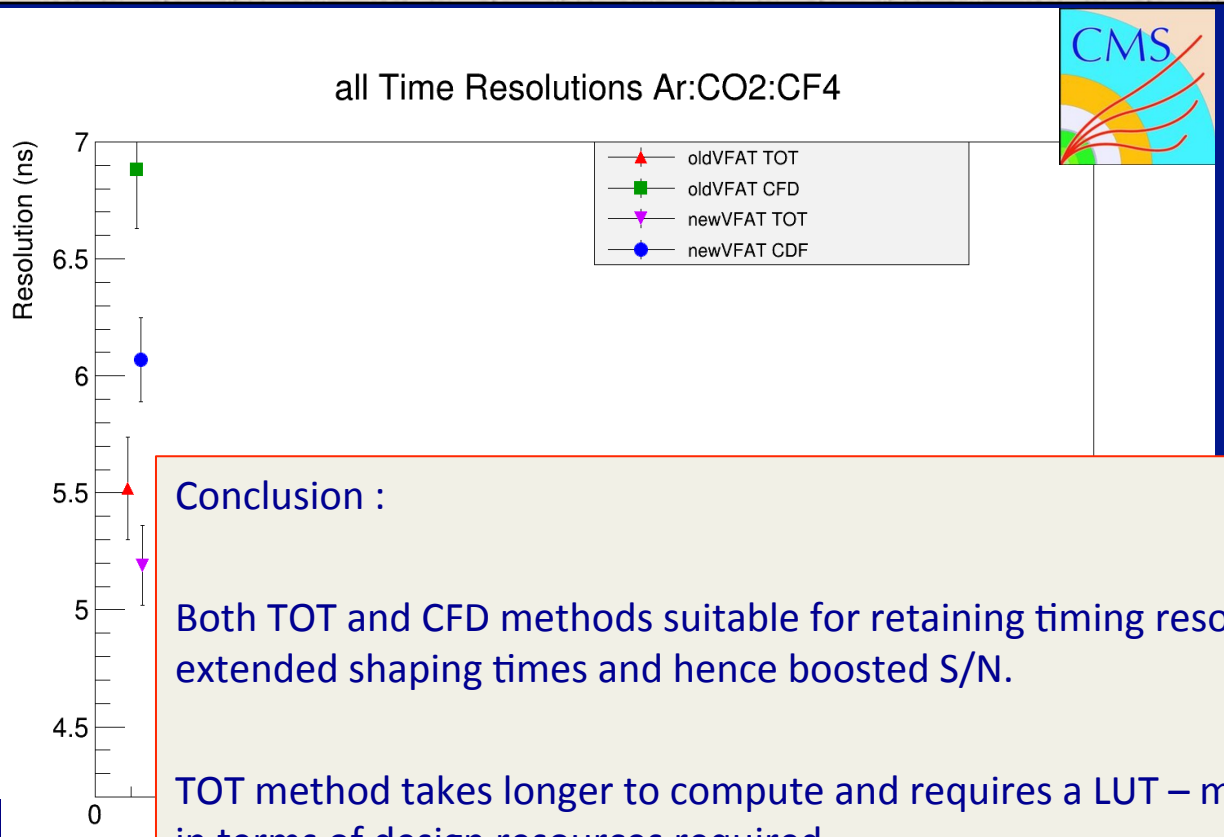
T.Maerschalk, ULB

Recovering Timing Resolution in VFAT3 TOT and CFD

ULB



CMS

Old VFAT3

Shaping time (ns)	20	
Resolution TOT (ns)	5.52 +/- 0.22	5.1
Resolution CFD (ns)	6.88 +/- 0.25	4.95

New VFAT3

Shaping time (ns)	25	
Resolution TOT (ns)	5.19 +/- 0.17	4.91
Resolution CFD (ns)	6.07 +/- 0.18	4.98

Conclusion :

Both TOT and CFD methods suitable for retaining timing resolution with extended shaping times and hence boosted S/N.

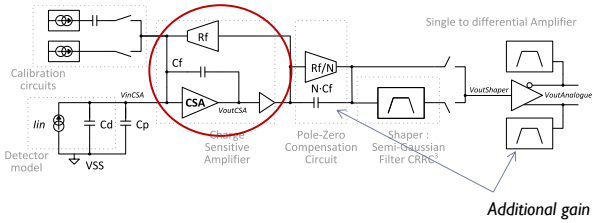
TOT method takes longer to compute and requires a LUT – more expensive in terms of design resources required.

CFD is the most efficient in terms of design resources.

CFD chosen for VFAT3 design.

Analog front-end

Front End electronics



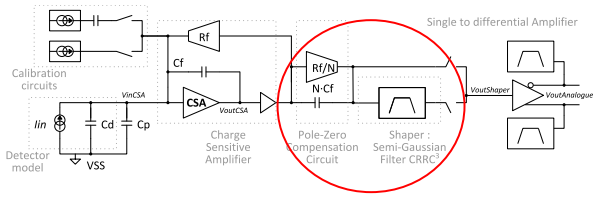
- Feedback capacitor

Cf	CSA Theoretical gain
100 fF	10 mV/fC
200 fF	5 mV/fC
400 fF	2.5 mV/fC
800 fF	1.25 mV/fC

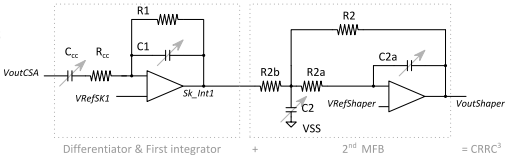
- CSA
  - Power consumption ~ 800µW @1.5V
  - 4 options for CFE. Typical performance with an ideal CRRC³ shaper :

CSA	Cdet	Tpeak	Phase margin	Gain	BW	GBW	Noise
1	30 pF	100 ns	90°	60 dB	1.8 MHz	816 MHz	918 e^-
2	30 pF	100 ns	85°	60 dB	2.4 MHz	786 MHz	764 e^-
3	30 pF	100 ns	78°	79.5 dB	0.3 MHz	787 MHz	840 e^-
4	30 pF	100 ns	85°	75 dB	0.3 MHz	807 MHz	1031 e^-

Front End electronics



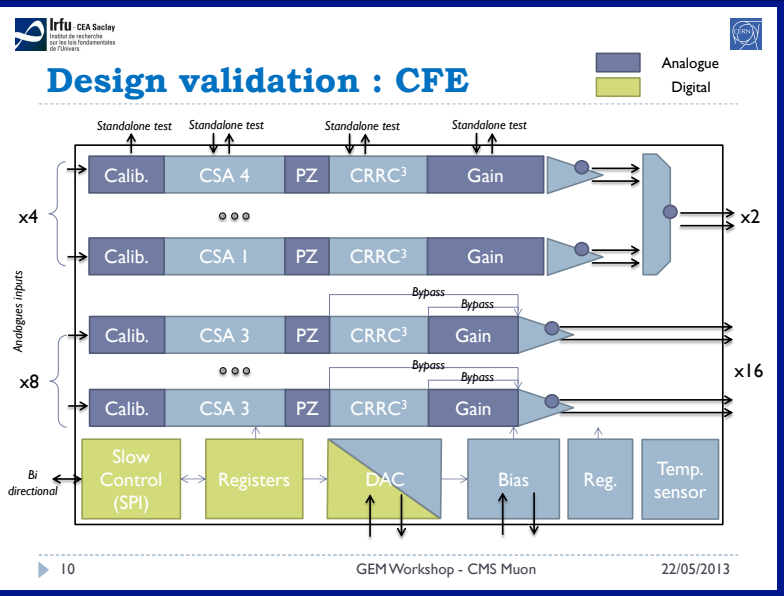
- Shaper CRRC / CRRC² / CRRC³
  - Programmable Tp
  - Programmable DC output
  - Power consumption : ~ 1.2 mW (programmable)



Key Parameter	Comment
detector charge polarity	Positive and Negative
Detectore capacitance range	5 - 80pF
Peaking Times (Tp)	25, 50, 75, 100, 200 ns
Programmable gain	1.25 to 50 mV/fC
Max Dynamic Range (DR)	Up to 200 fC
Linearity	< 1% of DR
Power Consumption	2mW/ch
Power Supply	1.5V
ENC	$\approx 1100e\ (with Tp = 100ns, Cd = 30pF)$
Technology	IBM 130nm

F. Guilloux, CEA Saclay

FE & CFD test chips



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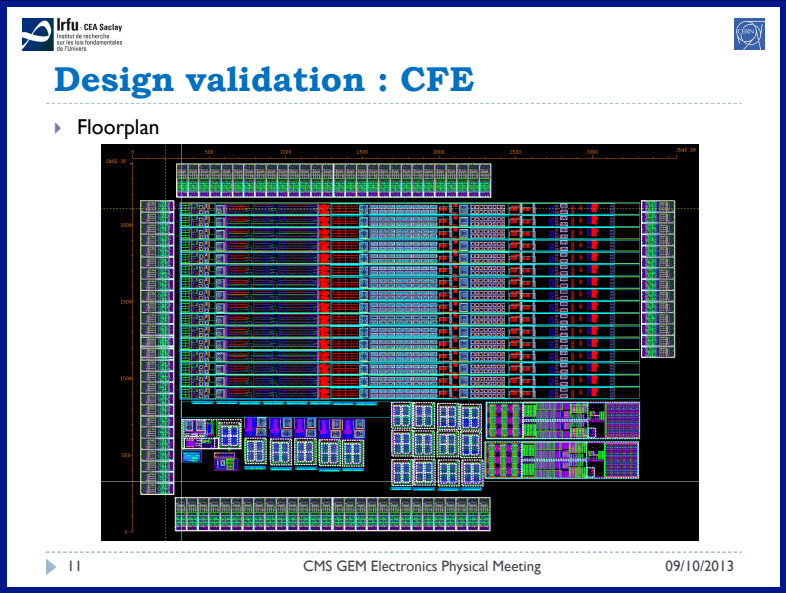
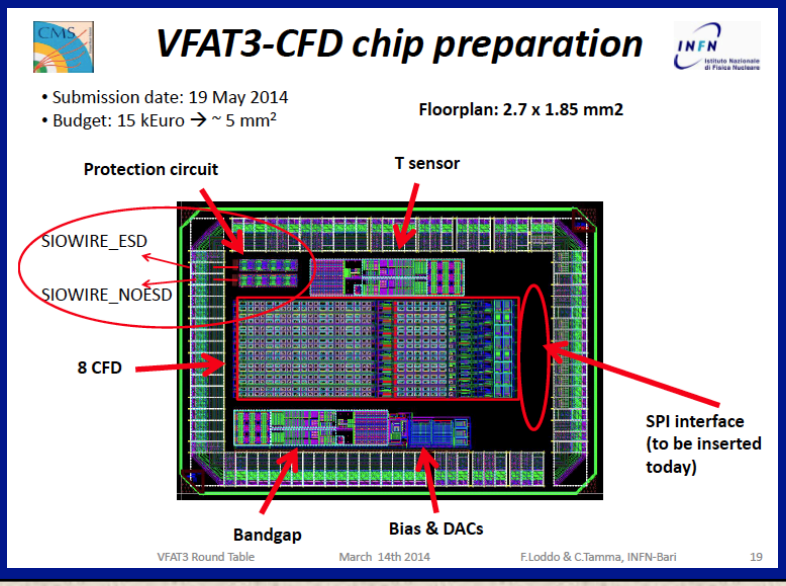
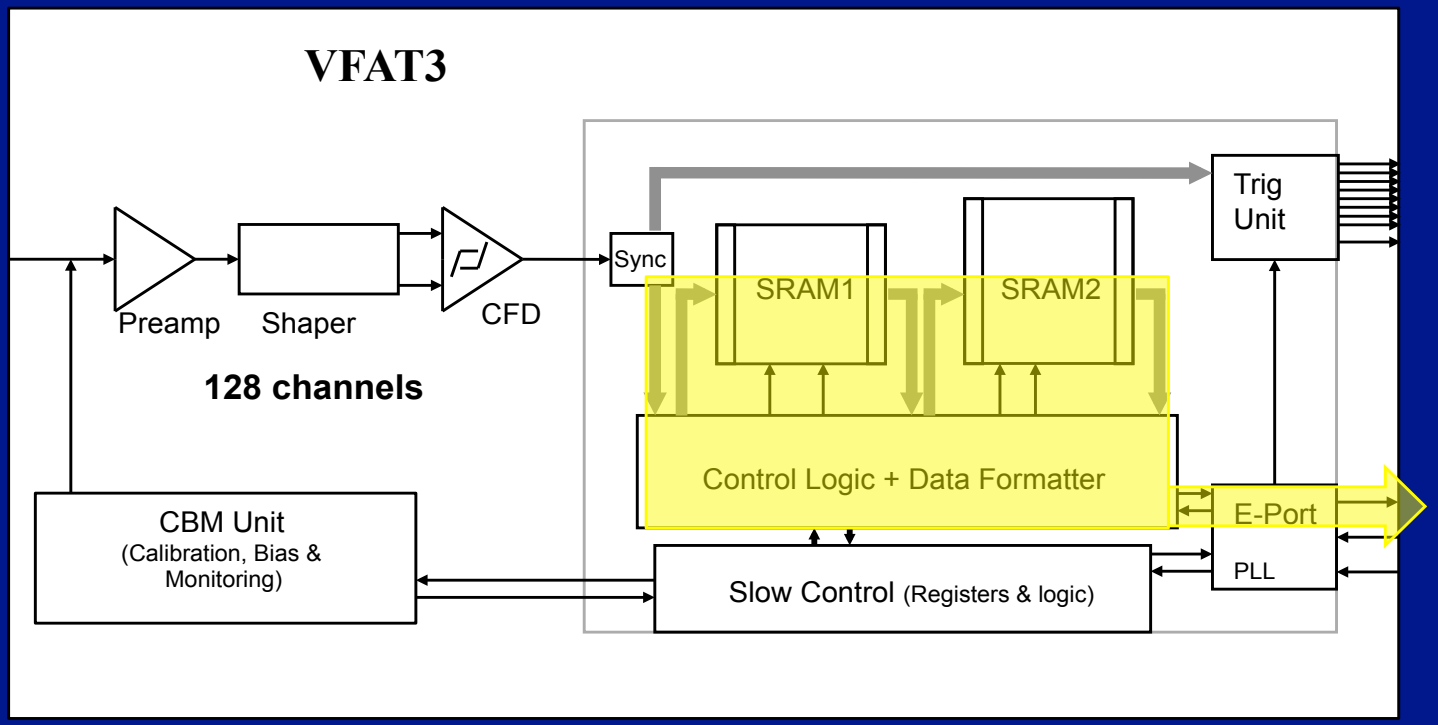


FE and CFD test chips planned for May 2014 submission

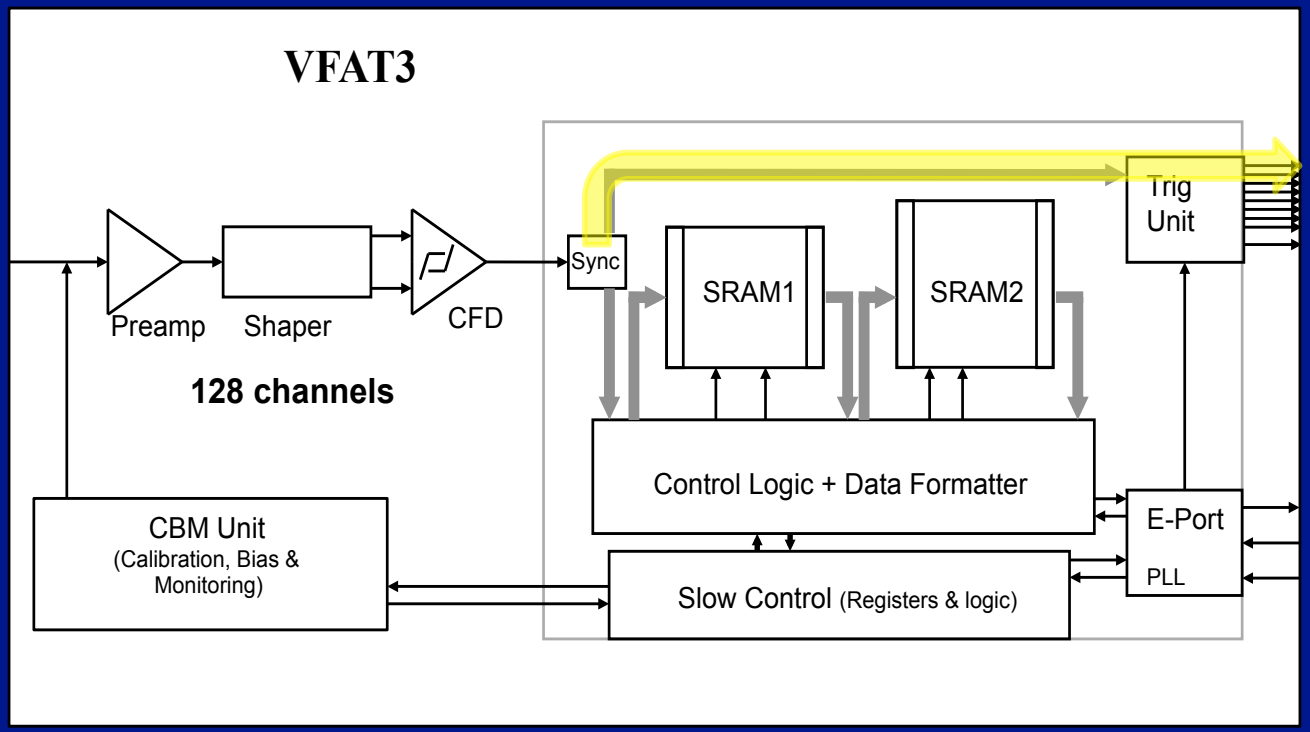


F. Loddo, C.Tamma , INFN Bari

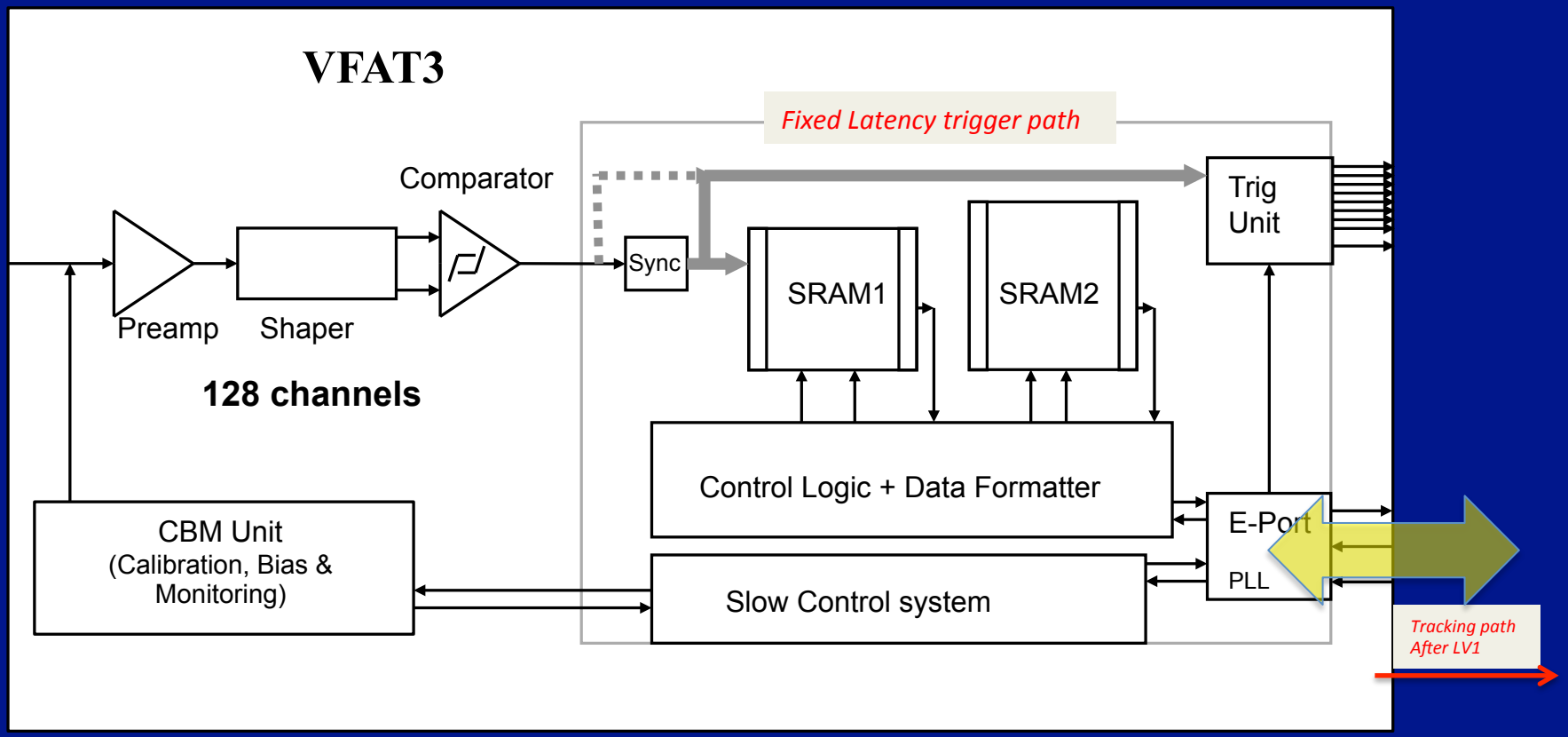
The Variable Latency Data Path



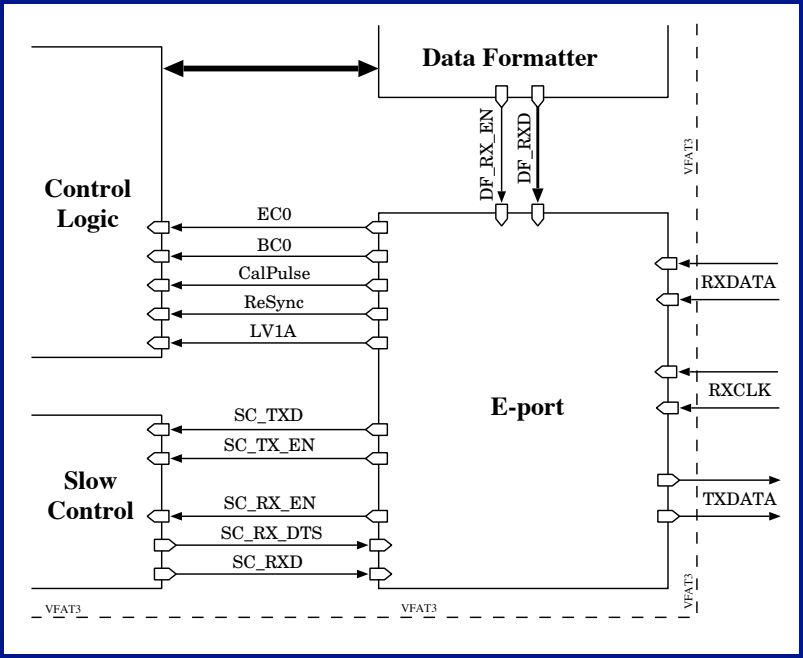
The Fixed Latency Trigger Path



VFAT3 Communication



E-Port ....



Name	4-bit word	8-bit representations	Disp.
A	0000	xxxxxxxx	0
		xxxxxxxx	0
B	0001	xxxxxxxx	0
		xxxxxxxx	0
C	0010	xxxxxxxx	0
		xxxxxxxx	0
D	0011	xxxxxxxx	0
		xxxxxxxx	0
E	0100	xxxxxxxx	0
		xxxxxxxx	0
F	0101	xxxxxxxx	0
		xxxxxxxx	0
G	0110	xxxxxxxx	0
		xxxxxxxx	0
H	0111	xxxxxxxx	0
		xxxxxxxx	0
I	1000	xxxxxxxx	0
		xxxxxxxx	0
J	1001	xxxxxxxx	0
		xxxxxxxx	0
K	1010	xxxxxxxx	0
		xxxxxxxx	0
L	1011	xxxxxxxx	0
		xxxxxxxx	0
M	1100	xxxxxxxx	0
		xxxxxxxx	0
N	1101	xxxxxxxx	0
		xxxxxxxx	0
O	1110	xxxxxxxx	0
		xxxxxxxx	0
P	1111	xxxxxxxx	0
		xxxxxxxx	0

8 bit Control codes.
Each code is allocated a dedicated function

FSCC	Character	Description
EC0	A	Reset the Event Counter.
BC0	B	Reset the Bunch-Crossing-Zero Counter.
CalPulse	C	Injection of CalPulse.
ReSync	D	Resets all state machines in CL and DF.
SCOnly	E	Force "Slow Control Only" Mode.
Run Mode	F	Return from "Slow Control Only" Mode.
LV1A	G	First Level Trigger.
SC0	H	Sends "0" to the Slow Control.
SC1	I	Sends "1" to the Slow Control.

All communication with VFAT3 passes through the E-port.
The functions provided by the E-Port include :

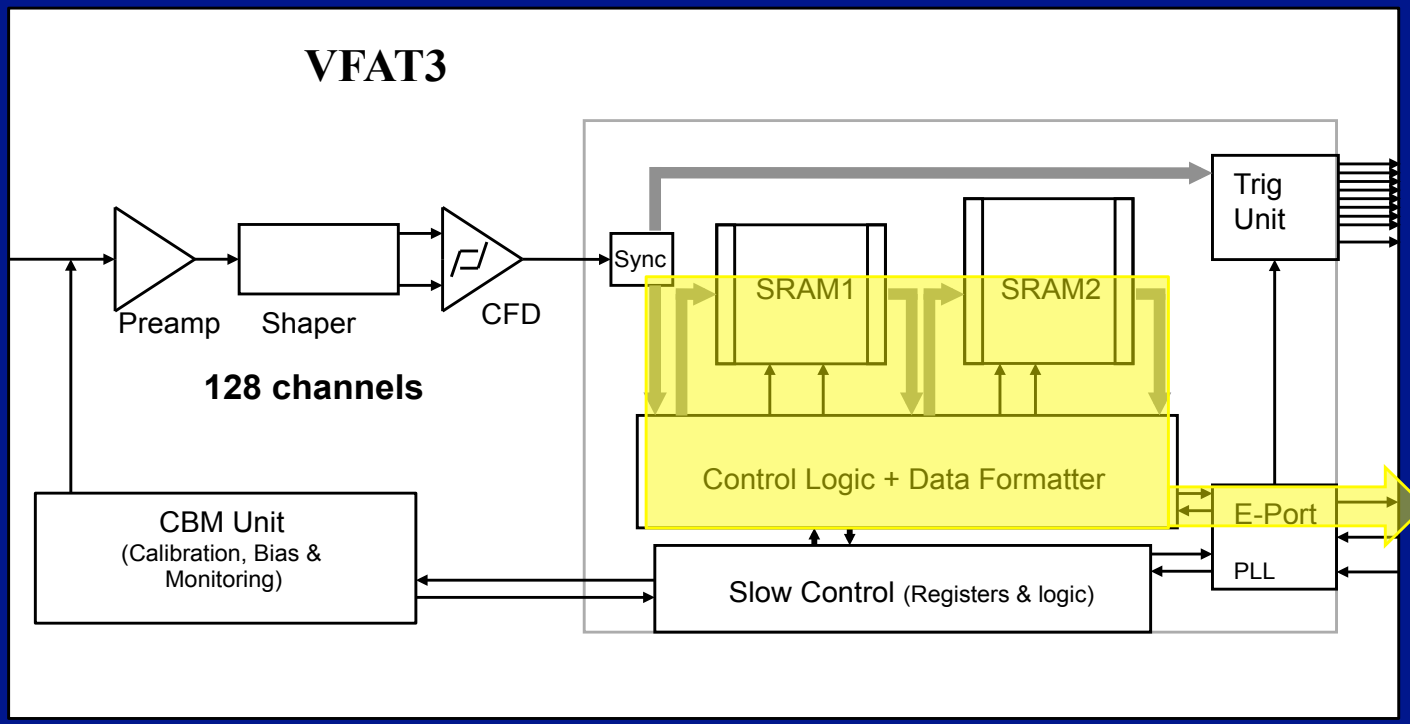
- Synchronisation (40MHz) & phase adjustment
- Reception of Control Commands via Control Codes
- Reception of Slow Control commands via Control Codes (SC0, SC1), *(IPbus wrapped in HDLC)*

- Transmission of data packets
- Transmission of Slow Control data packets
- Transmission of Error warnings

M. Dabrowski (CERN)

Slow Control : G.DeRobertis (INFN Bari)

The Variable Latency Data Path



Data packet path

Online:

VFAT3 DP should contain minimum amount of data possible to optimise bandwidth.

Can be zero suppressed or not

Offline :

DAQ DP must contain all information relating to :

Chip ID (location within the whole detector)
Event number
Channels hit.

Note on zero suppression:
If VFAT3 DP contains zero suppression then packets will arrive at the uTCA "out of order" with respect to other VFATs in the system however they will remain consecutive for each individual VFAT.

VFAT3 has 2 different options for the Data Packet "Lossless" and "SPZPS"

Data Packets : Lossless & SPZS

Single Time Slot Per Event *(if **TSPE** register is equal to 00)*

Data Packets

Lossless

Registers DT	SZP	SZD	Data Packet	No. Bits	Comment
0	0	0	Header I	8	***Basic data packet***
			EC+BC / EC / BC	8 - 48	*Size depends on **TT, Ecb, BCb***
			Data	128	
			CRC	16	
0	0	1	Header I	8	***Basic data packet***
			EC+BC / EC / BC	8 - 48	*Size depends on **TT, Ecb, BCb***
			Data	128	
			CRC	16	
			Header II	8	***Zero Suppressed***
			EC	8 - 24	*Size depends on **Ecb***
			CRC	16	
0	1	x	Header I	8	***Basic data packet***
			EC+BC / EC / BC	8 - 48	*Size depends on **TT, Ecb, BCb***
			Data	128	
			CRC	16	
			Header II	8	***Zero Suppressed***

Sequential Partial Zero Suppression

Registers DT	SZP	SZD	Data Packet	No. Bits	Comment
1	0	0	Header I	8	***Basic SPZS data packet***
			EC+BC / EC / BC	8 - 48	*Size depends on **Partitions/P16***
			Data	16 - 96	
			CRC	16	
1	0	1	Header I	8	***Basic SPZS data packet***
			EC+BC / EC / BC	8 - 48	*Size depends on **TT, Ecb, BCb***
			Data	16 - 96	*Size depends on **Partitions/P16***
			CRC	16	
			Header II	8	***Zero Suppressed***
			EC	8 - 24	*Size depends on **Ecb***
			CRC	16	
1	1	x	Header I	8	***Basic SPZS data packet***
			EC+BC / EC / BC	8 - 48	*Size depends on **TT, Ecb, BCb***
			Data	16 - 96	*Size depends on **Partitions/P16***
			CRC	16	
			Header II	8	***Zero Suppressed***

Relevant registers

ECb	Size(EC)	
00	8	*default*
01	16	
10	24	
11	*(8)*	

BCb	Size(BC)	
0	16	*default*
1	24	

TT	EC+BC / EC / BC	
00	EC + BC	*default*
01	EC	
10	BC	
11	*(EC + BC)*	

Partitions	No. Partitions
0000	1
0001	2
0010	3
0011	4
0100	5
0101	6
0110	7
0111	8
1000	9
1001	10
1010	11
1011	12
1100	13
1101	14
1110	15
1111	16

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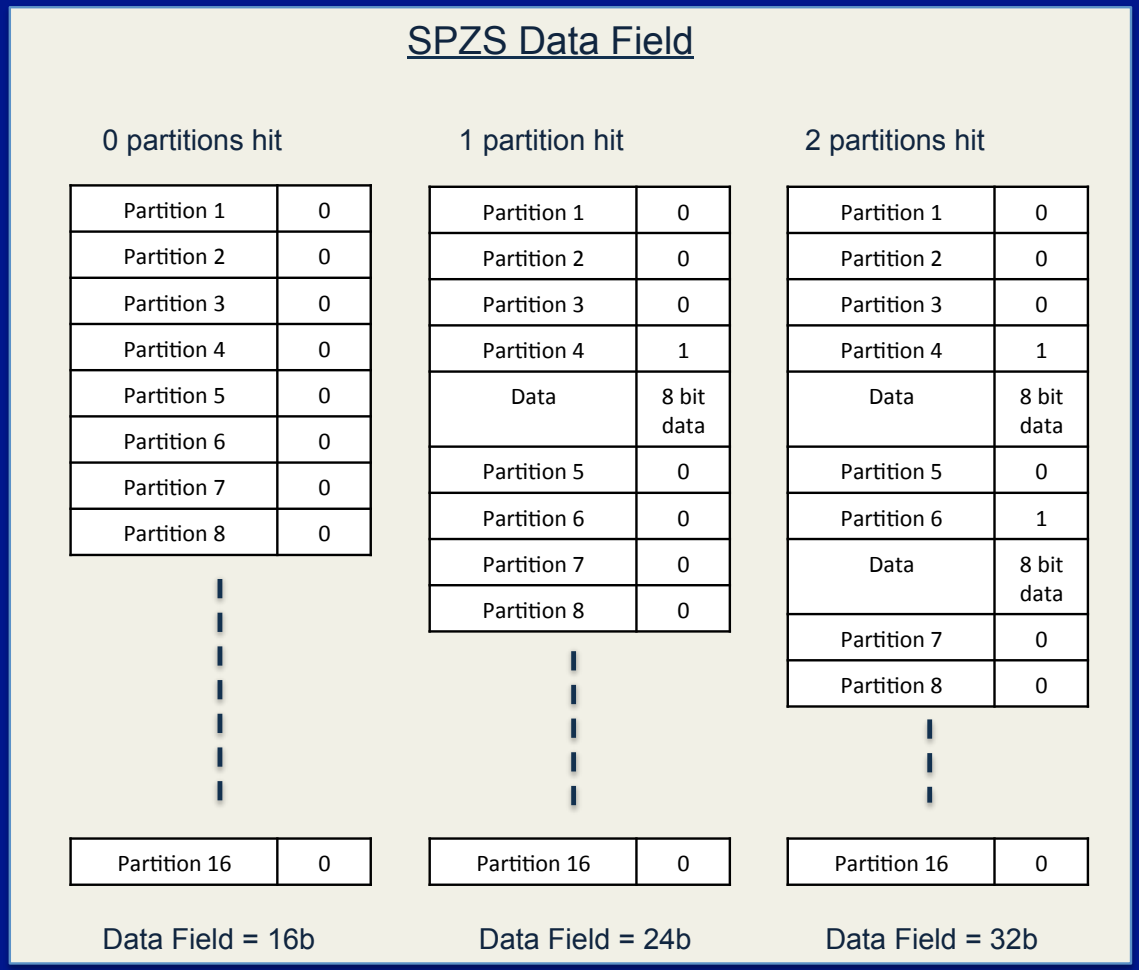
P16	Comment	
0	Send numbers of partitions accodring to **Partitions** register	*default*
1	Send only high level information (16bit)	

Highly programmable to optimise the data packet content depending on occupancy and trigger rate.

Multiple time slots per event can be obtained by the DAQ sending multiple successive VFAT triggers per one CMS LV1A accept. House keeping in the DAQ would be needed to keep track of VFAT3 EC values and the real CMS EC values.

"Sequential" Partition Zero Suppression (SPZS)
(a variation on the CMS RPC data format)



16 Partitions, 8 channels / partition

16 bits total for partition identification

8 bits per partition

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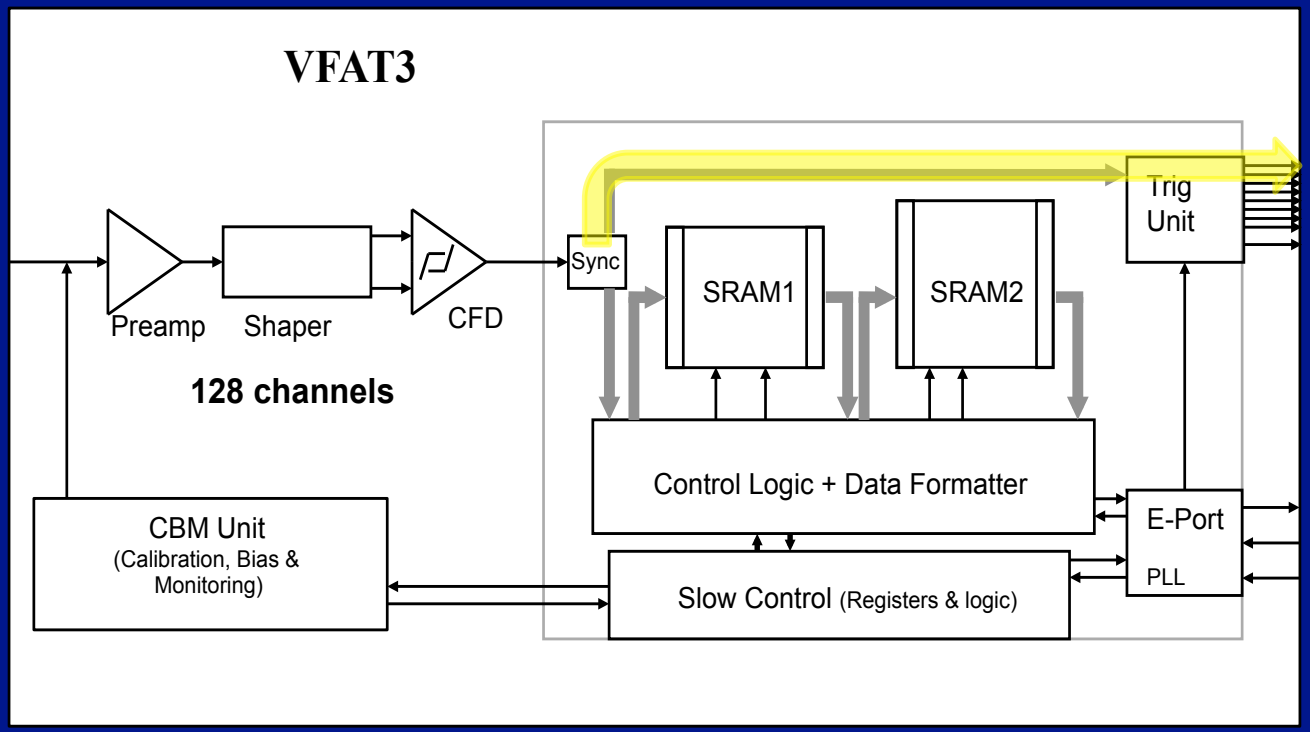
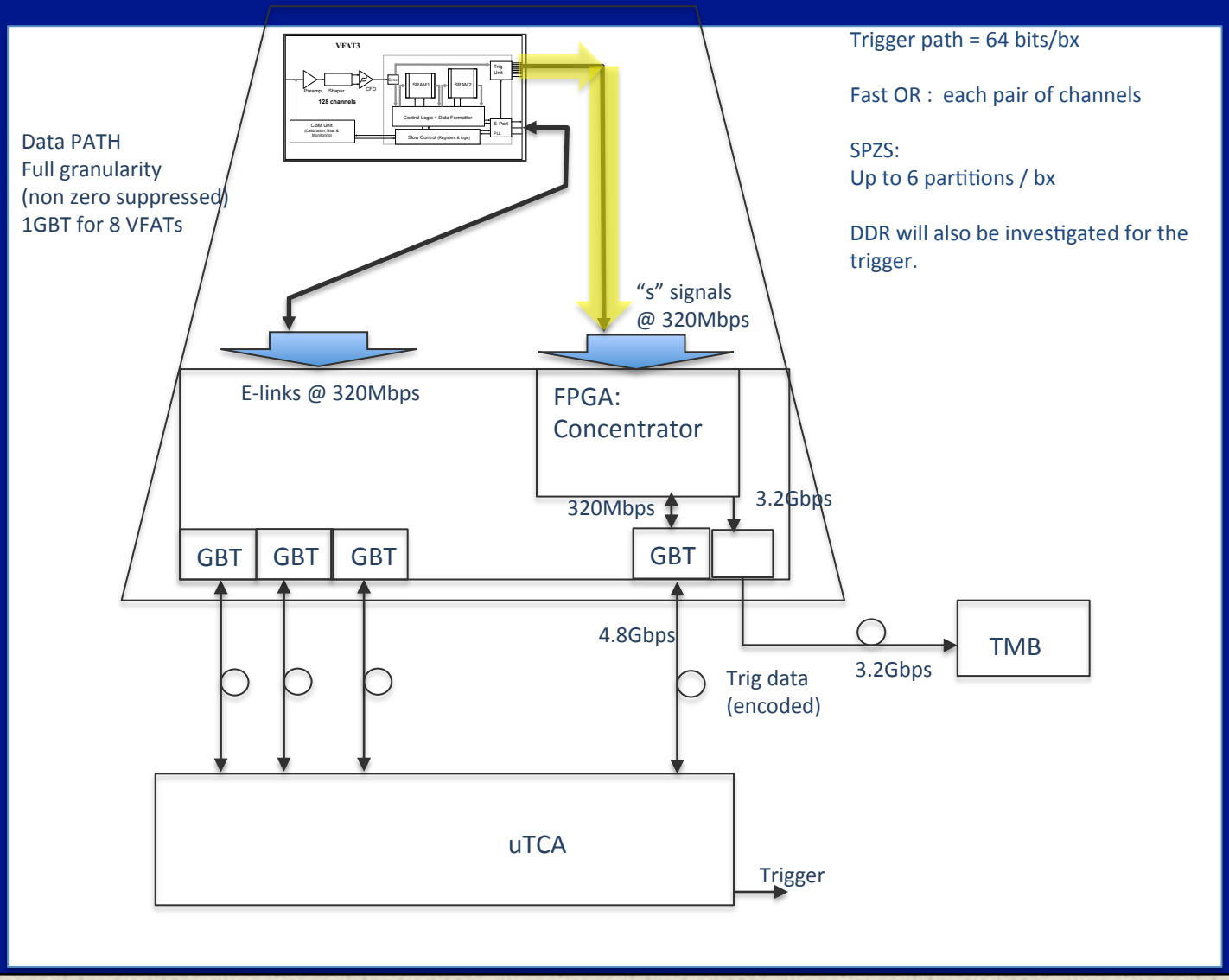
The Fixed Latency Trigger Path



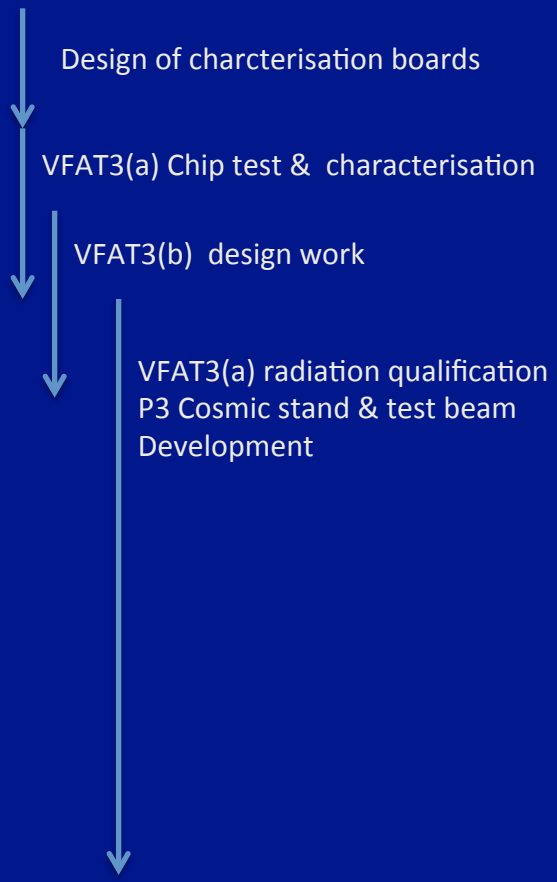
Trigger Path Data options



VFAT3 Submission Schedule & Goals

VFAT3 steps in yearly quarters

Q1 2015	Submission of VFAT3 in IBM130nm
Q2 2015	Return of VFAT3 from foundry
Q3 2015	Ist test results
Q4 2015	Release of VFAT3(a) if possible.
Q1 2016	2nd Submission of VFAT3(b) if necessary
Q2 2016	Return of VFAT3b from foundry
Q3 2016	Ist test results (b)
Q4 2016	Release of VFAT3(b)



Schedule risk factors:

Process: IBM 130nm. We are considering moving the design to TSMC 130nm or 65nm in which case the schedule would be affected.

Manpower : The chip is being designed largely by short term students. Relies on their contracts being extended.

Thanks