ATLAS Muon Trigger for HL-LHC

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Introduction

- Proposed ATLAS Phase-II hardware trigger
  - Level-0 trigger with 500 kHz and 6 μs latency.
  - Level-1 trigger with 200 kHz and 20 μs latency.

- Concept of the ATLAS Phase-II muon trigger
  - Keep Level-1 muon p_T threshold of 20 GeV for retaining acceptance for various physics processes.
  - Trigger logic based on the trigger chambers (RPCs and TGCs) remains at Level 0. Electronics modified.
  - Additional constraint based on precision tracking chambers (MDTs) at Level 0 or Level 1 proposed.

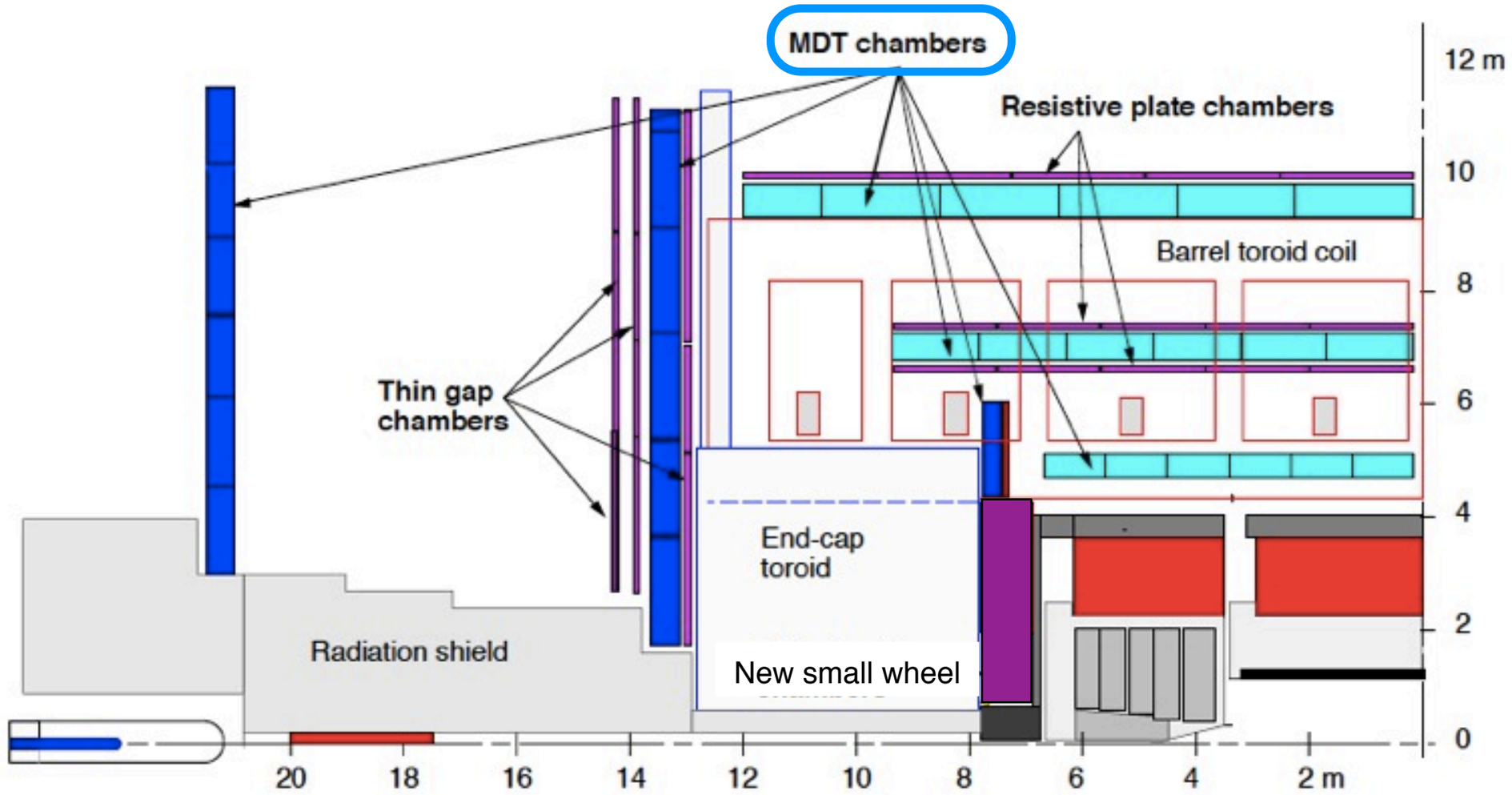
Contents of this presentation

1. MDT-based Level-0/1 muon trigger
   - Performance estimation with method overview
   - Proposed schema of electronics
2. Barrel Level-0 muon trigger
   - Proposed scheme of electronics
3. Endcap Level-0 muon trigger
   - Proposed scheme of electronics

1. MDT-based Level-0/1 muon trigger

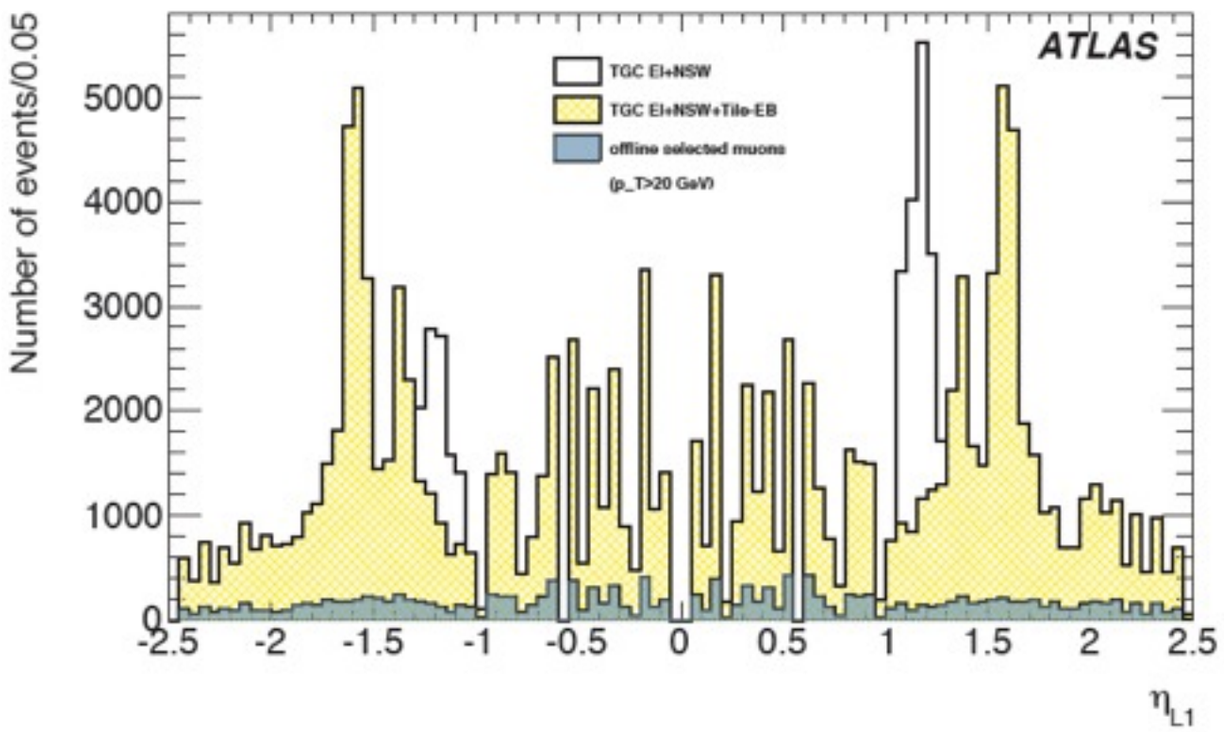
- Monitored Drift Tube ("MDT") for precision tracking.
- MDT-based trigger: candidate of the Phase-II Level-0/1 muon triggers. Exploit precision angular resolution.
- MDT covers a wide range in both barrel and endcaps.

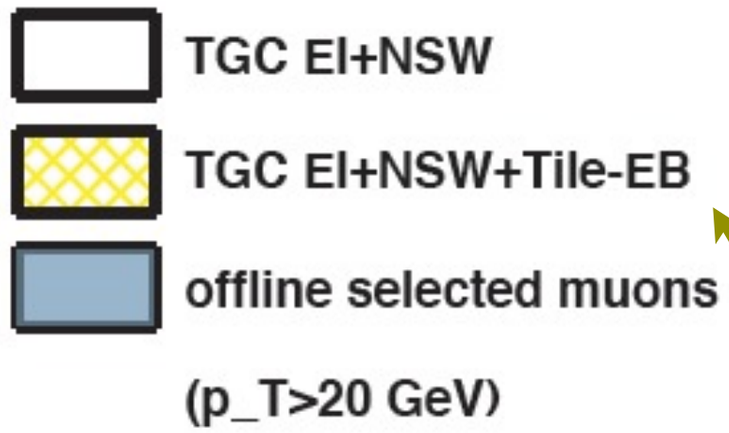
"Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment", CERN-2012-022.



Strategy for a performance estimation

Level-1 trigger rate after the Phase-I upgrade has been estimated in TDR for Phase-I upgrade of TDAQ [CERN-LHCC-2013-018].





Level-1 entries after Phase-I upgrade.

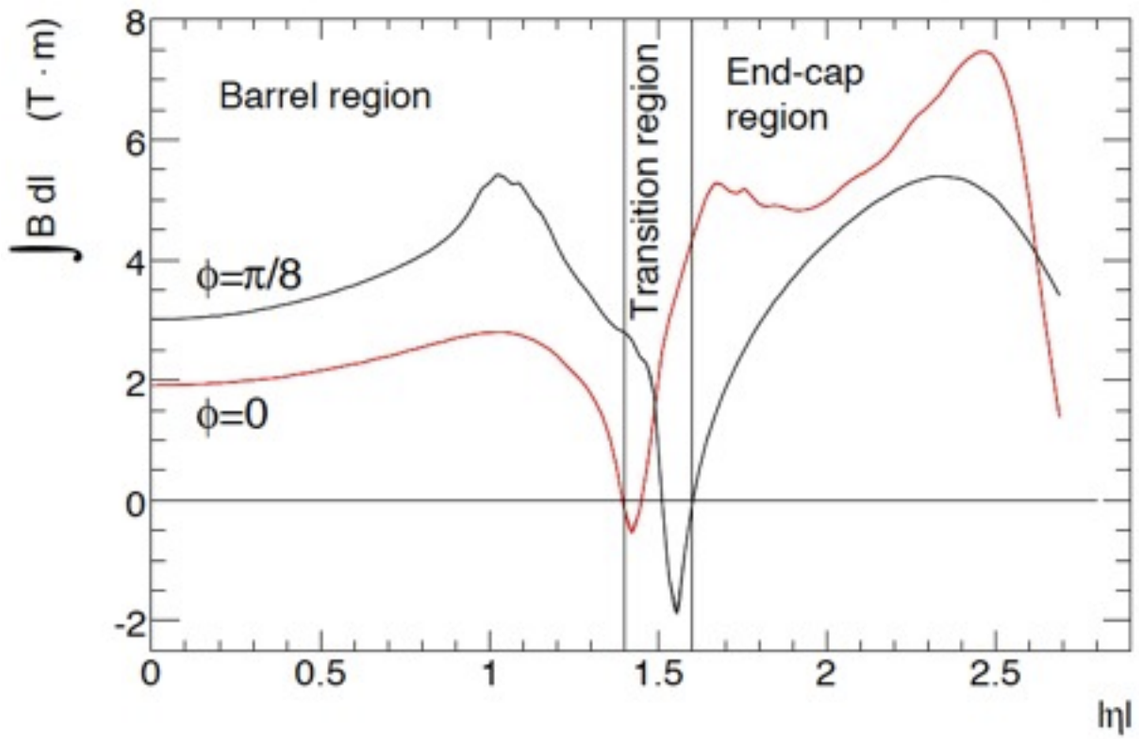
Using 2012 data, 8 TeV, 25 nsec.
No higher-level triggers applied.
No event filters applied.

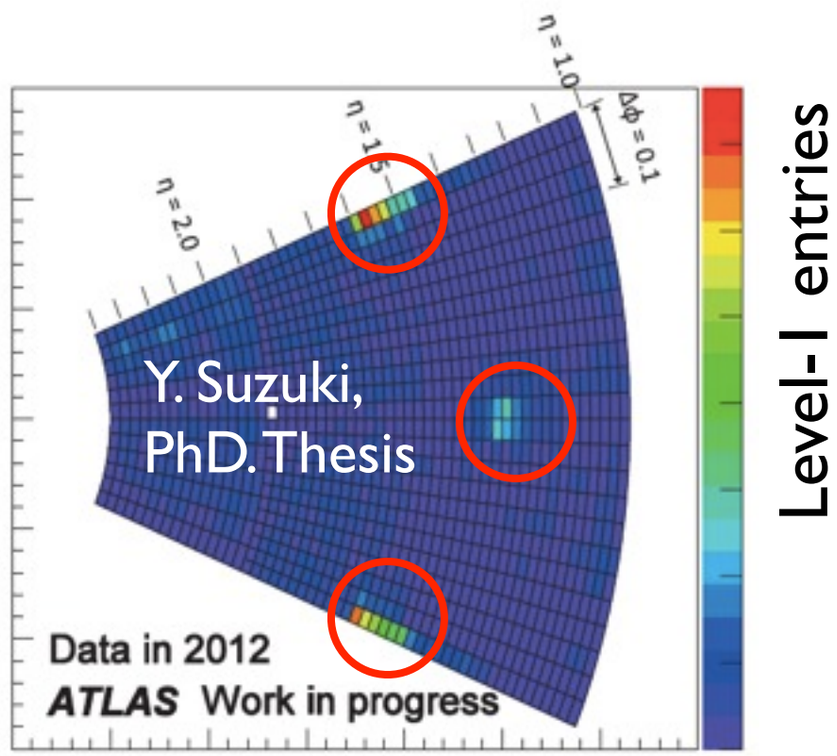
An MDT-based requirement is additionally applied for the Level-1 candidates which satisfy the requirements for the Phase-I upgrade.

Region mask

(Option for Phase-0/1 upgrades.)

Before including MDT-based requirement, we mask some regions in which the magnetic-field integral is small ("region mask").



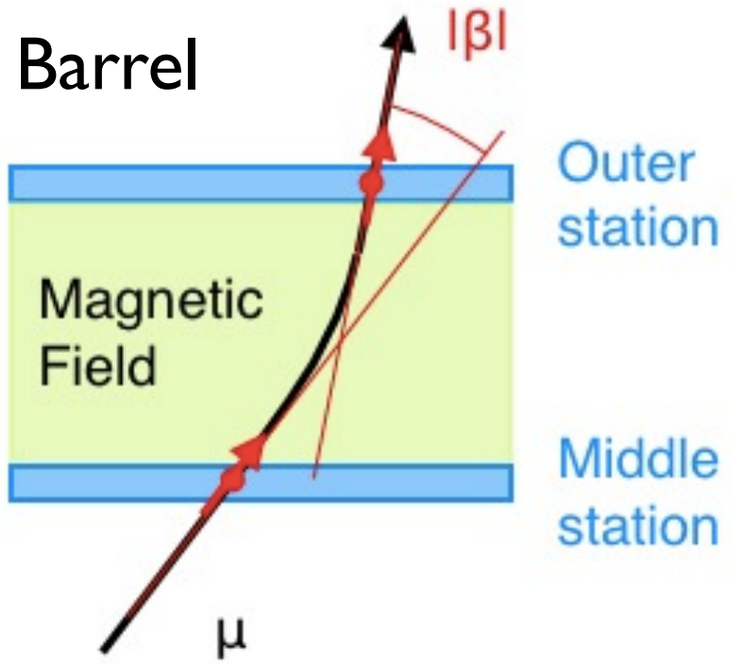


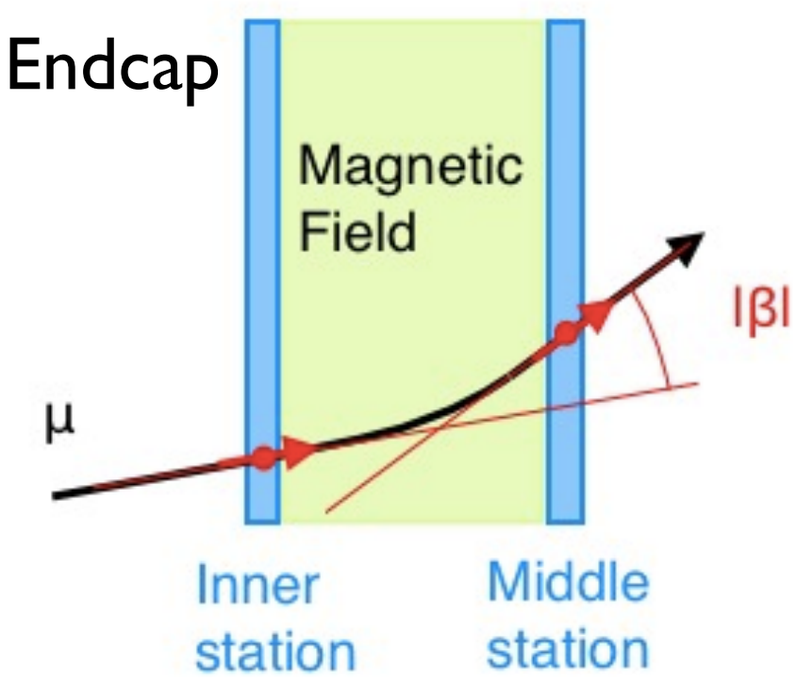
By introducing the region mask, Level-1 trigger rate is expected to reduce to about 90%, while an acceptance of 99% is retained.

Overview of an MDT-based requirement

Use a polar-angle difference β of the segments between:

- outer and middle stations in the barrel,
- middle and inner stations in the endcap.

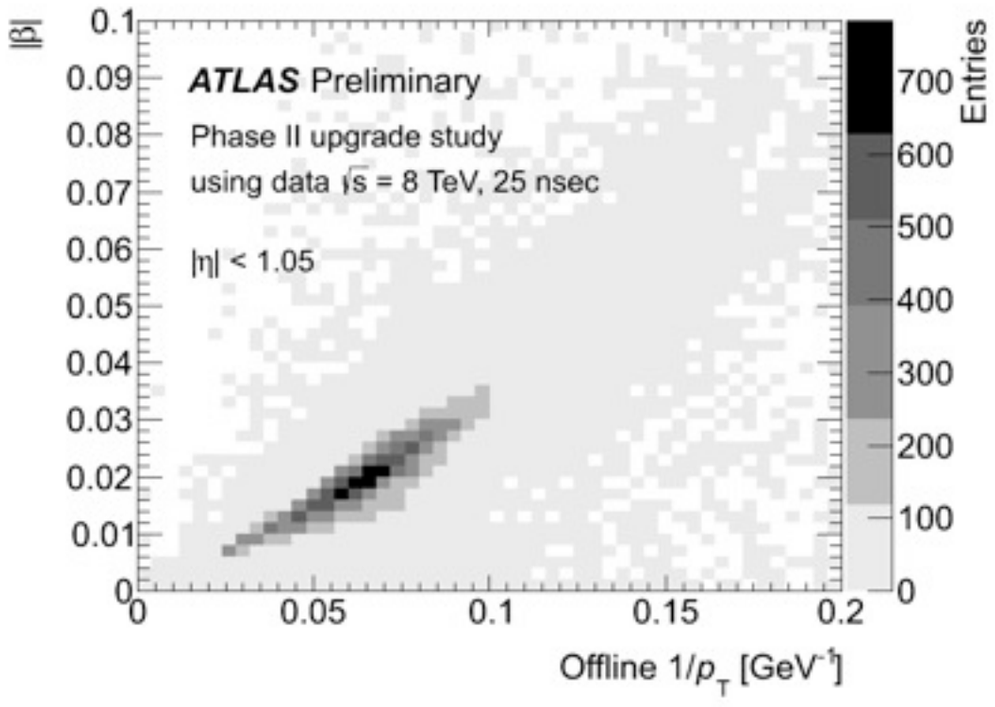




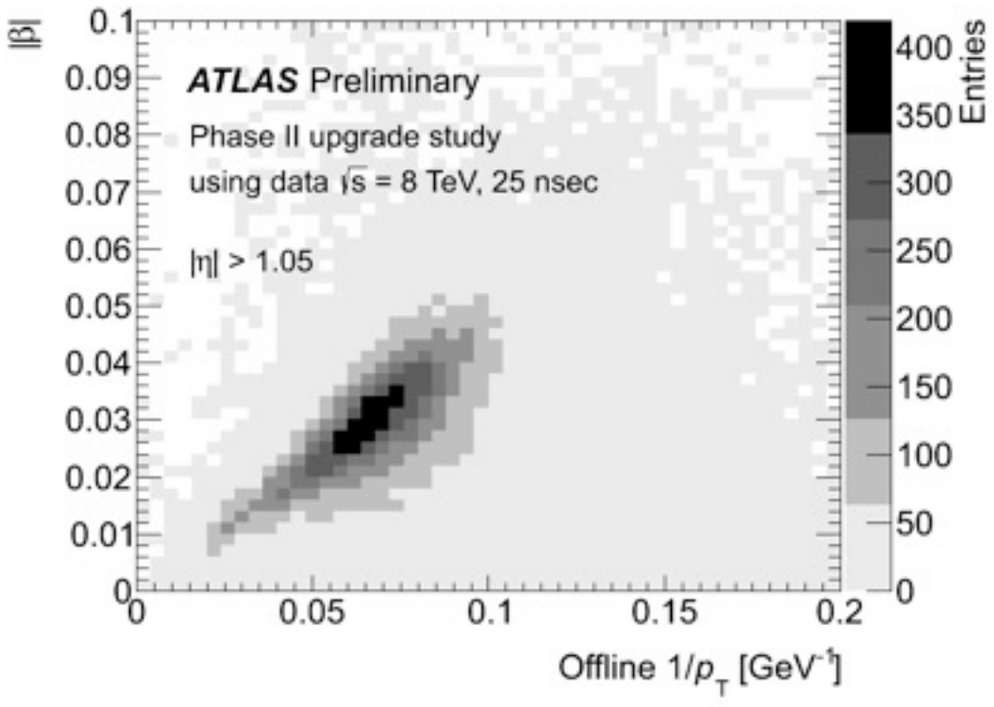
For estimating the performance, offline segments are selected in $\sqrt{(d\eta)^2+(d\varphi)^2} < 0.1$ from each Level-1 region of interest.
A combination is selected so that |β| becomes the smallest.

Level-1 muon candidates depending on |β| and $1/p_T$ after Phase-I requirements

Barrel (|η|<1.05)



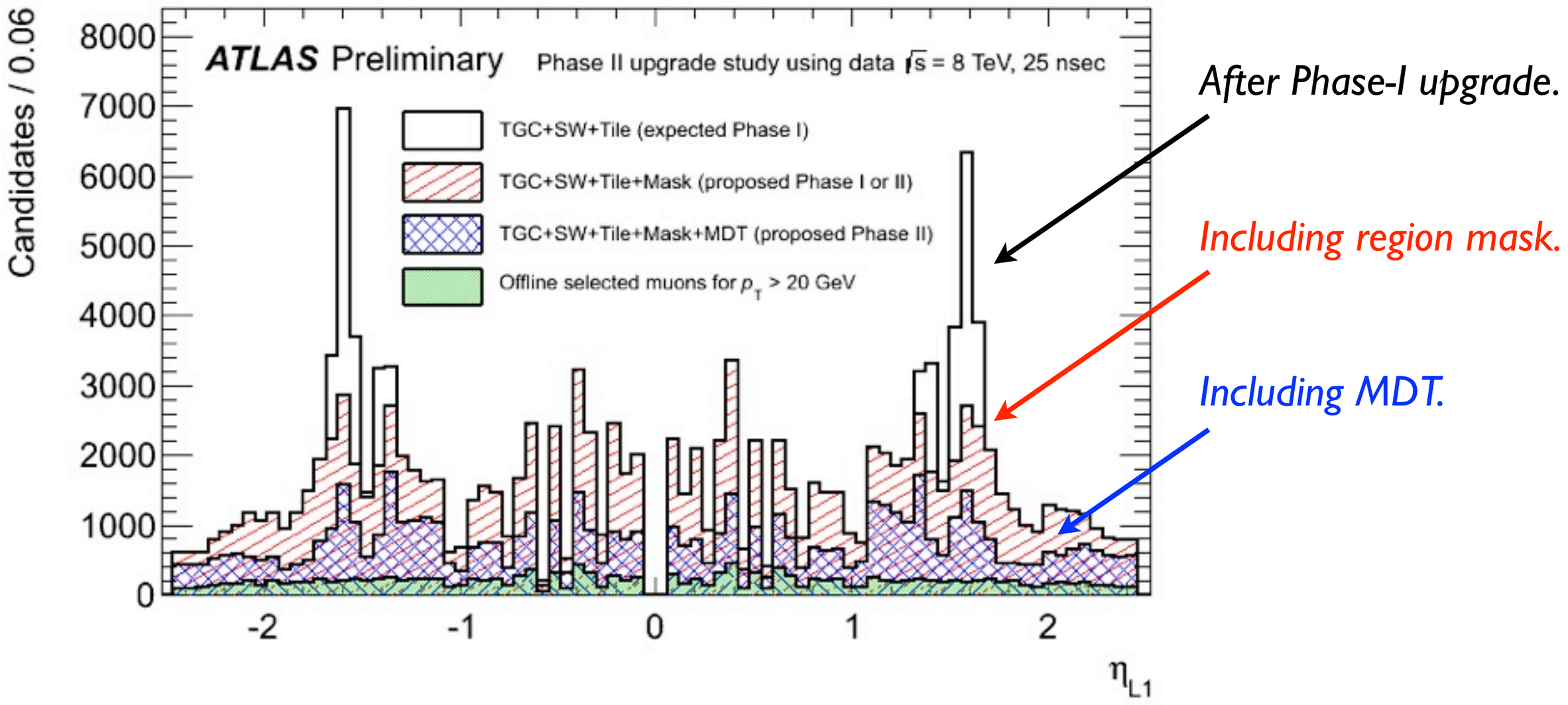
Endcap (|η|>1.05)



A large correlation between |β| and offline $1/p_T$ indicates a good separation of p_T region, e.g. p_T > 20 GeV, by a requirement on |β|.

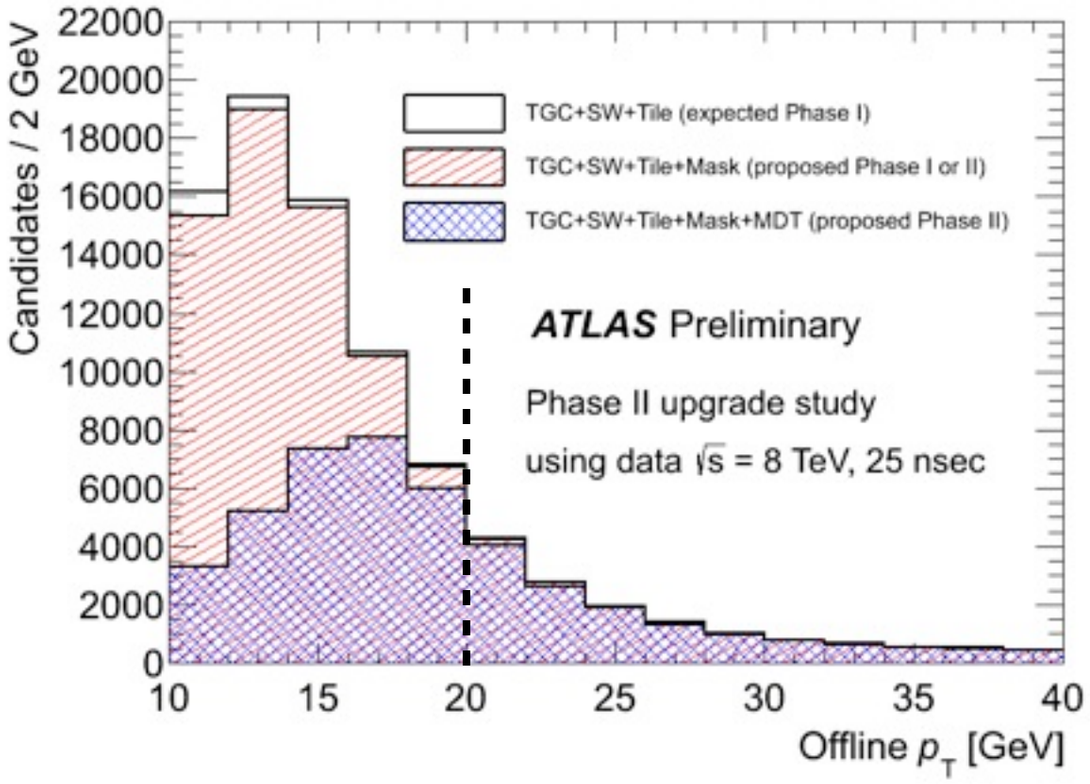
Requirement on |β| determined depending on the regions divided by η and φ (24 regions in total), so that the efficiency for the candidates with offline p_T > 20 GeV becomes > 95% in each region.

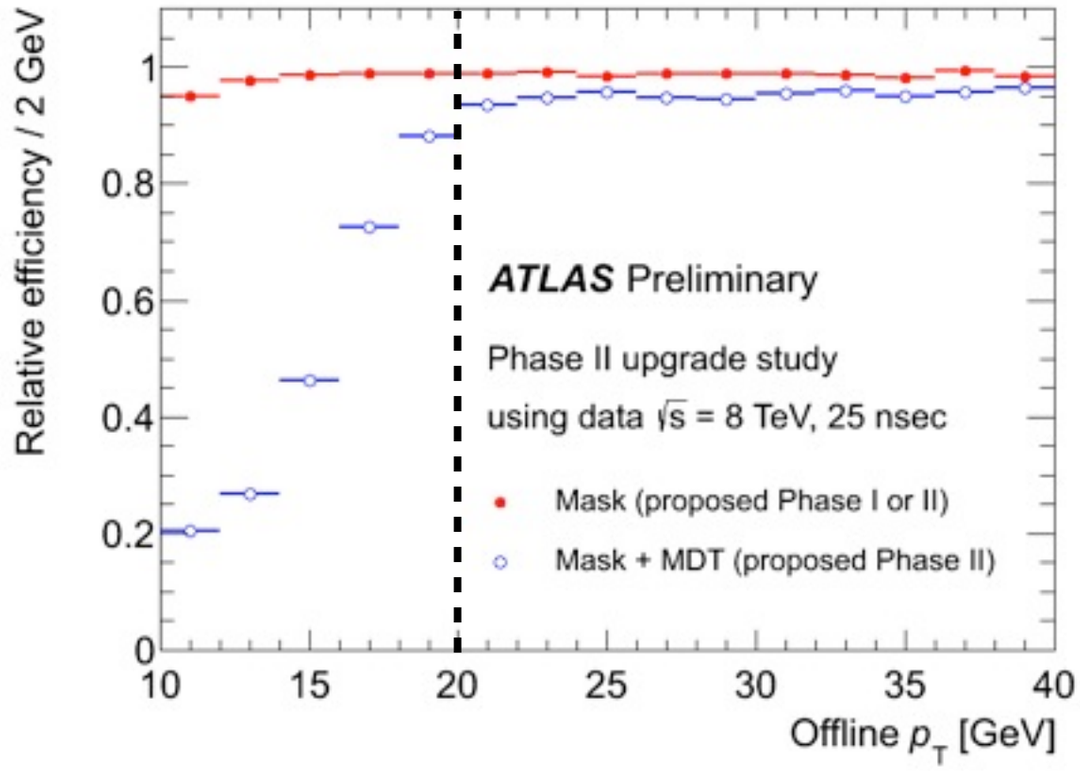
Level-1 muon candidates as a function of η



- Region mask rejects ~10% of the Level-1 candidates.
- MDT-based requirement rejects **~50%** of the Level-1 candidates.

Distributions of offline p_T and relative efficiency





White: after Phase-I upgrade.

Red: including region mask.

Blue: including MDT.

- Mask (proposed Phase I or II)
- Mask + MDT (proposed Phase II)

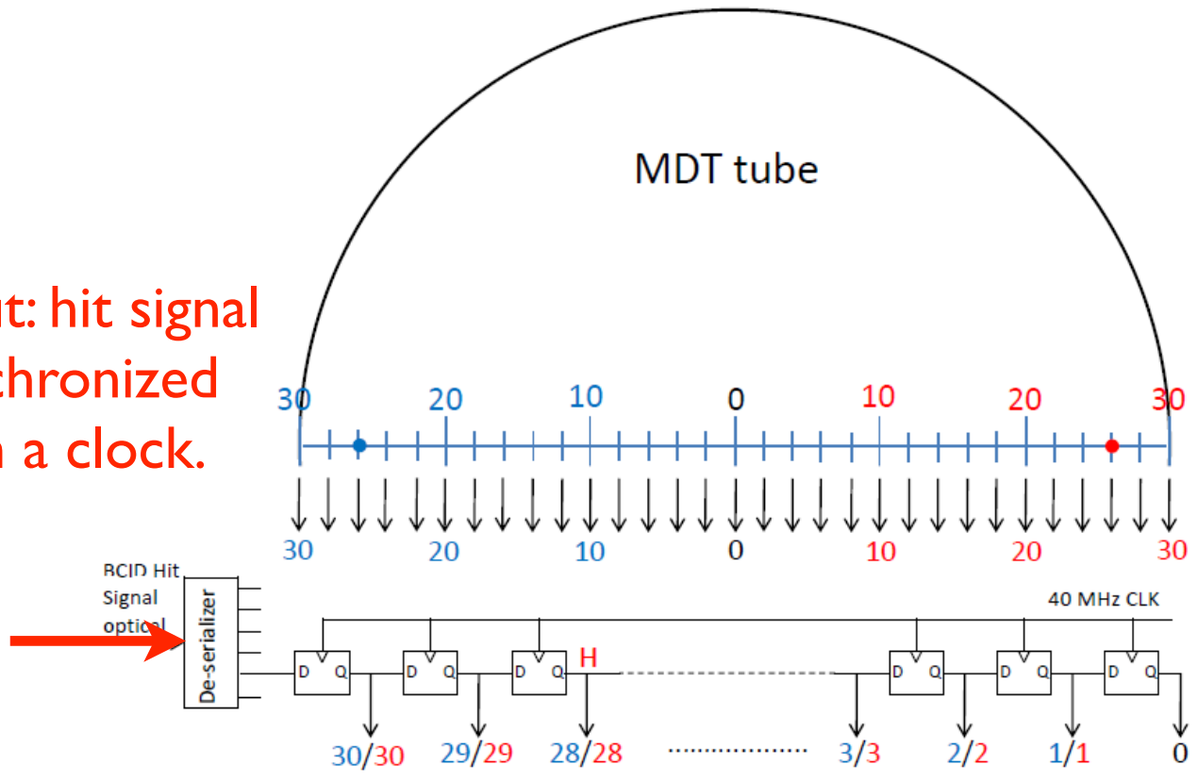
Candidates with offline p_T > 20 GeV well selected.

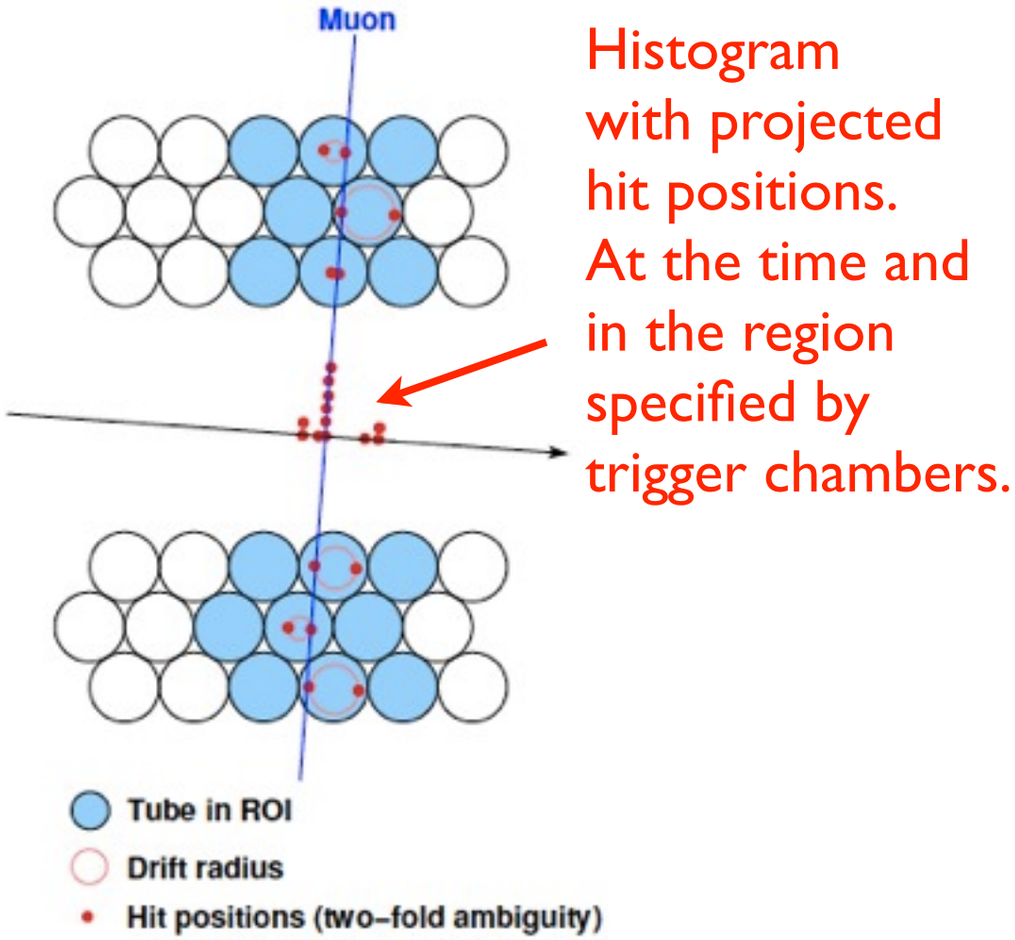
More explanation about this performance estimation:
https://twiki.cern.ch/twiki/bin/view/AtlasPublic/L1MuonTriggerPublicResults

Fast segment reconstruction

- At a Level-0/1 trigger level, full track information cannot be used.
- Algorithm at Level-0/1 based on shift registers or FIFO proposed; this method provides binary hit-time information for each tube.
- Timing and region information from trigger chambers planned to be used for constraining segment reconstruction.
- Expect a ~1 mrad level resolution.

Input: hit signal synchronized with a clock.





Histogram with projected hit positions. At the time and in the region specified by trigger chambers.

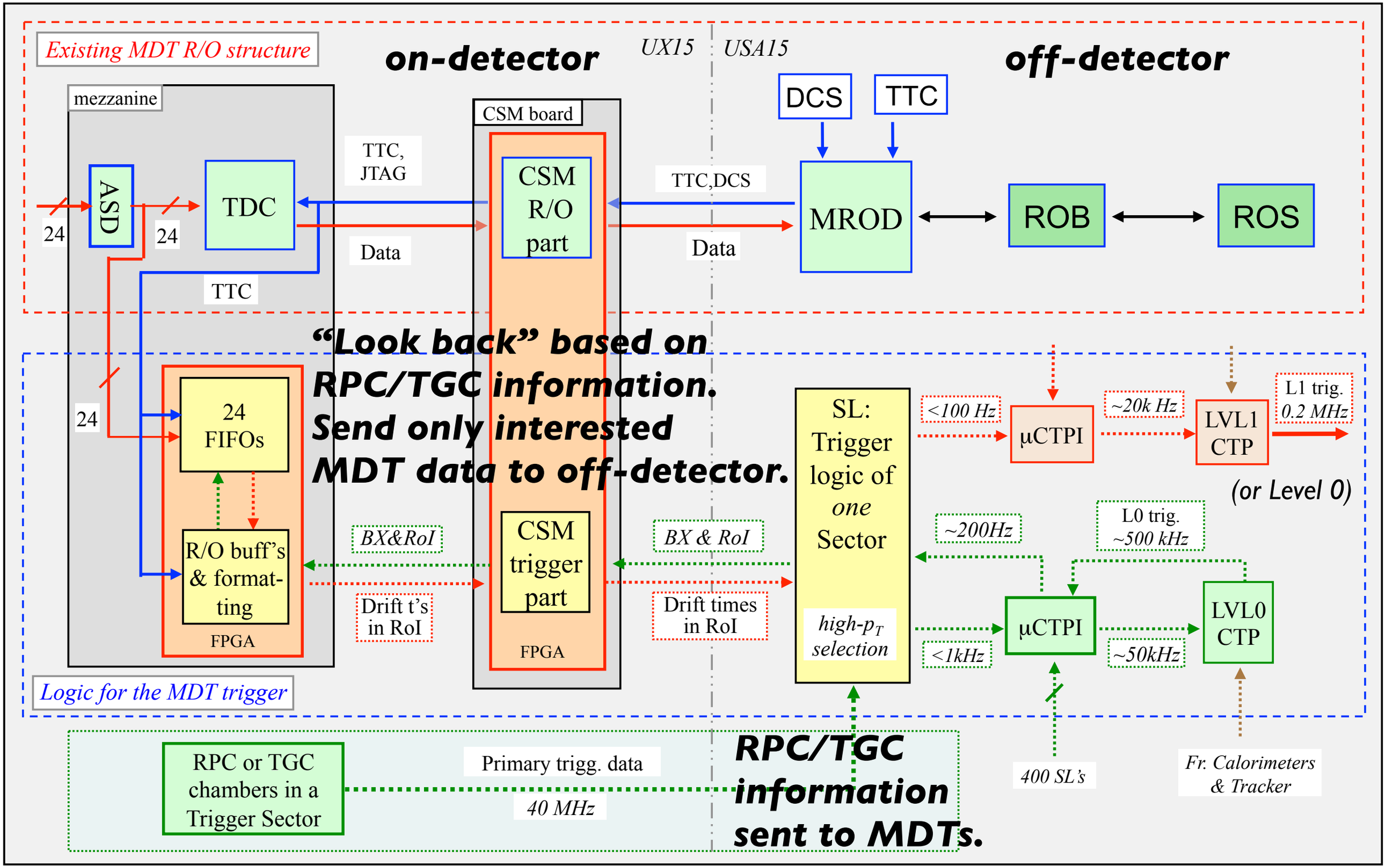
Overview of the proposed schema for MDT-based trigger electronics

- Will focus on two proposed schema for electronics.

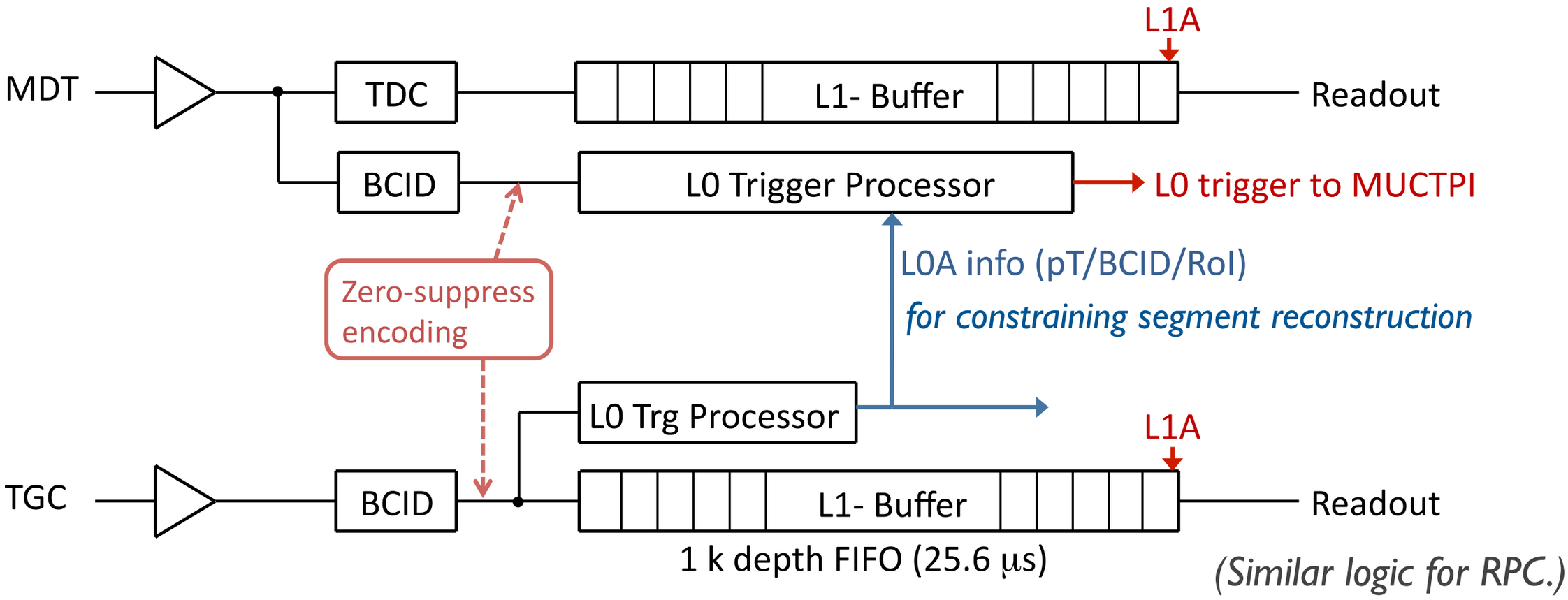
1. "RoI-based" scheme to send MDT data after selection based on regions of interest transferred from RPC/TGC to off-detector.
   - Less MDT information sent to off-detector (less fibers).
   - More latency due to the time of sending RoI to MDT frontend.
2. An alternative scheme to send all MDT data to off-detector.
   - Less latency since no transfer of RoI to MDT frontend.
   - More MDT information sent to off-detector (more fibers).

Bunch-crossing timing and region of interests from RPC/TGC
used for constraining segment reconstruction at MDT in both schema.

"RoI-based" scheme for MDT-based trigger



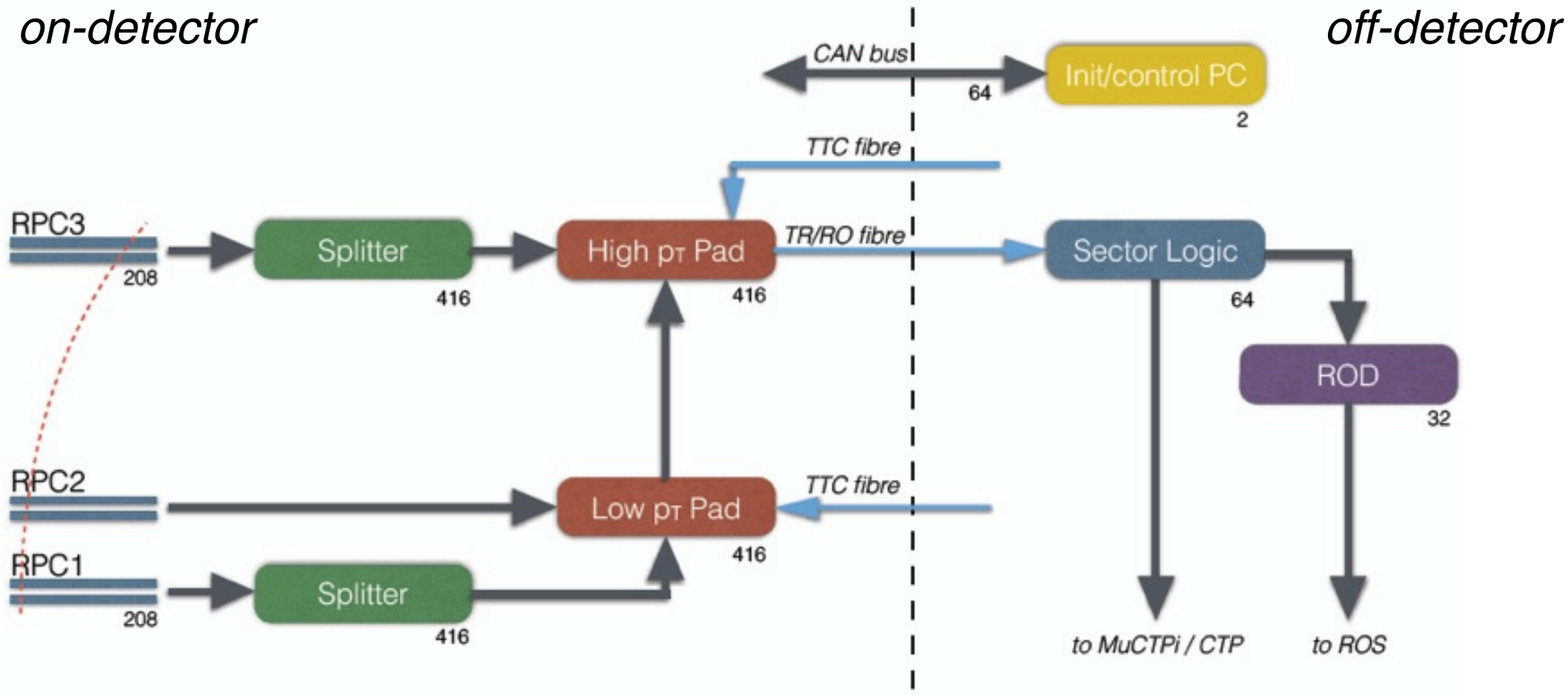
Alternative scheme for MDT-based trigger

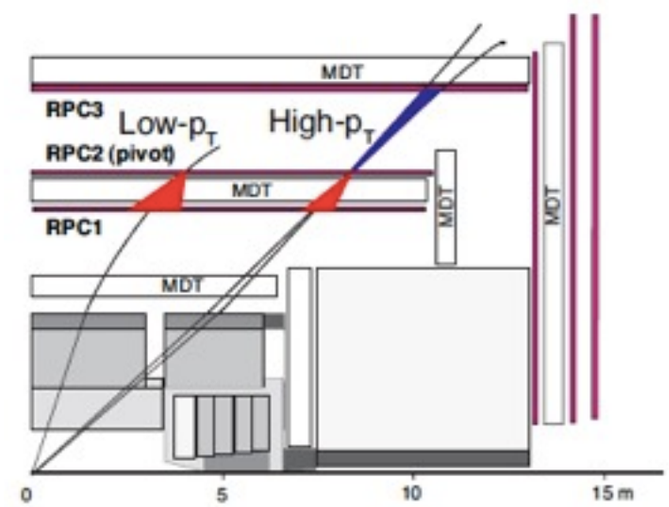


- MDT data sent to off-detector w/o selection based on TGC/RPC Info.
  - While data are merged, zero-suppressed, and encoded, more fibers are needed with respect to the "RoI-based" scheme. Estimated $\#_{fibers} \lesssim 5000$.
- Expected latency: < 4 μsec, safely smaller than Level-0 latency of 6 μsec.

2. Barrel Level-0 muon trigger

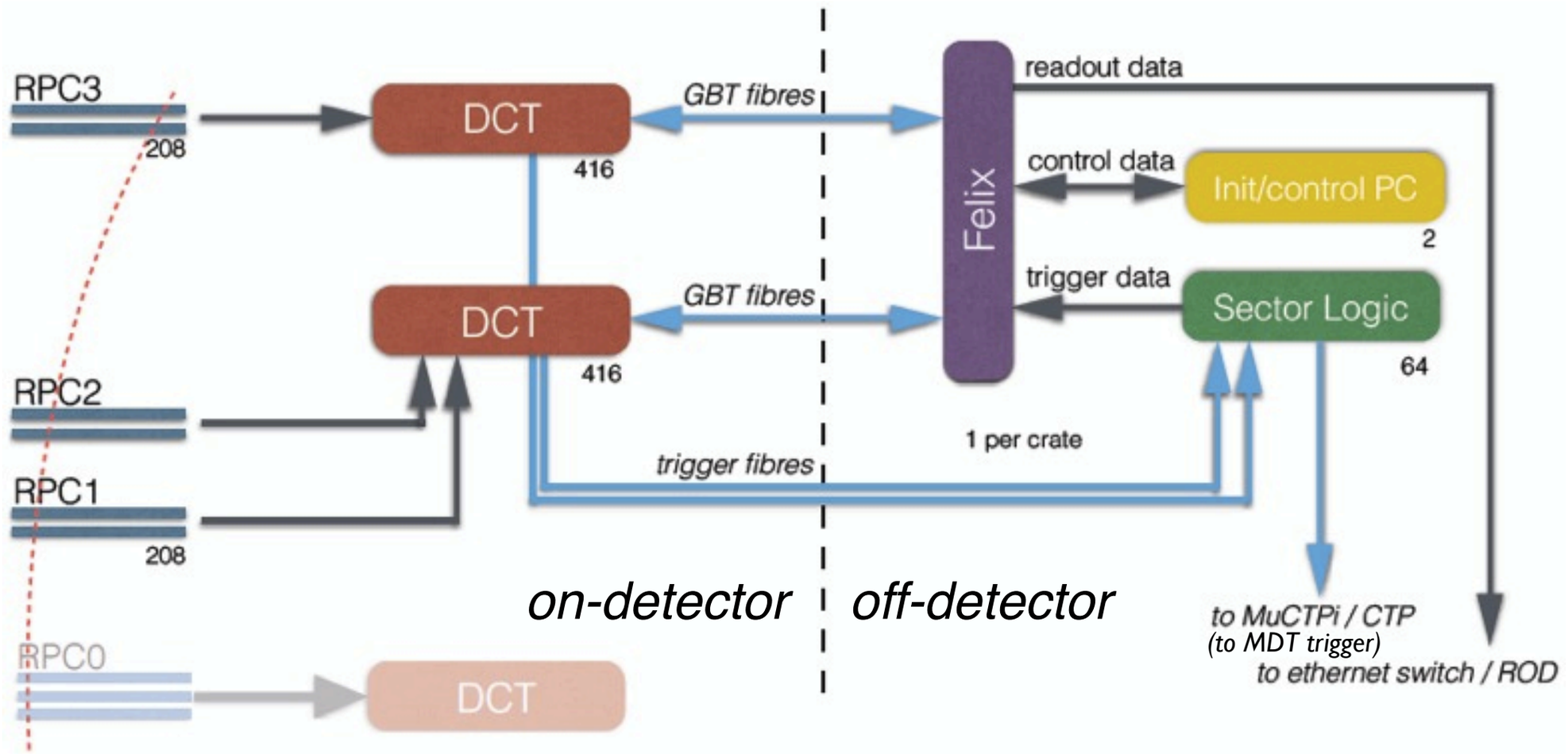
Current L1 muon barrel trigger system





- Pads take a coincidence between layers, selects candidates in η and φ independently, and associates candidates to regions of interest.
- Sector Logic selects muon candidates with a scheme based on coincidence windows, and sends trigger signal to MuCTPi.

Phase-II L0 muon barrel trigger system

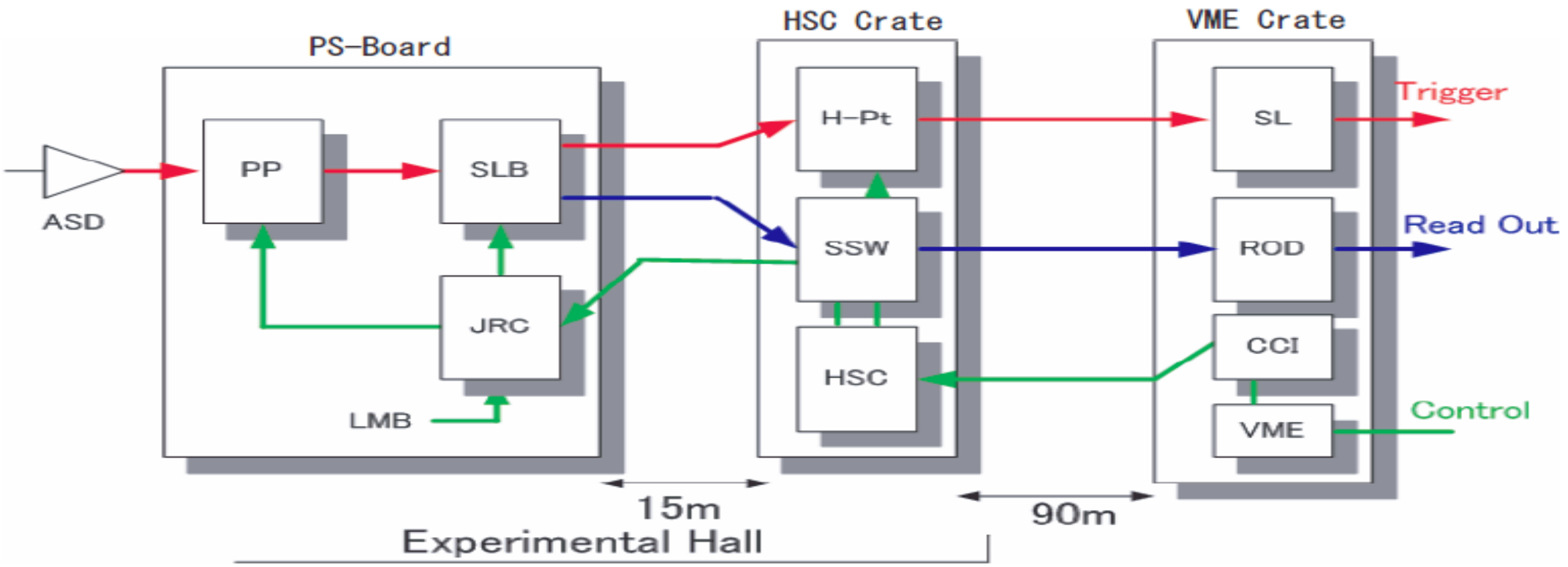


- Front-end cabling not replaced.
- Pad box replaced by DCT box.
  - Simple logic in DCT.
  - Time-over-threshold measurement considered for improving resolution.
- A proposal: installing RPCs in inner station.

- ROI-based scheme maintained.
- Most of the trigger algorithm in SL, providing flexibility, easier operation and maintenance, and less radiation.
- Information probably transferred to the MDT trigger electronics.

3. Endcap Level-0 muon trigger

Current L1 muon endcap trigger system



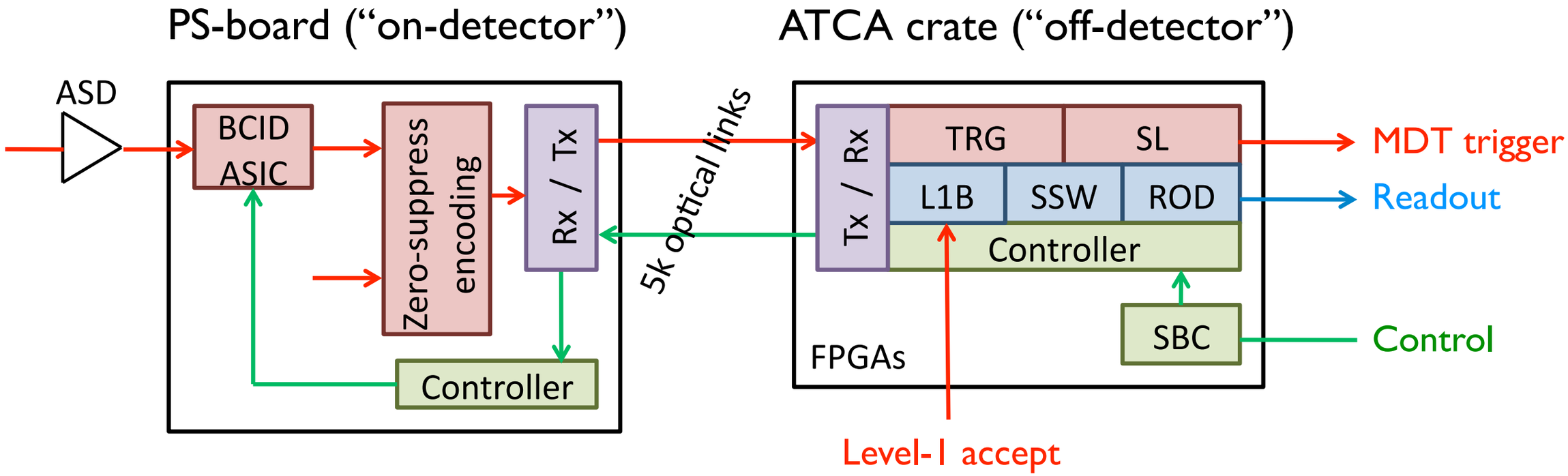
PS-Board (on chambers)
- Patch-Panel ASIC (PP)
  LVDS Rx, variable delay, BCID,
  Test pulse generator
- Slave Board ASIC (SLB)
  Trigger logic,
  L1-Buffer (3.2 μs), Readout

HSC Crate (on Big Wheel)
- H-pT Board, H-pT ASIC
  Trigger Logic
- Star Switch Board (SSW)
  Readout
- HSC
  Crate controller

VME Crate (USA15)
- Sector Logic (SL)
  wire-strip coin.
  pT calculation
- ROD
  Readout
- CCI
  front-end controller

Coincidence-window scheme in SL.

Phase-II L0 muon endcap trigger system



- ASIC's for PS-Board:
  - LVDS Rx, variable delay, BCID, and test pulse generator.
  - Zero-suppress and encoding logic of hit signals and interface to GBT.
- Module with FPGAs for trigger and readout located off-detector.
  - Most of the trigger algorithm located off-detector, providing flexibility, easier operation and maintenance, and less radiation.
  - Information for MDT trigger sent from Sector Logic ("SL").
  - Receive Level-1 accepts. Long Level-1 buffer (no separate Level-0 buffer).

Conclusion

- MDT-based trigger is a candidate of the Level-0/1 muon triggers for HL-LHC at ATLAS.
  - Trigger rate is estimated to reduce to about 50% based on a data sample for 8 TeV and 25 nsec.
  - RPC/TGC information for constraining tracking at MDT.
- RPC/TGC electronics will be replaced.
  - Most of the trigger logic will be located off-detector; increased algorithm flexibility, easier operations and maintenance, and less radiation.