Radiation Tests Discussion

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Considerations for GEM Components

- VFAT 2/3 chips will require SEU testing
  - Must do this in a beamline test… protons
    - Requires at least 40 MeV beam
    - Need flux ~10^8 p/cm^2/sec or higher
- Artix7 will require SEU and total dose tests
  - Can achieve both simultaneously in a beam test
  - Special firmware is probably required, with SEU mitigation
    - SEU tests must be designed in consideration of FPGA elements used in GEM firmware (BRAMs, GTX, etc)
  - Expected dose ~10 krad for 10 years at HL-LHC
    - Test to ~30 krad or more
- Other elements can probably be chosen from tables of already tested components
  - LDOs, PROMs, etc.
  - Need to make sure that OH-V2 uses GBT or Cern QPLL for de-jitter
  - What about SFF/SFP to be used for slice test?

Summary of All TAMU Reactor Tests (1)

Part/Chip Name	Chip Type	10 krad Exposure Pass/Fail	30 krad Exposure	Result Comments
Maxim 8557ETE	Voltage Regulator	Pass	Fail	5 out of 6 die at 30 krads
Micrel MIC69502WR	Voltage Regulator	Pass	Pass	
Micrel MIC49500WU	Voltage Regulator	Pass	Pass	
National Semi LP38501ATJ-ADJCT-ND	Voltage Regulator	Pass	Pass	
National Semi LP38853S-ADJ-ND	Voltage Regulator	Pass	Pass	
Sharp PQ05VY053ZZH	Voltage Regulator	Pass	Fail	Fails to regulate
Sharp PQ035ZN1HZPH	Voltage Regulator	50% Pass	Fail	Fails to regulate
Sharp PQ070XZ02ZPH	Voltage Regulator	Fail	Fail	Fails to regulate
TI TPS740901KTWR	Voltage Regulator	Pass	Pass	
TI TPS75601KTT	Voltage Regulator	Fail	Fail	Fails to regulate
TI TPS75901	Voltage Regulator	Fail	Fail	Fails to regulate
ST Micro 1N5819	diode	Pass	Pass	
ON Semi 1N5819	diode	Pass	Pass	
Fairchild 2N7000	N-channel FET transistor	N/A	Pass	
Analog Devices AD8028AR	High Speed, Rail-to-Rail Input/Output Amplifiers	N/A	Pass	
Analog Devices ADM812	Voltage Monitor	N/A	Pass	
National Semi LM41211M5-1.2	Precision Micropower Low Dropout Voltage Reference	N/A	Pass	
National Semi LM4121AIM5-ADJ	Precision Micropower Low Dropout Voltage Reference	N/A	Pass	

Summary of TAMU Reactor Tests (2)

Part/Chip Name	Chip Type	10 krad Exposure Pass/Fail	30 krad Exposure	Result Comments
National Semi LM19CIZ	TO-92 Temperature Sensor	N/A	Pass	
Maxim MAX680CSA	+5V to ±10V Voltage Converter	N/A	Pass	
Maxim MAX664CSA	Dual Mode 5V/Programmable Micropower Voltage Regulator	N/A	Fail	Dead
Maxim MAX4372	High-Side Current-Sense Amplifier	N/A	Pass	
Micrel MIC35302	High-Side Current-Sense Amplifier	N/A	Fail	Dead
Micrel MIC37302	High-Side Current-Sense Amplifier	N/A	Fail	Dead
Fairchild MM3Z4V7C	Zener Diode	N/A	Pass	
Fairchild MM3Z5V1B	Zener Diode	N/A	Pass	
Sharp PQ7DV10	Variable Output 10A Voltage Regulator	N/A	Pass	
TI TPS7A7001	Very Low Dropout, 2A Regulator	N/A	Fail	Fails to regulate

Summary of TAMU Reactor Tests (3)

Part/Chip Name	Chip Type	10 krad Exposure Pass/Fail	30 krad Exposure	Result Comments
TI SN74LVC2T45	Two-bit Dual-supply Tri-statable Bus Transceiver	N/A	Pass	
Analog Devices ADM660AR	CMOS Switched-Capacitor Voltage Converter	N/A	Pass	
Analog Devices ADM8828	Switched-Capacitor Voltage Inverter	N/A	Pass	
Intersil ICL7660S-BAZ	Switched-Capacitor Voltage Converter	N/A	Fail	Dead
Linear Technology LTC1044CS8	100mA CMOS Voltage Converter	N/A	Pass	
Maxim MAX1044CSA	Switched-Capacitor Voltage Converter	N/A	Fail	Dead
Maxim MAX860-UIA "uMAX"	Switched-Capacitor Voltage Converter	N/A	Pass	
Maxim MAX861-ISA	Switched-Capacitor Voltage Converter	N/A	Pass	
Microchip TC1044SCOA	Charge Pump DC-TO-DC Voltage Converter	N/A	Pass	
Microchip TC962COE	High Current Charge Pump DC-to-DC Converter	N/A	Pass	

SEU Test Results for CSCs

- Performed at UC Davis and TAMU Cyclotron facilities
  - All chips survived 30 kRad dose

- Finisar Optical Transceiver ftlf8524e2gnl: Transmit side
  - Gigabit Ethernet packet transmission tests to PCI card, 4 kB @ 500 Hz
    - ➢ Bad or missing packets received at the PC are "transmit" SEUs
    - ➢ Note that the duty cycle here is significantly less than 100%
  - These SEUs caused lost GbE packets and rare "powerdown" events
  - SEU cross section result: $\sigma = (4.3 \pm 0.3) * 10^{-10}$ cm^2
  - Correcting for real CSC transmitter duty cycle: $\sigma = 6.7 * 10^{-8}$ cm^2 per link
    - ➢ We expect to see ~10 SEU per link per day during HL-LHC running
      - Very low rate of single bit errors: just 1 error per 20 trillion bits on each link
- Finisar Optical Transceiver ftlf8524e2gnl: Receive side
  - These SEUs only caused transient bit errors
  - SEU cross section: $\sigma = (7.5 \pm 0.1) * 10^{-9}$ cm^2 per link
    - ➢ We expect to see ~1 SEUs per link per day
  - *Three Finisars tested: one died at 33 krad, another at 41 krad
    - ➢ The third chip survived with 30 krad and still working on the bench in 2014

FPGA SEU Results for CSCs

- Xilinx Virtex-6 FPGA, model xc6vlx195t-2ffg1156ces
  - Enabled native ECC feature in Block RAMs
  - CLB tests based on triple-voting system
  - Results are summarized below

- GTX Transceiver (55% used in FPGA)
  - Random PRBS data patterns @3.2 Gbps on each of eight links
  - These SEUs only caused transient bit errors in the data
  - SEU cross section result: $\sigma = (10 \pm 0.8) * 10^{-10}\ \mathrm{cm}^2$
- Block RAM (74% used in FPGA)
  - Built-in ECC feature was used to protect data integrity
  - Software controlled write and read for BRAM memory tests
  - No errors were detected in the BRAM contents: mitigation at work
  - SEU cross section: $\sigma_{90\%} < 8.2 * 10^{-10}\ \mathrm{cm}^2$
- CLB (43% used in FPGA)
  - SEU cross section result: $\sigma = (6.0 \pm 0.5) * 10^{-9}\ \mathrm{cm}^2$
    - With this we expect ~1 CLB SEU per FPGA per day in CSC DCFEBs

Other References

- From Magnus
  - https://twiki.cern.ch/twiki/bin/viewauth/CMS/RadiationHardCOTS