The CMS Endcap Muon Modular Track Finder (MTF) Overview / Software

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Re-commissioning legacy SP

MPC and SP participate in all CSC global runs – CSCTF provides triggers for readout

Conversely:

- **we can test new MPC hardware at the B904 test stand**
- **otherwise, little operational testing that we can do without running with the CSC system at P5**

At run start, CSCTF system will be operationally at least as ready for beam as CSCs are:

- **MPCs will be validated with new mezzanines mounted**
- **MPC → SP communication will be validated**

If any element of the chain is not working, this will immediately be seen in the CSC global runs – chambers or sectors will not produce triggers

CSCTF Specific Tasks:

Use of legacy software, firmware minimizes work needed

Upgrade online PC OS / update software as needed

(in sync with rest of CMS AFAIK)

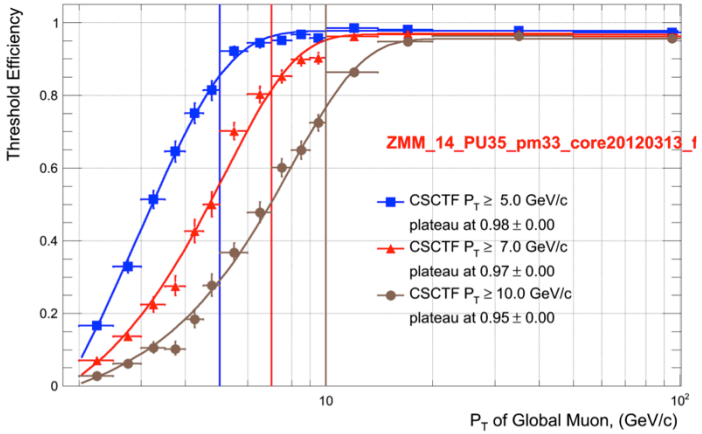
Include unganged ME1/1 information:

- **Validate ME1/1 input format**
- **Get approval of track quality changes**
- **Modify firmware accordingly**
- **To first order, p_T LUTs are ok**

Corrections for ME4 B field changes:

- **Waiting on official samples with correct B fields**

old core, ptmethod33
high eta quality 3



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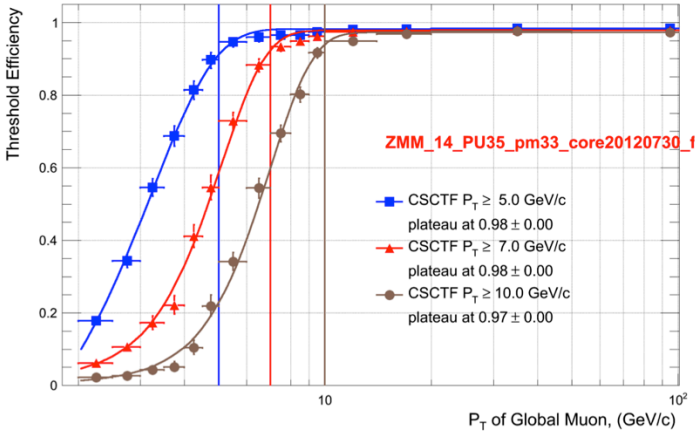
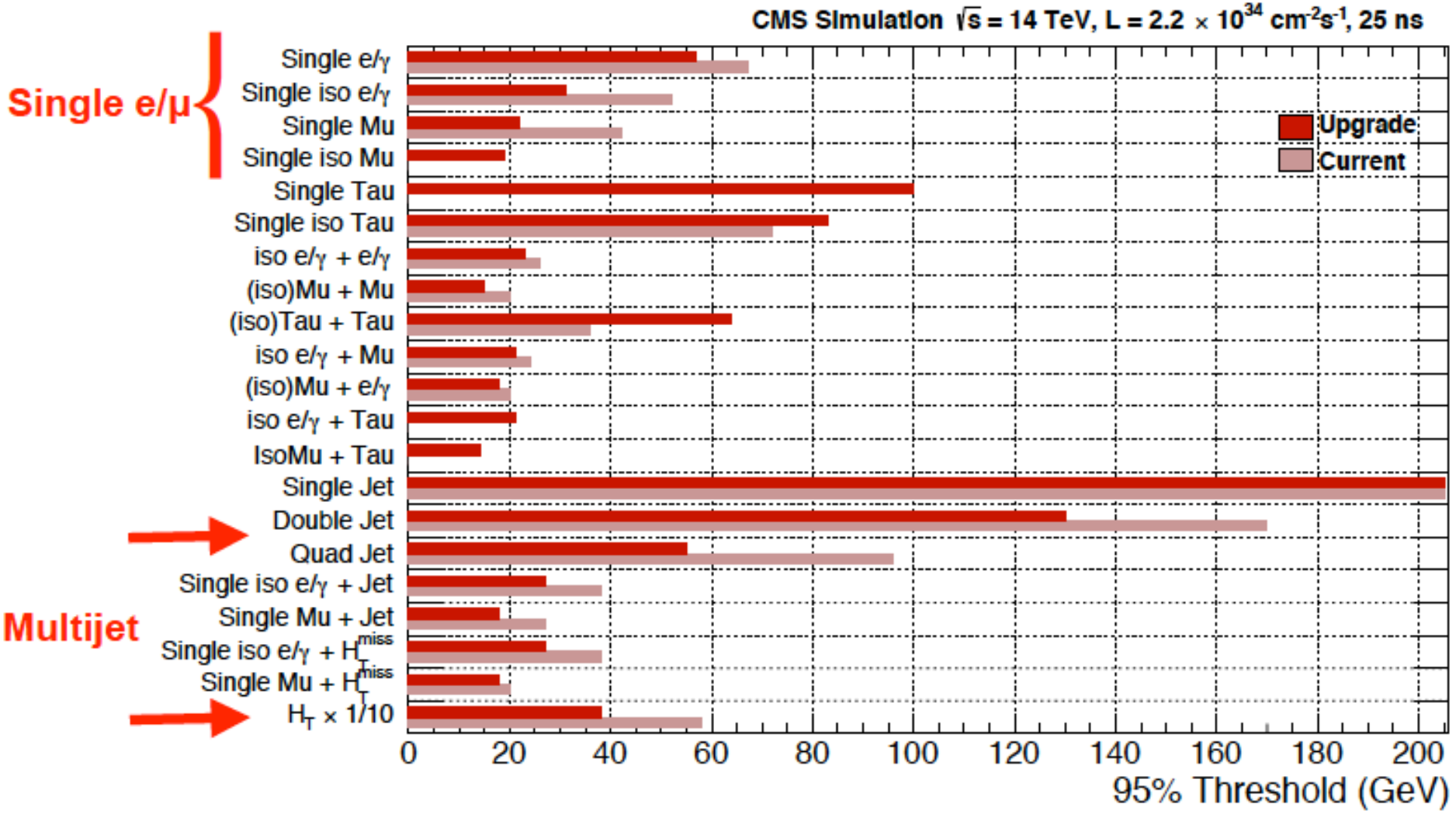


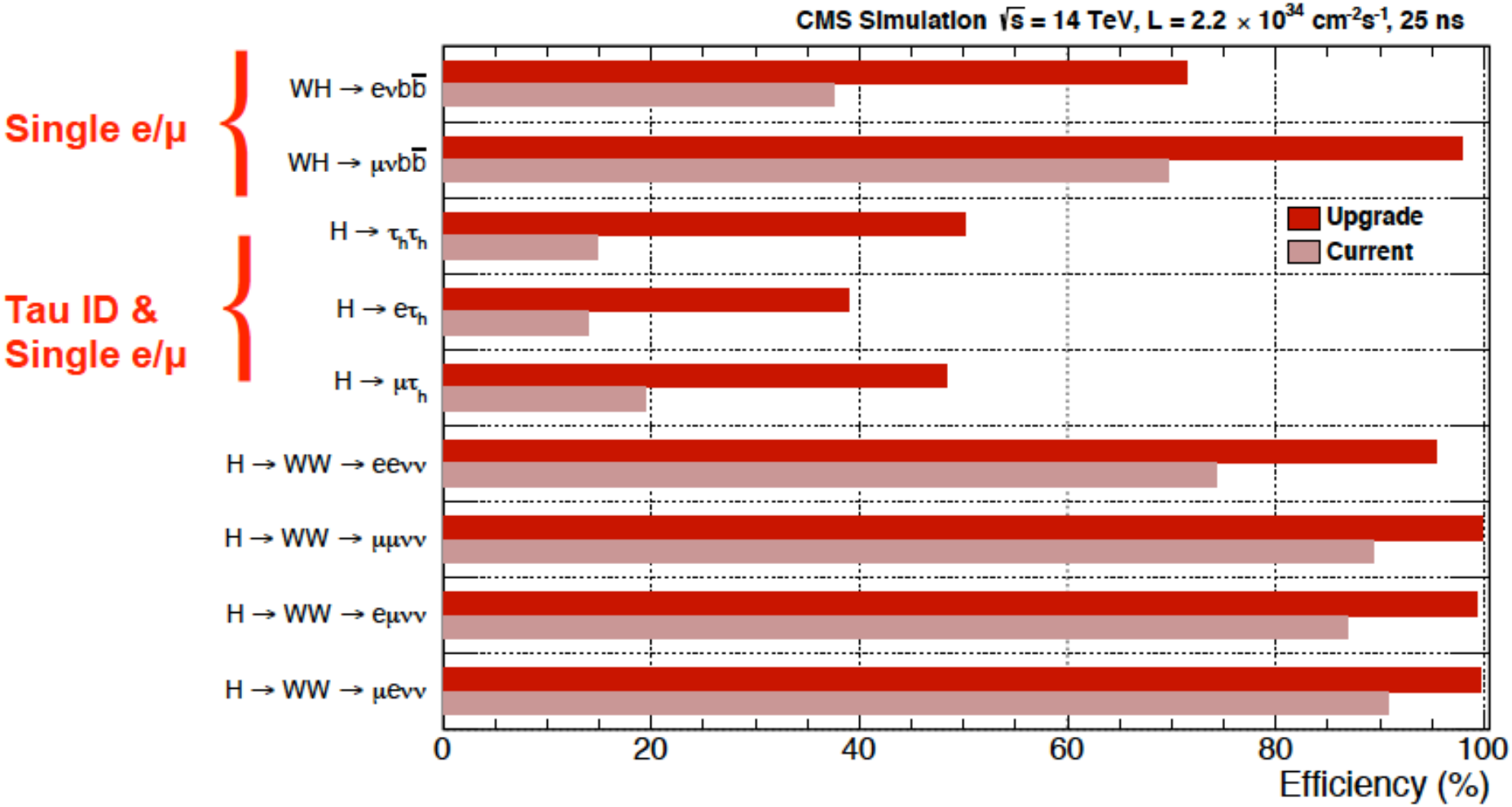
L1 Upgrade – Executive Summary

- **Trigger rates are driven by the increase in luminosity, the center-of-mass energy, and by higher PU**
- **Mitigate by improving e/γ isolation, τ id, muon pT resolution, muon isolation, jets with PU subtraction, and L1 menu sophistication**
- **Increase system flexibility with high bandwidth optical links and large FPGAs, and standardize on μTCA telecom standard in CMS**
- **Build and commission upgrade in parallel with current trigger system to safeguard physics, decouple from LHC schedule**
  - **Target deployment in 2016, implement some improvements in 2015**
- **Overall design:**
  - **Two-layer calorimeter trigger with tower-level precision and pile-up energy subtraction**
  - **Integrated muon trigger combining all 3 muon systems in track-finding, more sophisticated pT measurement**

Performance: Trigger Thresholds



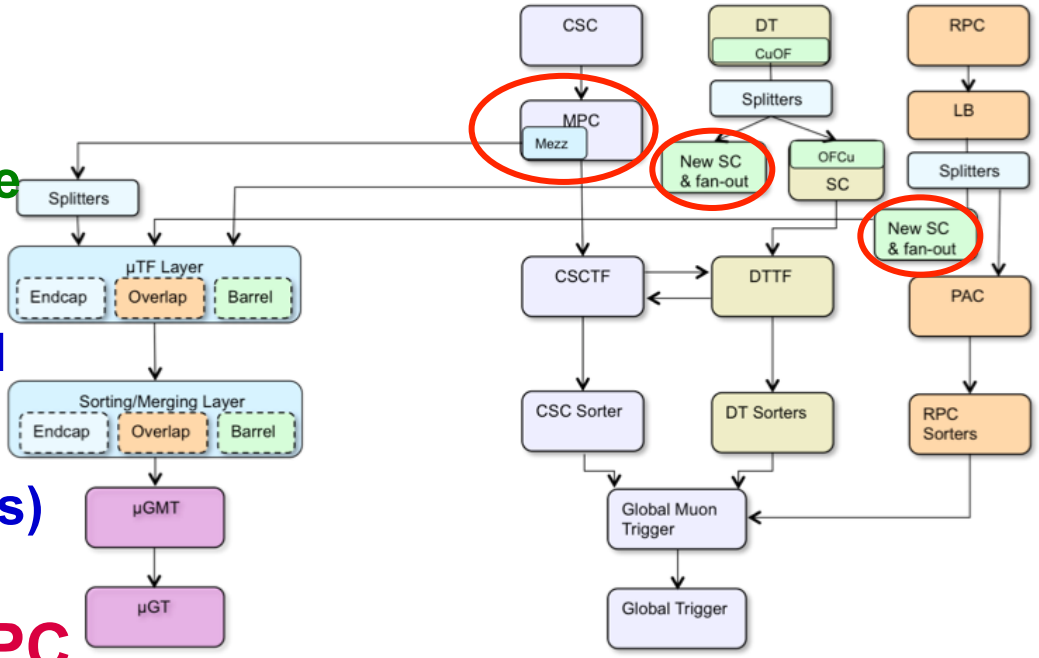
Performance: Higgs



Overview: Muon Trigger

Install fully parallel and higher bandwidth optical path for CSC

- **New CSC MPC mezzanine cards installed in cavern during LS1**
- **Alleviates bottleneck and send all segments from each CSC (robustness to PU and collimated signals)**



Install splitters for a *fraction* of DT and all RPC in LS1 and add new fanout and data concentrator systems

Build up new Track Finder in 2015 and commission in parallel, ready by 2016

- **Endcap hardware design is proposed by CMS to be used for all muon regions: endcap, barrel, and overlap**

Muon Track Finder Upgrade

Improve upon successful features of current CSC Track-Finder

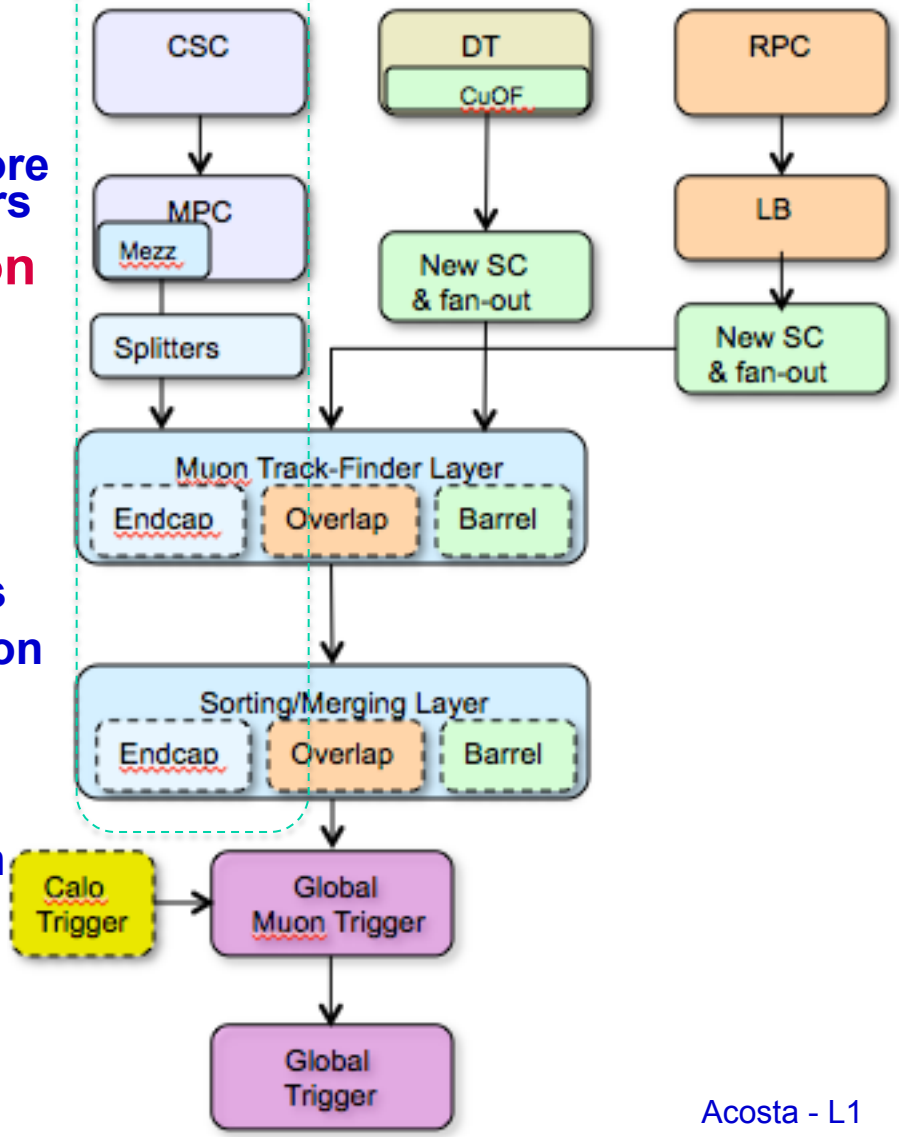
- Enlarge LUT memory for pT assignment, and FPGA to handle more hits from PU and additional chambers

Use the redundancy of the three muon detection systems earlier in the trigger chain

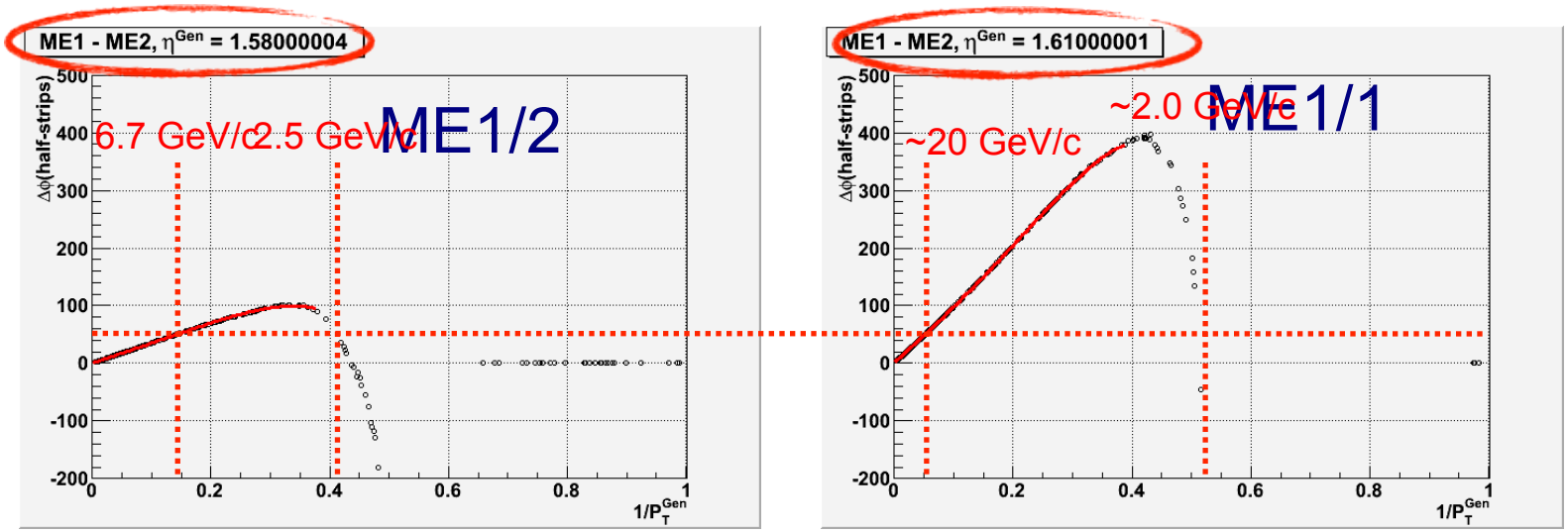
- Create one higher resolution muon trigger rather than combine lower resolution ones
- Improve robustness in the case of dead channels/chambers and cracks
- Refine deflection angle at each station when two muon systems record hits

Segment into Barrel, Overlap, and Endcap regional processors

- No lateral data exchange, split muon signals upstream of Track-Finders
- Report more muons, and at higher precision, for improved isolation, b-tagging, invariant mass, etc. at the Global Trigger



p_T assignment issues Specific to CSCTF

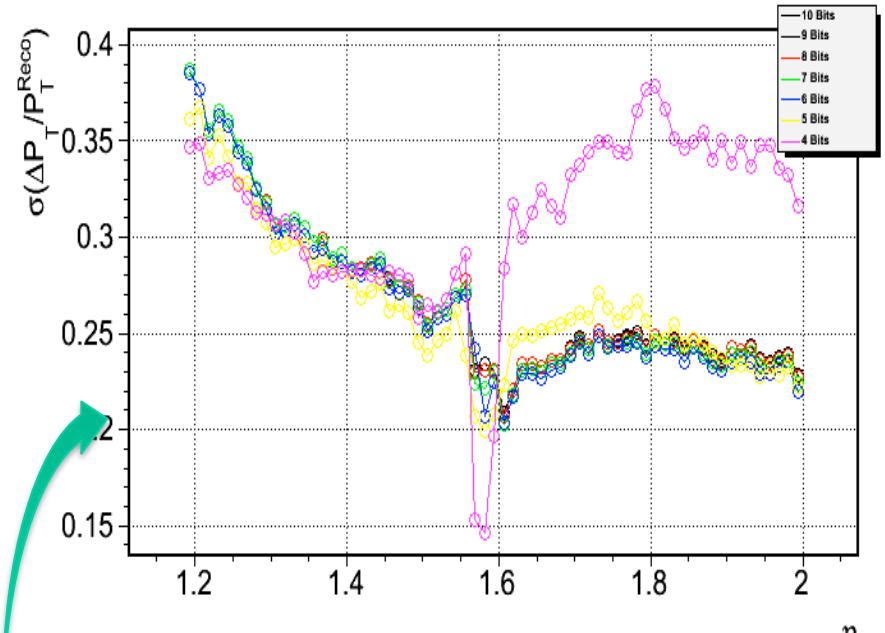


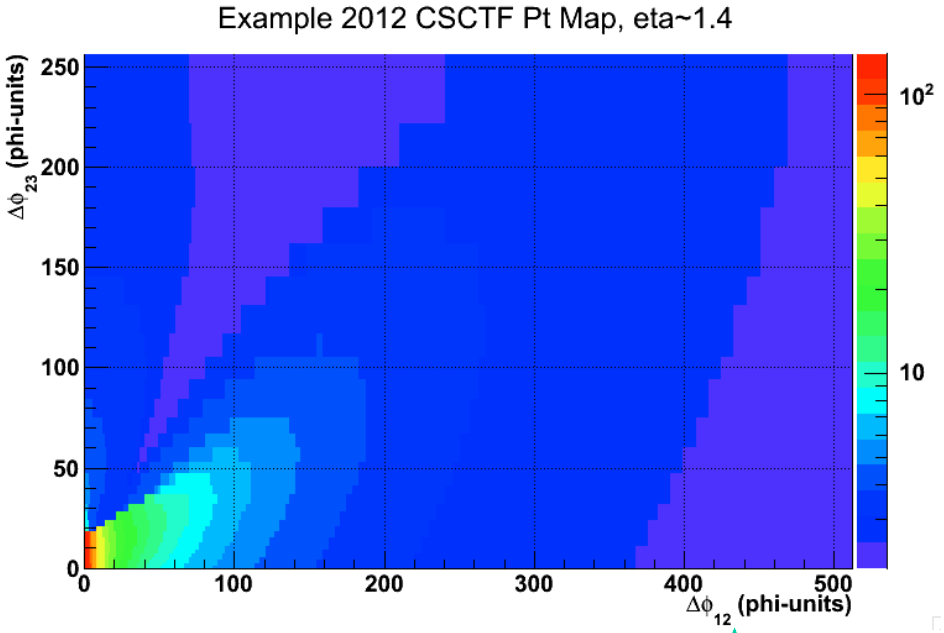
Example using muon propagator

B field is inhomogenous, path length varies as well - deflection amount is very η-dependent

The behavior of ME1-ME2 muons strongly depends on which part of ME1 they hit (ME1/1 vs ME1/2)

CSCTF p_T Assignment Method





most powerful variables sent into η-specific LUTs

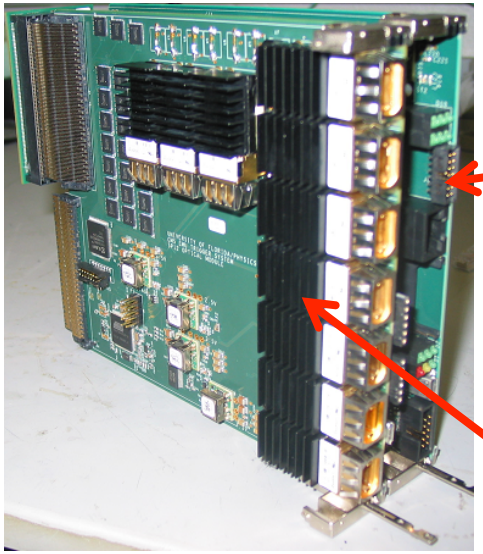
LUT outputs p_T, currently hardwired to board output content determined via max log-likelihood fit

variable Δφ binning of LUTs gives more precision where it is more useful for p_T assignment

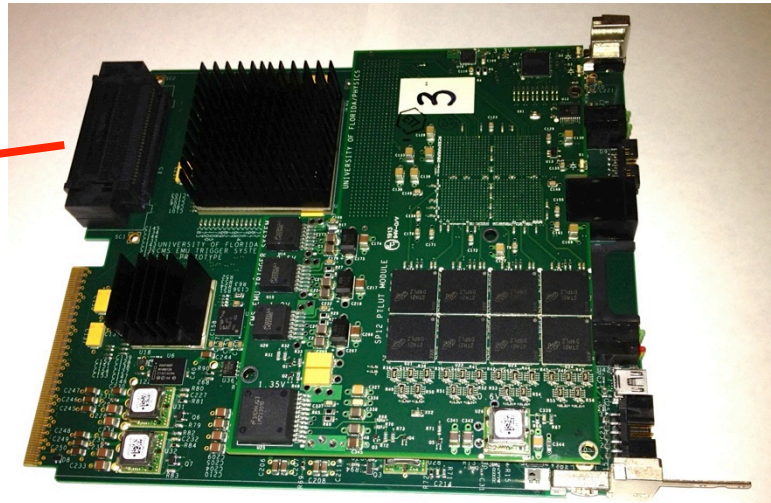
Muon Trigger Hardware: MTF7

Muon Track Finder processor

- Optimized for maximum input from muon detectors (84 input links, 24 output links)
- Dual card with large capacity for RAM (~1GB) to be used for p_T assignment in track finding



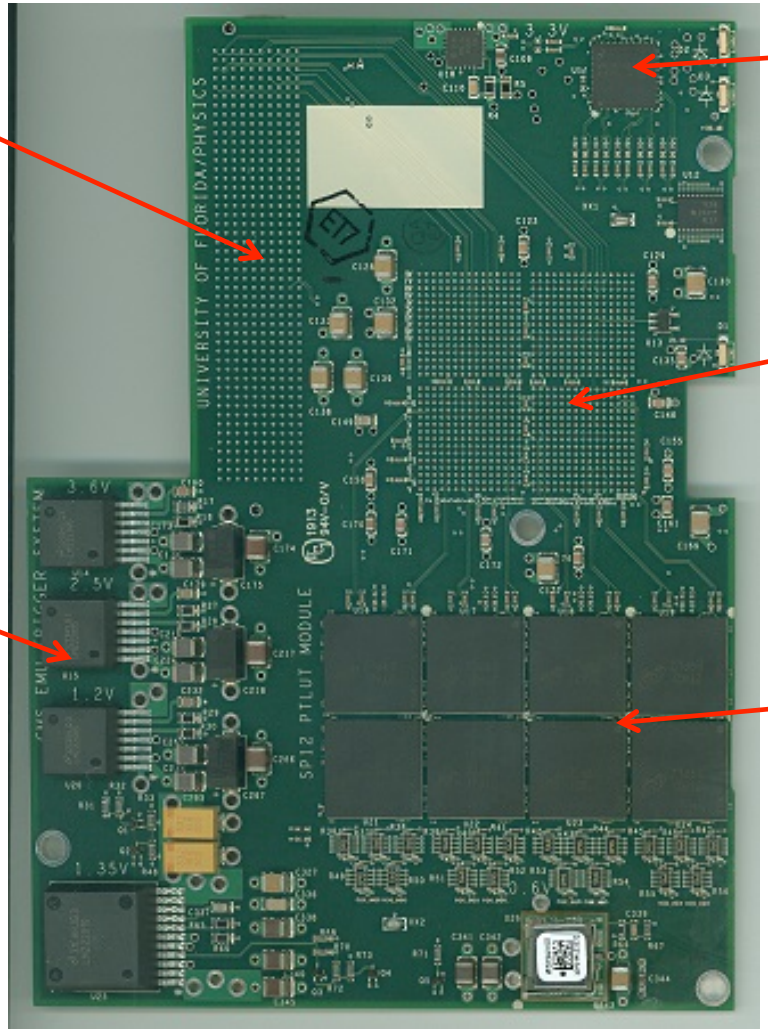
Front: Optics card



Back: Core FPGA card with P_T LUT mezzanine

- Current prototype based on Virtex 6 FPGA is undergoing final tests (RLDRAM memory access)
- Virtex 7 FPGA design is ~75% done, expected late 2013

p_T LUT module



Base board connector

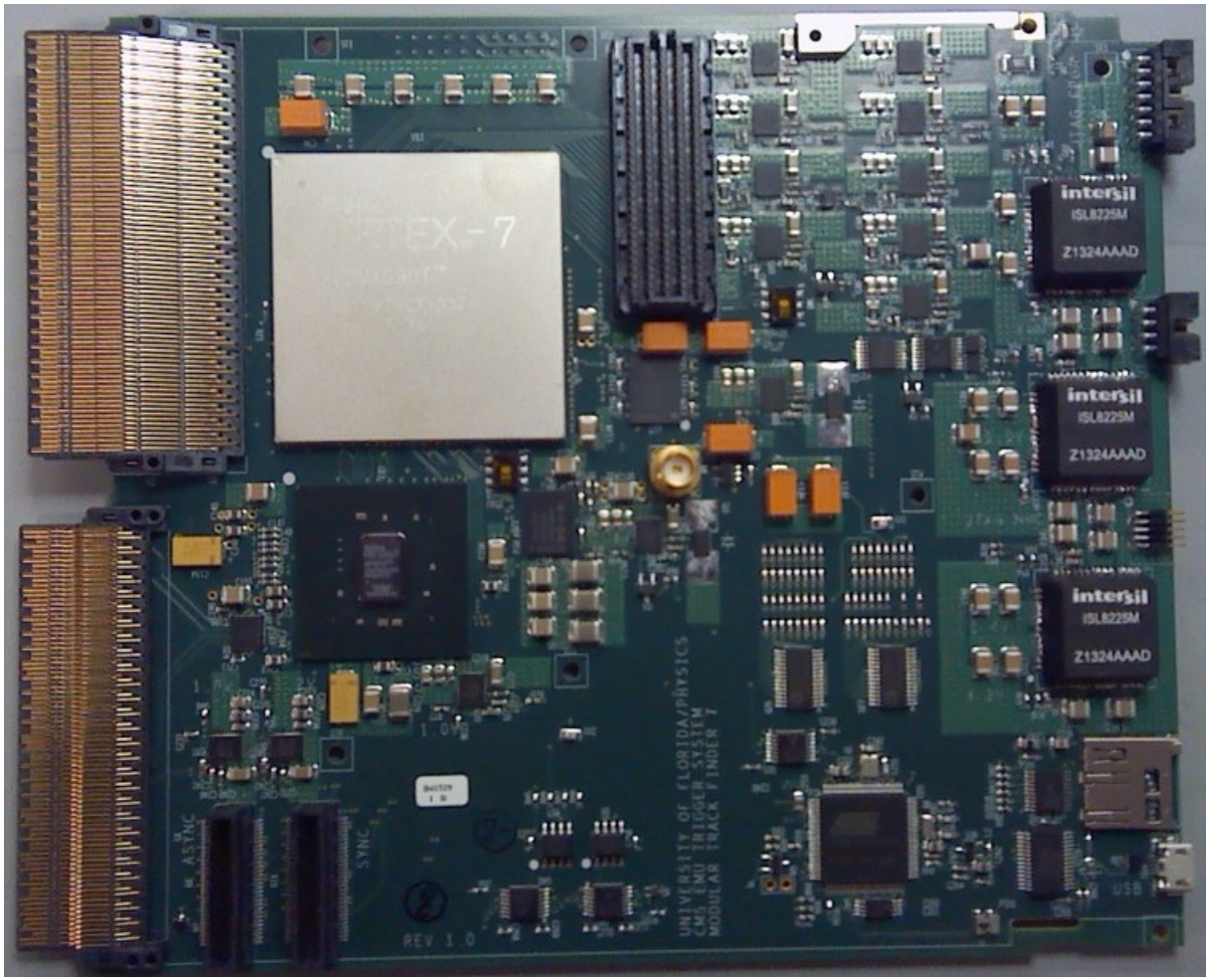
Clock synthesis and distribution

Glue logic FPGA (Spartan-6)

DC-DC converters

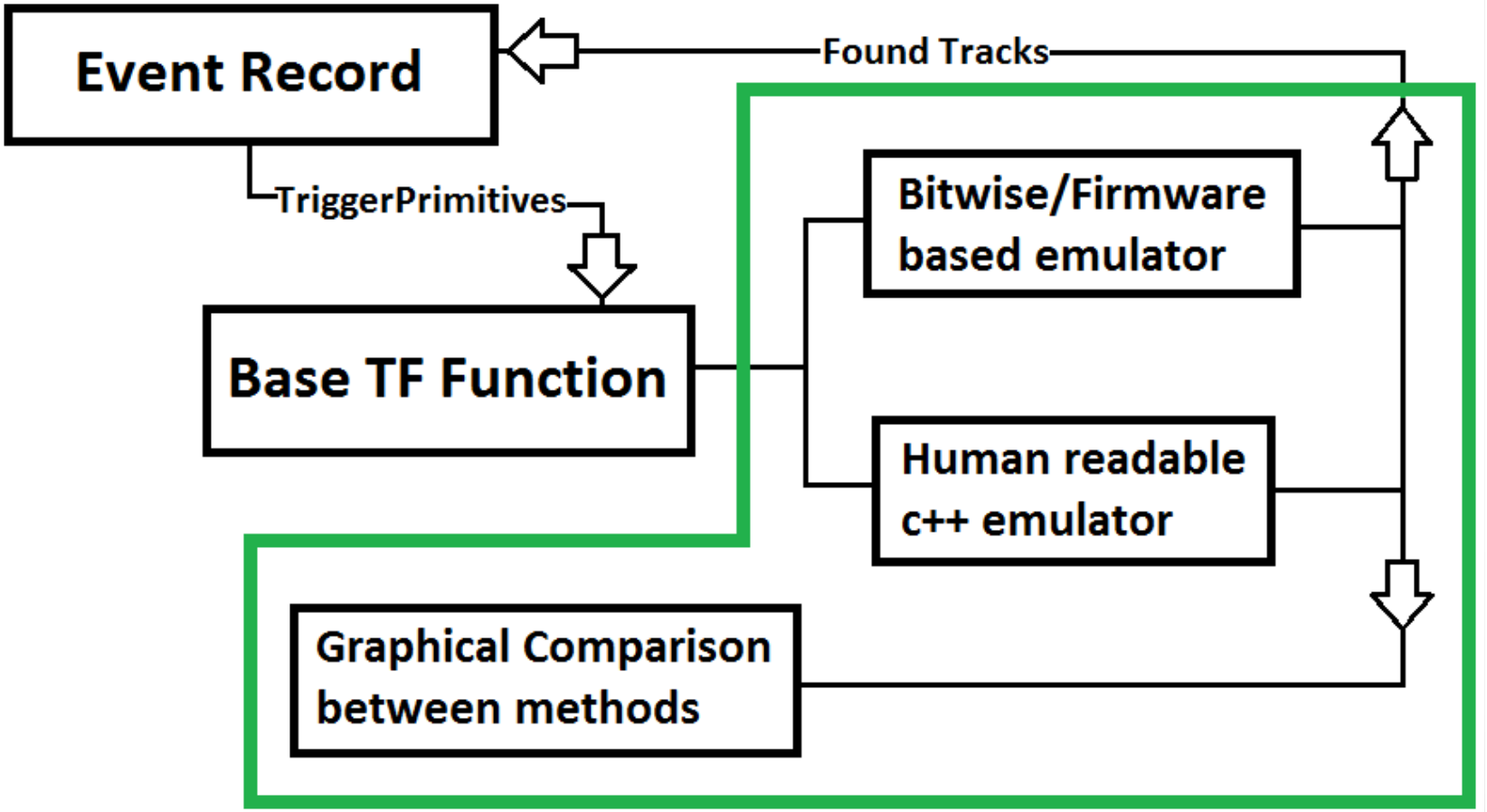
RLDRAM3 memory
16 chips, 8 on each side
(clamshell topology)
Total size:
512M x 18 bits ≈ 1GB
Upgrade possible to
2 GB with bigger
RLDRAM3 chips
(no board redesign)

MTF7 Base Board Prototype



- **Detailed review in A. Madorsky's talk next**

Emulator And Offline Software



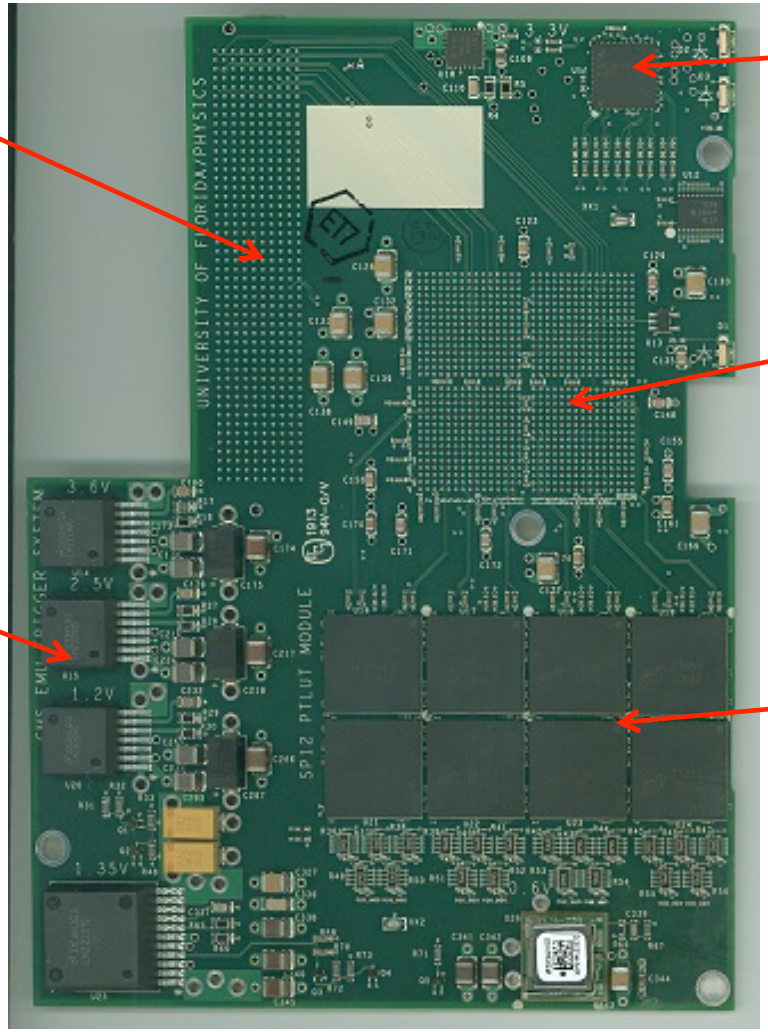
- First version of each part of the chain written and tested
- Now cleaning up, working on better interface(s)

TF Algorithm Performance

Category	Count	Frac.
Muons generated	4627	---
No LCTs in event	7	0.2%
One LCT in event	76	1.6%
“Fair game” muon in event	4544	100.0%
One muon track found	4451	**98.0%**
Two muon tracks found	51	**1.1%**
No muon tracks found	42	**0.9%**
LCTs in ME3, ME4 only	31	0.7%
Other Algo. Failure	11	**0.3%**

- **Efficiencies due to design, algorithm and choices recovered**
- **Need to address ghosting (~1%), interface to p_T assignment**

PT LUT module



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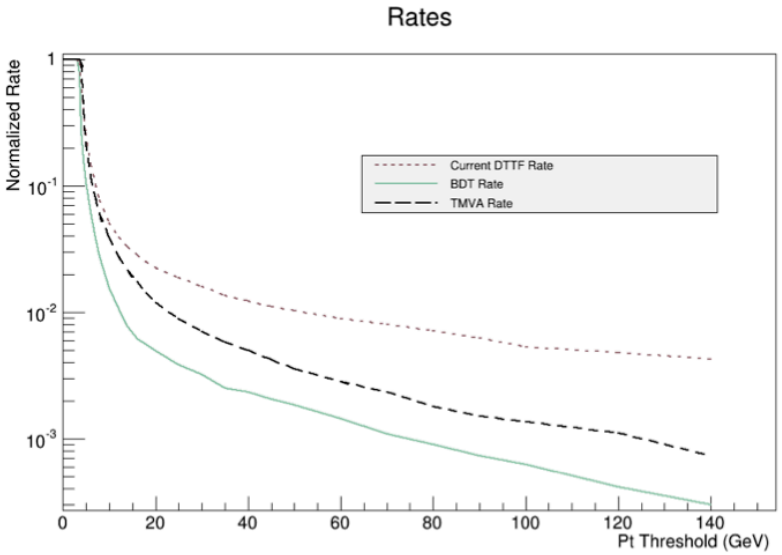
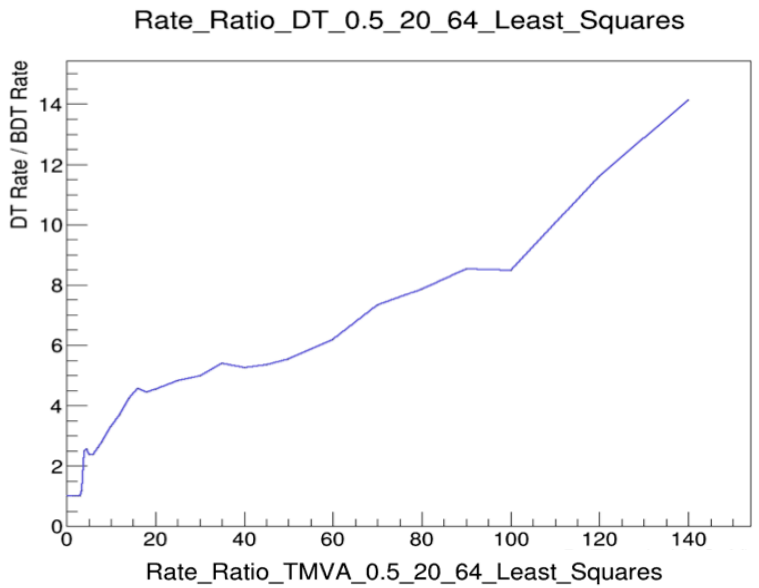
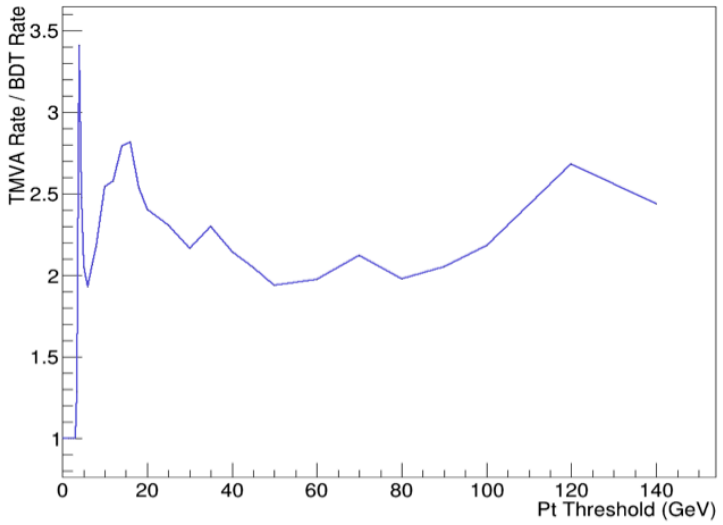
BDT p_T assignment





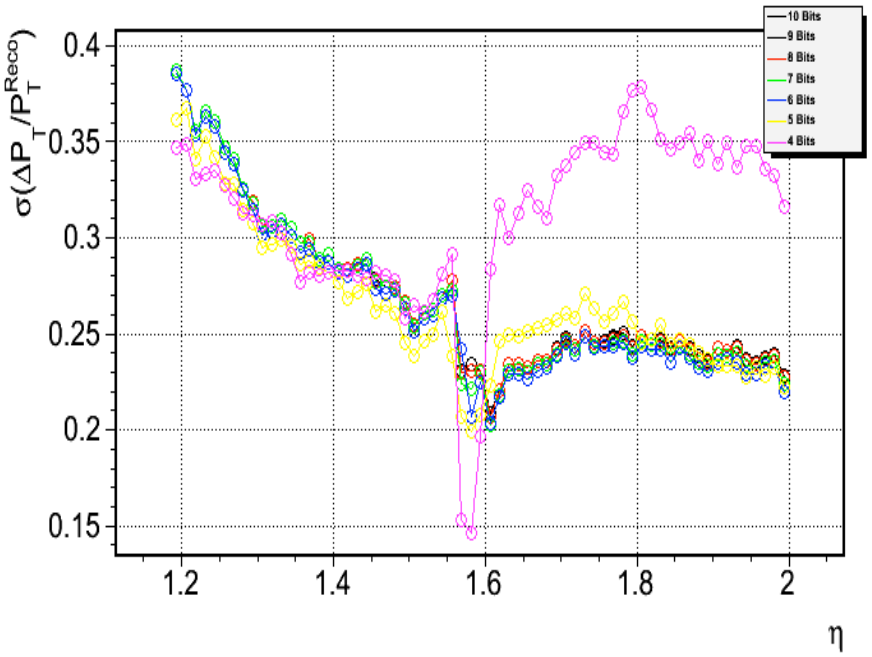


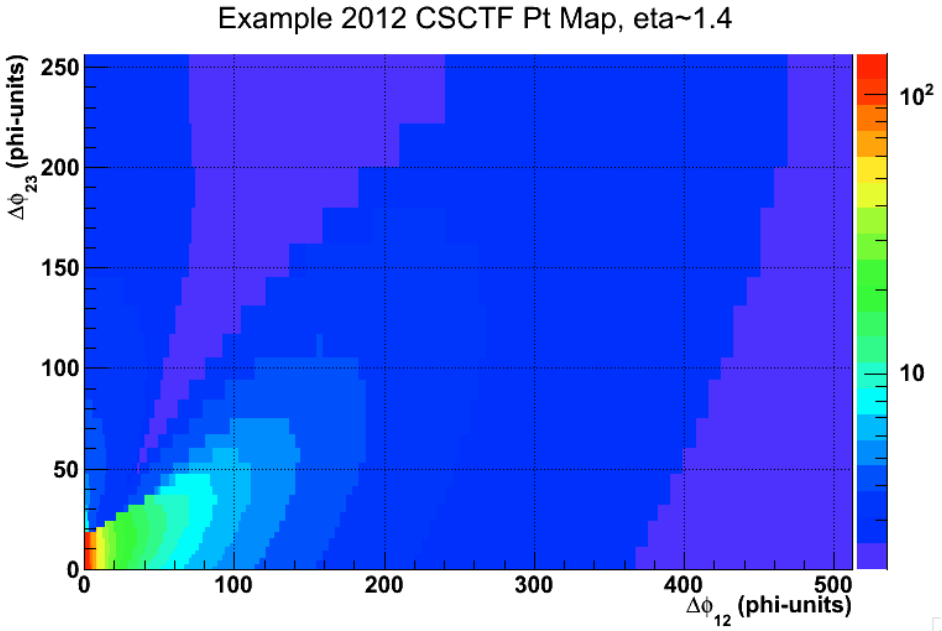
Improved BDT performance:

- **Finalized study with DTTF information as placeholder**
- **Private BDT allows more complex topologies than TMVA**
- **Least squares loss function gives more weight to tails – rate reduction**

Memory Address Space

- Assigning pT offline is one part of the problem - BDTs
- Optimally recording this information in LUTs is another [chopping up parameter phase space]
- Investigated various ways of finding optimal distribution, none solve problem automatically
- First iteration – use same technique as for CSCTF:



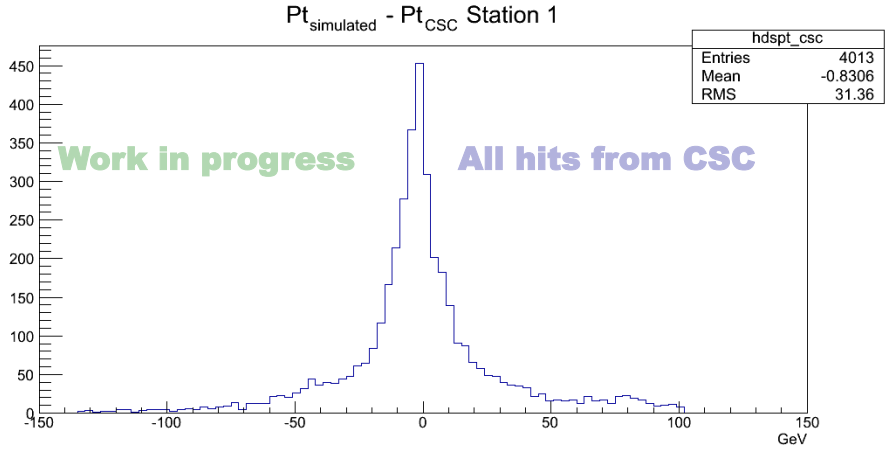


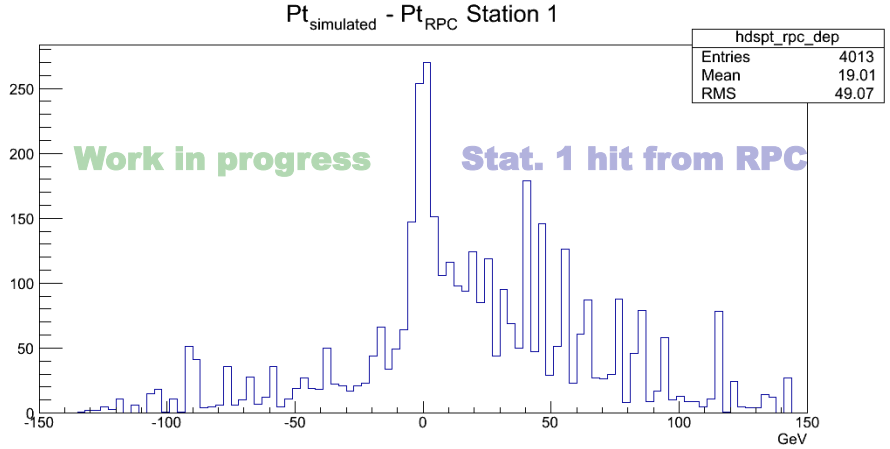
Explore new handles

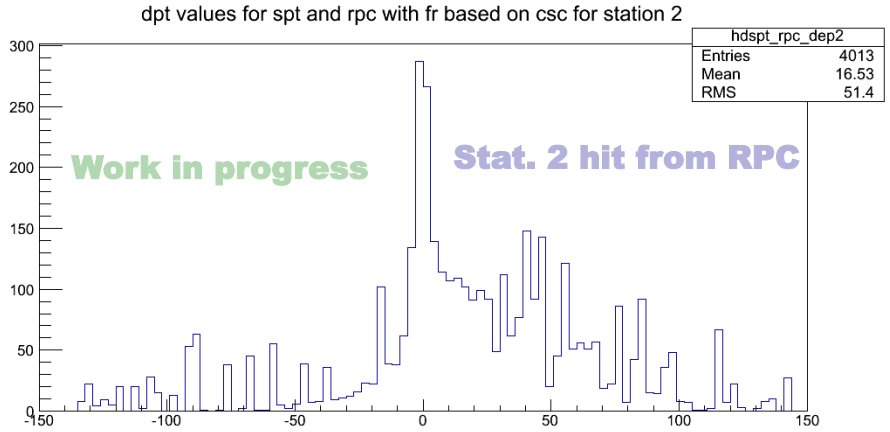
Construct pointing angles:

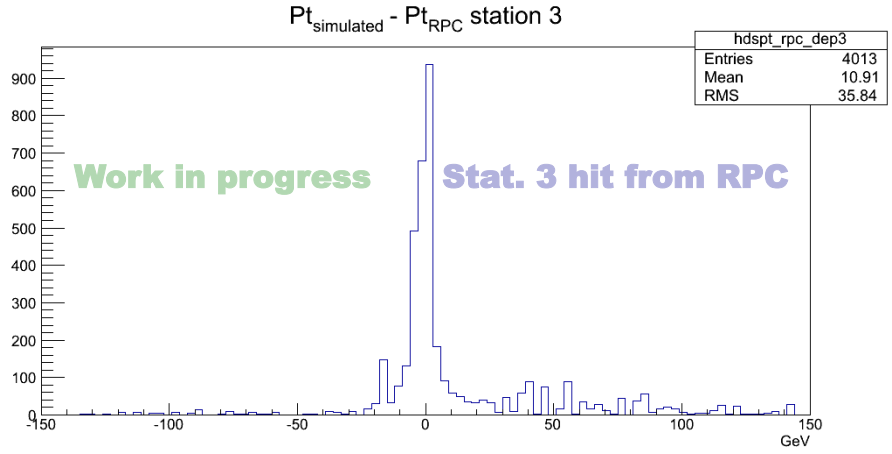
- Sector overlap regions, chamber overlap regions

Study use of RPC hits in pT assignment:









Roadmap to commissioning (I)

- **Hardware:**
  - Build + test MTF7 prototypes (A. Madorsky)
  - Build + test MPC prototypes (M. Matveev)
  - Lay down fibers to counting room (TBA)
  - Build prototype patch panel (A. Madorsky, C. Reeves)
    - test, ship to CERN, install in counting room (TBA)
- **Firmware:**
  - Core logic firmware (A. Madorsky)
  - "Wrapper" – spy buffers, registers, DAQ (TBA)
  - Detector geometry, pT assignment tables (TBA)
- **Offline Software:**
  - First implementation of track finding algorithm (A.Madorsky, M.Carver)
  - First implementation of pT assignment module (B. Scurlock, A. Carnes) – in progress
  - First implementation of post-LUT tail clipping

Roadmap to commissioning (II)

- **Offline Software, continued:**
  - First version of bitwise emulator (M. Carver) handed off to GEM trigger group for studies
  - Online / offline monitoring – need to write equivalent of CSCTF online / offline monitors for new objects
- **Online Software:**
  - Run control via PCIExpress, IPBus
  - PCIExpress included into HAL (G.P. Di Giovanni)
    - Expect this will simplify online SW development
    - Start from porting CSCTF online onto HAL + PCIExpress

MTF7 Schedule

Prototype validation

- Bench testing (Feb-Mar 2014)
- MTF7→MP7 (GMT) integration test (April 2014)
- RPC GOL → MTF7 integration test (April 2014)
- Beijing concentrator → MTF7 integration test (May 2014)

Production readiness review, CD-2/3 (May 2014)

Production

- Procurement (June-Aug 2014)
- Board fabrication (July-Aug 2014)
- Board assembly (Aug-Sep 2014)
- Board testing (Sep-Nov 2014)

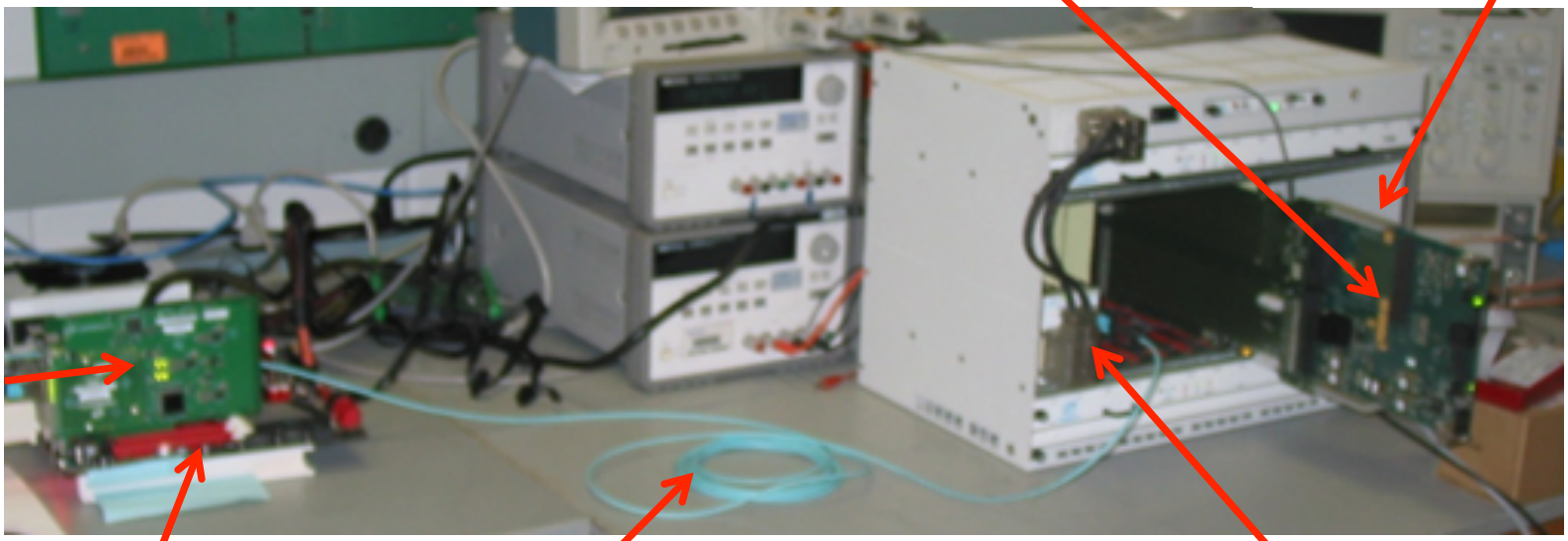
Summary

- First MTF prototypes in hand, testing has started
- Now have prototypes for entire chain MPC -> patch panel -> MTF, next milestone – assembly at CERN
- Improved understanding of BDTs and their optimization, start implementing for CSCTF
  - One last DTTF exercise: min pT(TMVA, private)
- TF algorithm emulator under testing by GEM group
- Monitoring – need to start effort on that side
  - Start from duplicating Run 1 functionality, add features
- Online Software:
  - Summer: D. Rank – first software to combine XDAQ and PCIExpress (hardcoded)
  - Jan 25: G.P. di Giovanni – first integration of PCIExpress into HAL software framework
  - Next – duplicate Run 1 functionality

Closing thoughts

- Overall in pretty good shape
- Key milestone reached: full chain of components available
- Recommend to aggressively pursue moving hardware to CERN, install at PT 5
- Aim to commission as much of the system as possible as early as possible
- Starting Jan 2015, we will need to support 2 systems at the same time
- The sooner we make the switch to the new trigger, the less time and effort we waste supporting two systems
- Need to consider possibility of other muon systems not being ready – new MS to legacy GMT link?

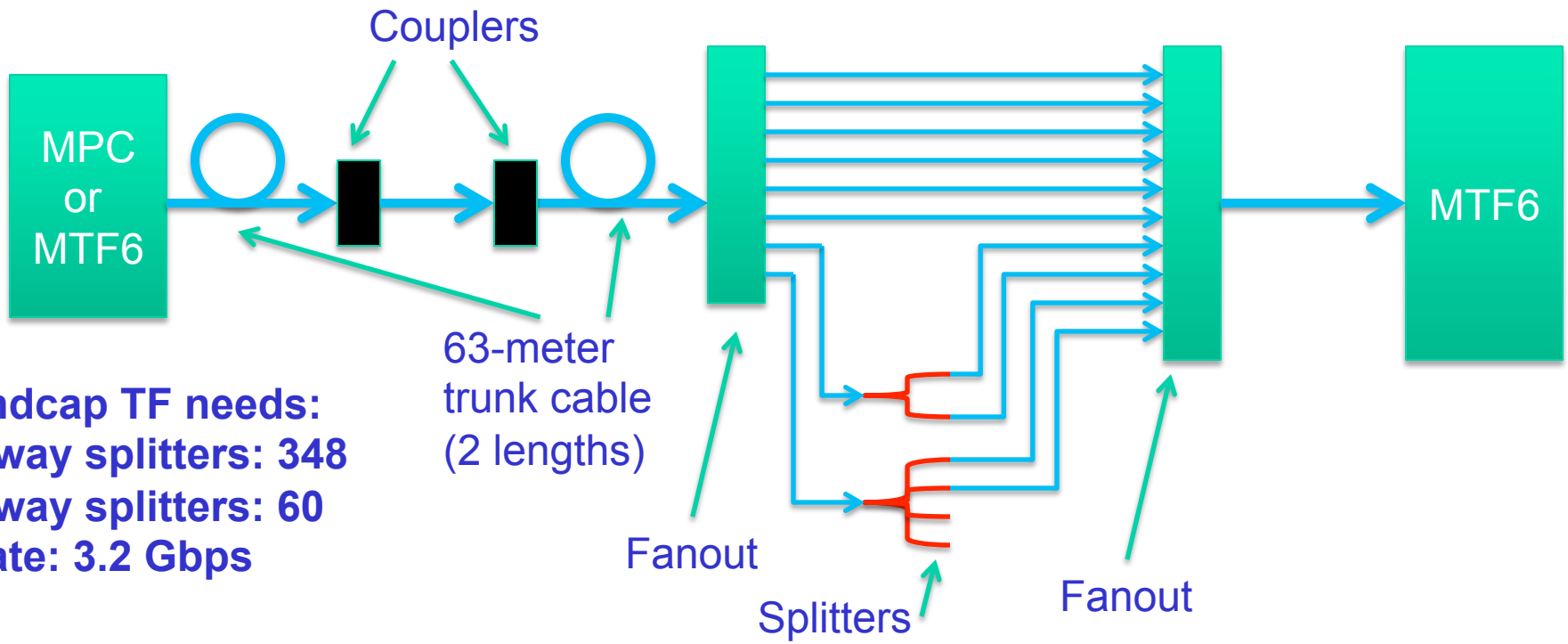
PCI Express tests: Setup



Multiple PC adapters tested →
Best results: HIB35-x4
Also least expensive

Vendor	Card
Vadatech	PCI113
Samtec	PCIEA
OneStopSystems	HIB35-x4

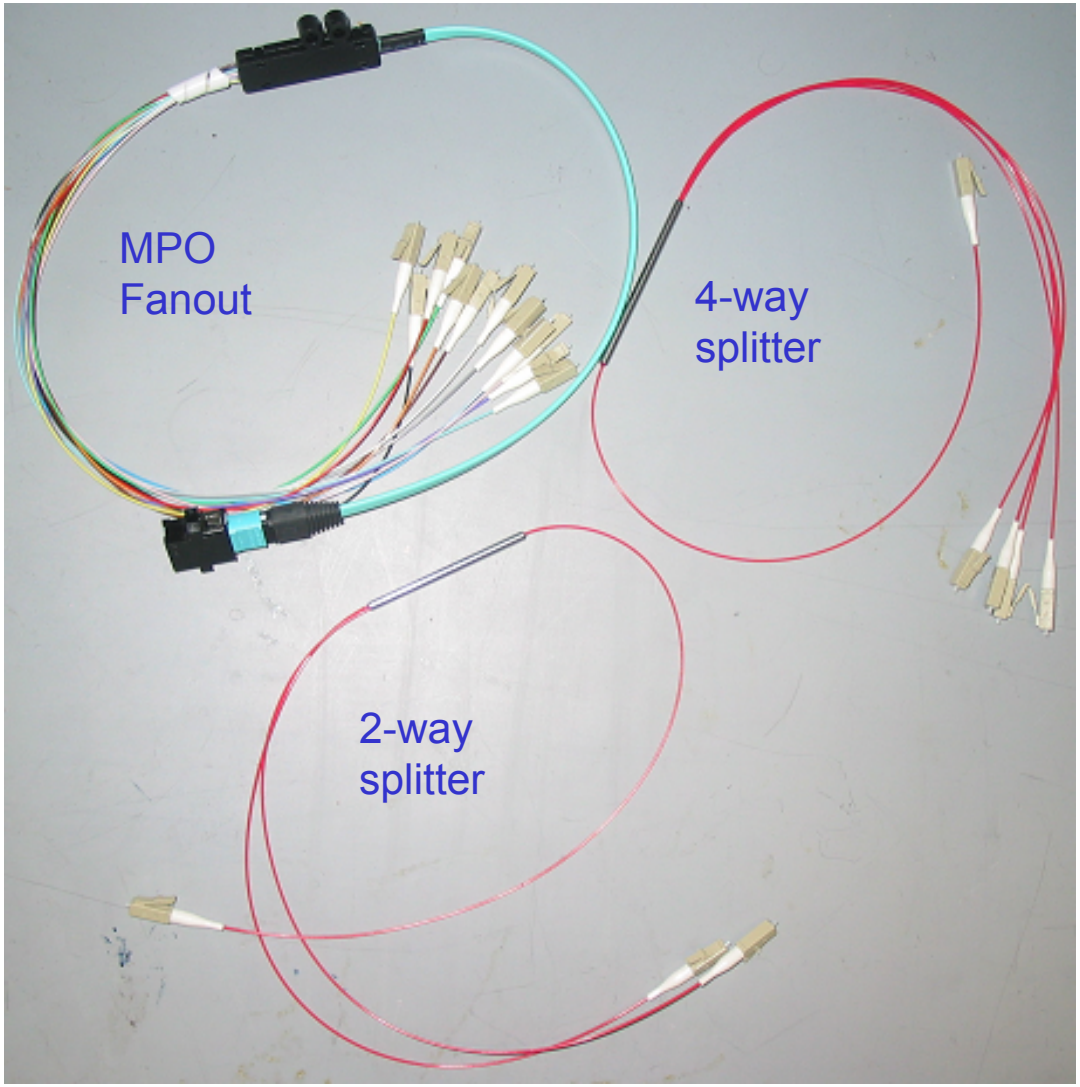
Optical components tests



Endcap TF needs:
2-way splitters: 348
4-way splitters: 60
Rate: 3.2 Gbps

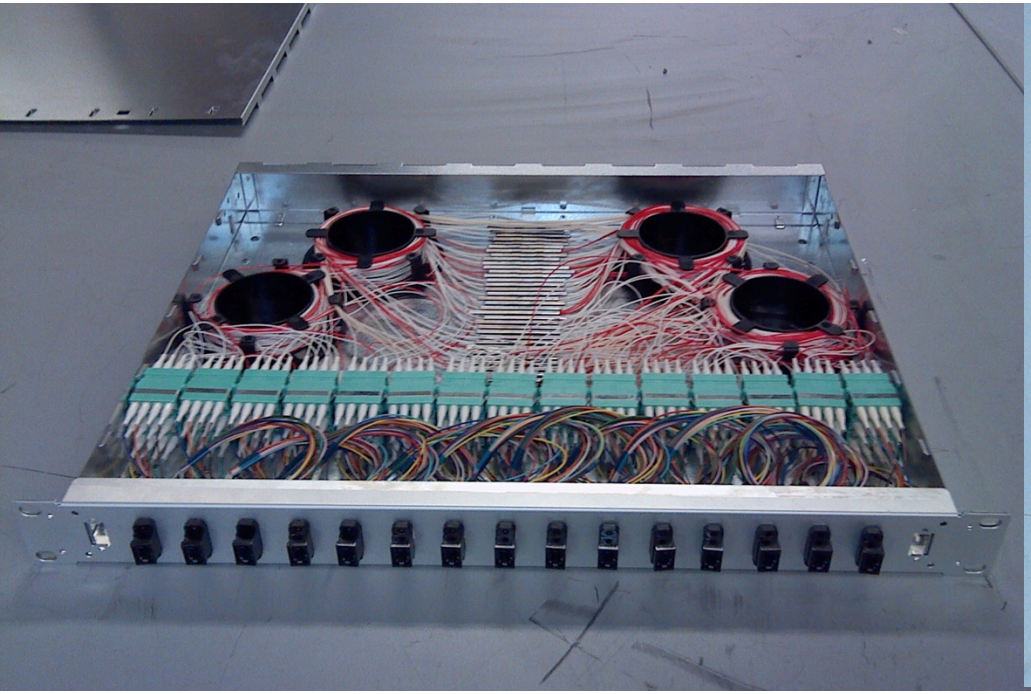
- **Trunk cable identical to what will be used for Endcap TF**
- **Total length (126 m) exceeds actual max fiber length in Endcap TF system (113 m)**
- **Results:**
  - **@3.2 Gbps: no errors with 2-way and 4-way splitting**
  - **@1.6 Gbps: 2-way splitting OK, errors with 4-way**
  - **Newer optical receivers lose efficiency at low bitrates**

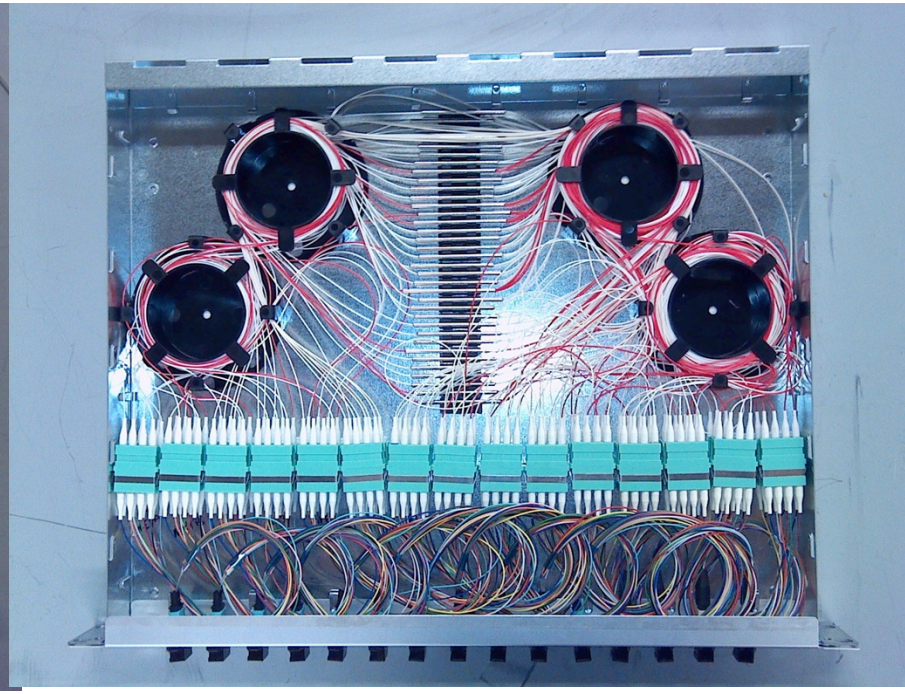
Optical components



Components from Fibertronics

Optical patch panel





- 15x12-core connectors on the user side
- 180 individual optical signals routed inside the patch panel
- One 1U patch panel handles the splitting and routing of optical signals for one sector