Overview of TAMUQ Capabilities and Expertise

Mazen A. R. Saghir

Electrical and Computer Engineering Program
Texas A&M University at Qatar

Texas A&M University at Qatar

- A branch campus of Texas A&M University
  - Established in 2003 in Education City, Doha, Qatar.
  - Offering four undergraduate engineering programs (electrical, mechanical, chemical, petroleum); and a Masters degree in chemical engineering.
  - Approximately 450 undergraduate students; 20 graduate students; and 50 faculty members.
  - Approximately $100 M in research funding (Qatar National Research Fund's National Priorities Research Program (NPRP)) across 140 active projects.

TAMUQ CMS Team

- Faculty Members
  - Othmane Bouhali (Science program; CMS member since 1994)
  - Mazen Saghir (ECEN program)
- Research Staff
  - M. Abi Akl (Ph.D. candidate and physics lab coordinator)
  - Y. Maghrbi (Post-doctoral fellow)
  - A. Castaneda (Post-doctoral fellow)
  - A. Buhmaid, A. Youssouf, S. Abu Salem, W. Sabek (Undergraduate students)

CMS Activities at TAMUQ

- GEM simulation (field map, avalanche, gain, ...)
- Test beam data analysis
- Simulation of mechanical deformations in GEM foils
- Background studies (GE-1/1 station and beyond)
- Non-standard Higgs search
- FPGA design and development
  - Power/thermal management
  - Reliable operations

Research Funding

- Active Projects
  - QNRF funded TAMU-TAMUQ project (2012–2015)
  - UREP funded TAMUQ project (2013–2014)
  - Internal TAMUQ funding (2012–2014)

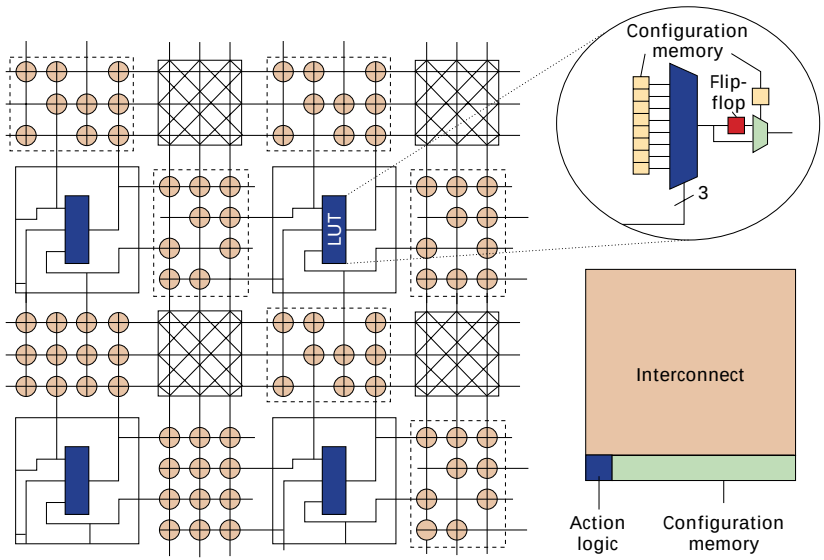
- Future Projects
  - QNRF funding requested (2014–2017)
  - QNRF funding extension (2015–2018)

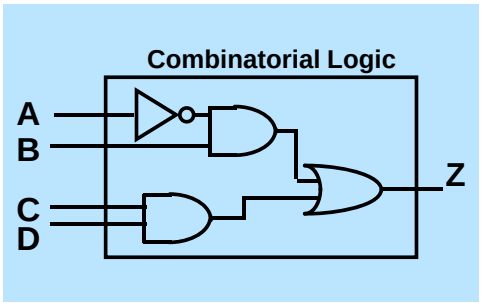
FPGA Primer

- FPGA = **F**ield **P**rogrammable **G**ate **A**rray
  - A programmable logic device that can be used to implement dedicated hardware circuits.
  - Unlike other integrated circuits, FPGAs can be reprogrammed after they have been fabricated.
  - Originally used for circuit prototyping and validation, but today used for full system implementations.

- A FPGA consists of an array of programmable logic cells connected by a programmable interconnection network.
  - Each logic cell is a small memory called a lookup table (LUT).
  - The network consists of wire segments connected by programmable switch boxes.
  - Changing the contents of the LUTs and the switch boxes changes the functionality and organization of the circuits implemented in the FPGA.

FPGA Primer (2)



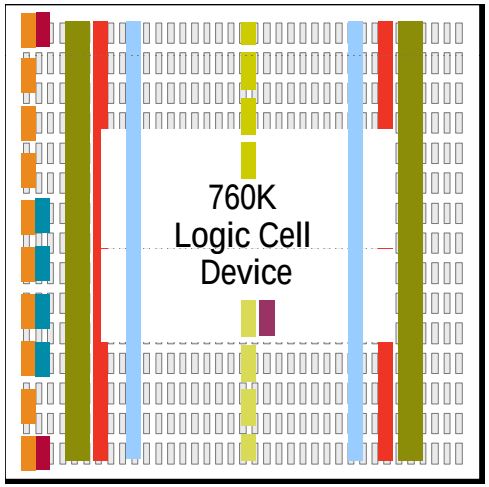


A	B	C	D	Z
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
	.	.	.	
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Contemporary FPGAs

- In addition to programmable logic cells, contemporary FPGAs include a mix of **embedded hardware blocks**.
  - Example: Arithmetic, memory, MAC controllers, fast serial interfaces, etc...
  - Support common applications while using FPGA resources efficiently.

Virtex-6 FPGAs



FIFO Logic
Tri-mode EMAC
System Monitor

Common Resources

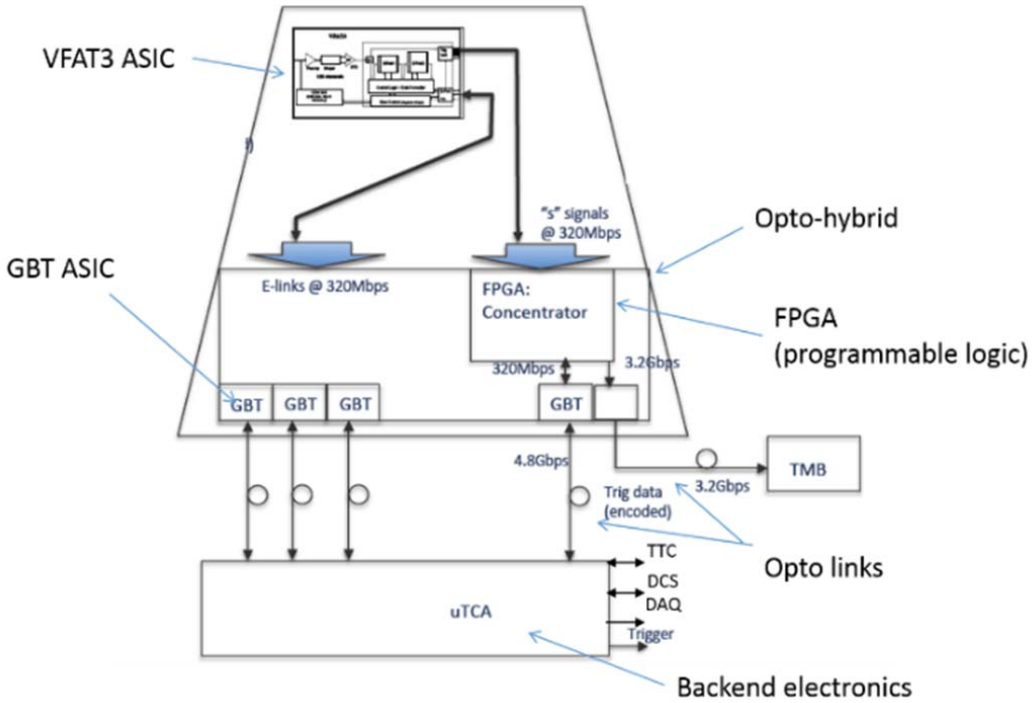
LUT-6 CLB
BlockRAM
DSP Slices
High-performance Clocking
Parallel I/O
HSS Transceivers*
PCIe® Interface

How do we “program” FPGAs?

- FPGAs are programmed using a hardware description language (e.g. VHDL or Verilog).
  - Special tools convert HDL code to a configuration bit stream through a series of steps (logic synthesis, technology mapping, placement and routing)
  - The bit stream is downloaded to the FPGA and used to configure the device.
- A good FPGA designer understands hardware design, FPGA design tools, and the application domain.
  - Not commonly found in computer programmers!

FPGAs in the CMS Experiments

- Format and sort GE-1/1 data from the VFAT2/3 ASICs to produce a complete event stream (e.g. list of hits and their addresses).
- Pre-process data (e.g. hit position coordinate formating) before transmission to uTCA over optical links



Some Challenges

- Performance
  - Over 80 million measurements after each collision at 40 MHz collision rate.
  - Need to identify promising events and reduce event rate to about 100 Hz.
- Power consumption and thermal management
  - High complexity designs consume more power and generate more heat.
  - Limited space in CMS chambers for heat dissipation equipment
- Reliability
  - High radiation environment can cause transient single-event upsets (SEUs) that cause FPGAs to malfunction.

Possible Solutions

- Performance
  - Develop highly optimized parallel algorithms that can operate on partial data.
- Power consumption and thermal management
  - Select appropriate voltage-scaled FPGA devices that balance data processing and power needs.
  - Apply low-power FPGA design techniques (e.g. clock gating and multiple clock domains to reduce dynamic power; embedded hardware blocks to reduce area and static power).
- Reliability
  - Use periodic bit scrubbing to refresh SEU-prone circuits. Scrubbing rates can be determined from irradiation tests.

TAMUQ Roles

- Working closely with TAMU-CS to develop solutions and prototypes for Slice Test (2016–2017) and full installation for LS-2 (2018–2019)
  - FPGA device selection and board design
  - Algorithm development and optimization
  - Exploring suitable power-aware and SEU mitigation designs
  - Irridation studies
  - Power consumption and SEU mitigation studies.

FPGA Resources at TAMUQ

- State-of-the-art lab facilities
  - Latest FPGA development boards (Xilinx Zynq and Virtex-7) and software design tools (Xilinx ISE, EDK, Vivado)
  - Central Electronics Shop with 8-layer PCB fabrication and electronic component soldering capability.
  - Digital oscilloscopes and power measurement instruments
- BEECube BEE4 prototyping board.
  - 4 Xilinx Virtex-6 FPGAs
  - Ideal for large system prototyping and development.
- Convey HC-2ex blade
  - Hybrid computing platform (Quad-core Intel Xeon + 4 Xilinx Virtex-6 FPGAs)
  - Ideal for scientific computing applications.

Thank you!

Questions?