CSC Endcap Muon Port Card Status

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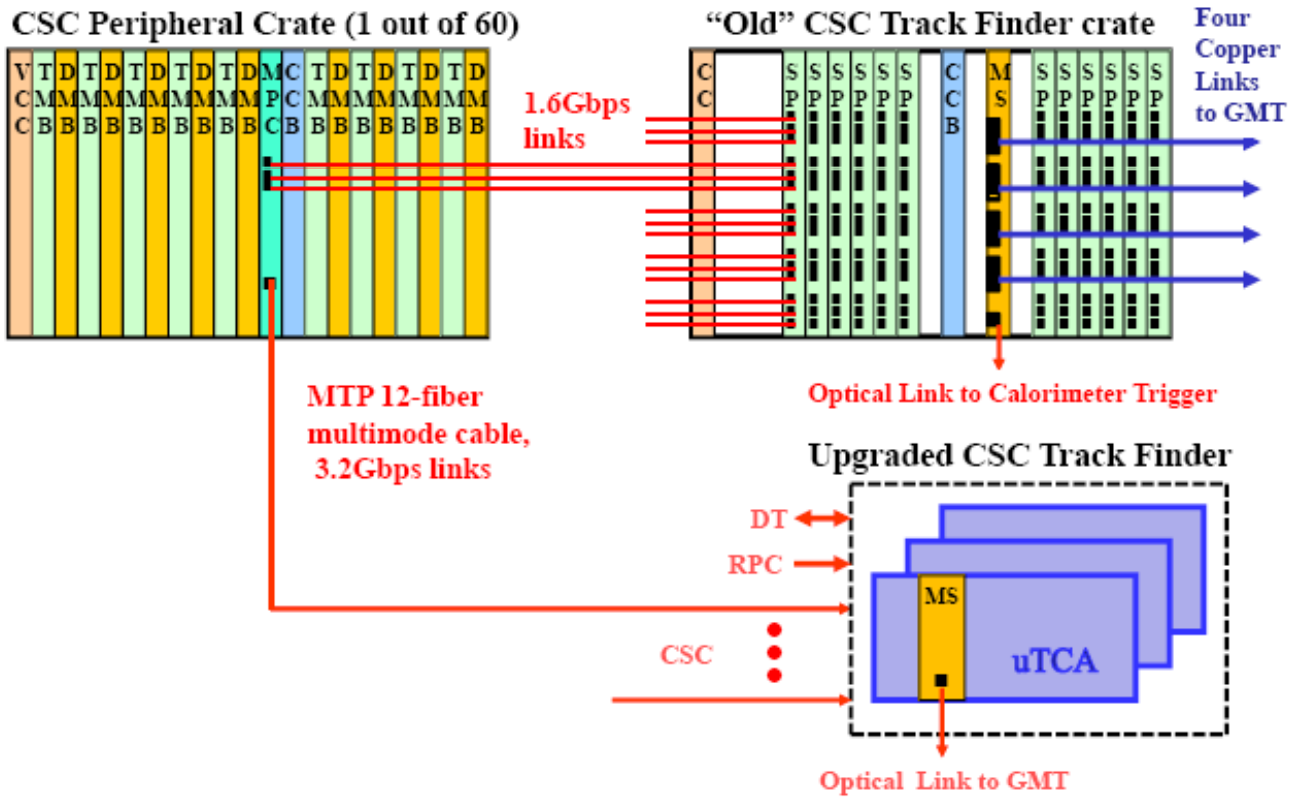
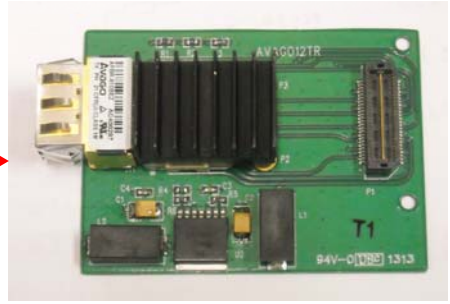
MPC Upgrade Goals



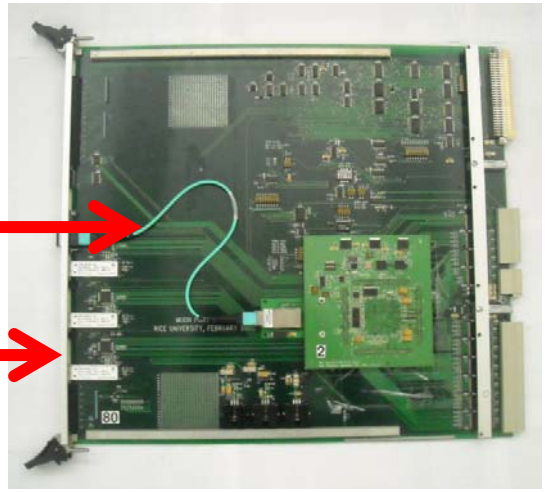
- Be able to deliver up to 18 trigger primitives from the EMU peripheral crate to the upgraded Sector Processor
- Preserve sorting capabilities of the Muon Port Card
- Preserve 3 old 1.6Gbps optical links to the existing CSCTF

Muon Port Card Status

- 85 optical transmitter boards have been fabricated and assembled in October. Based on Avago AFBR-810 transmitter

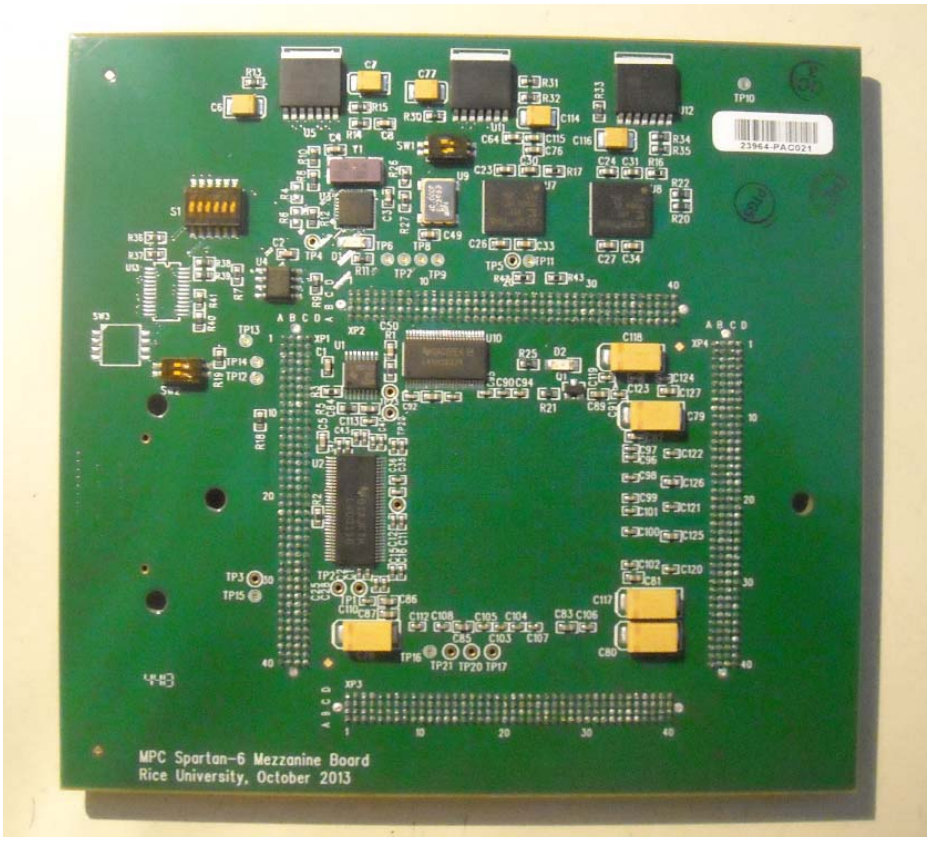


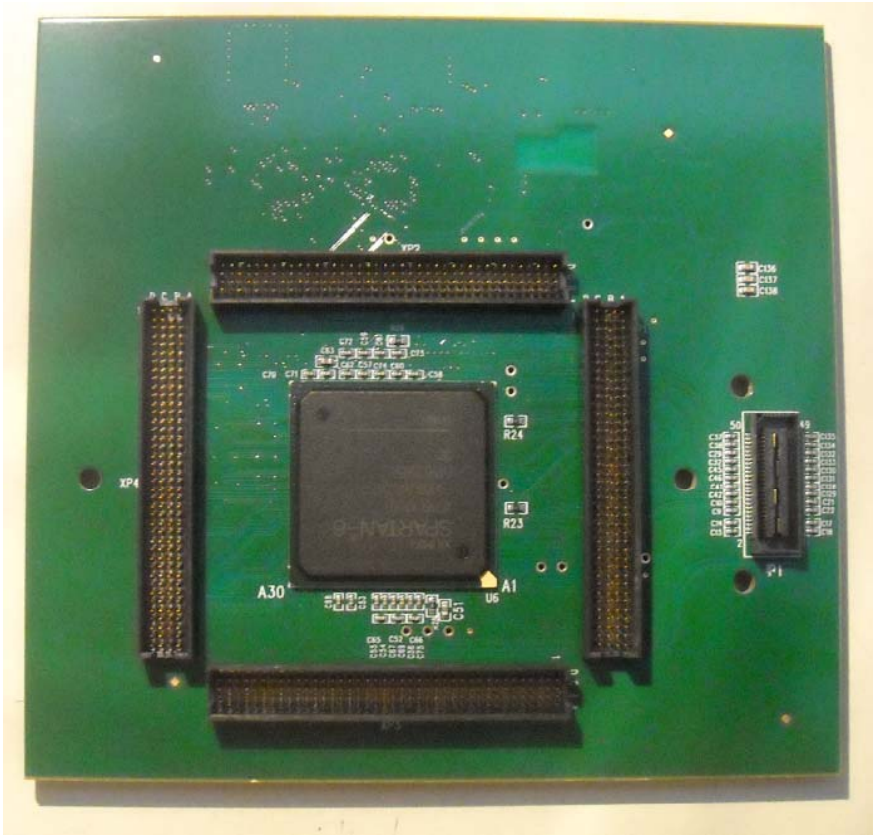
- Received 90 optical pigtails from CERN in November
- Fabricated 81 new front panels (we have 81 baseboards)



- All 84 pluggable optical transmitters from Avago have been received (delayed by 1-2 months)
- 85 assembled Spartan-6 mezzanines arrived from Pactron on Jan 6

MPC Production Mezzanines

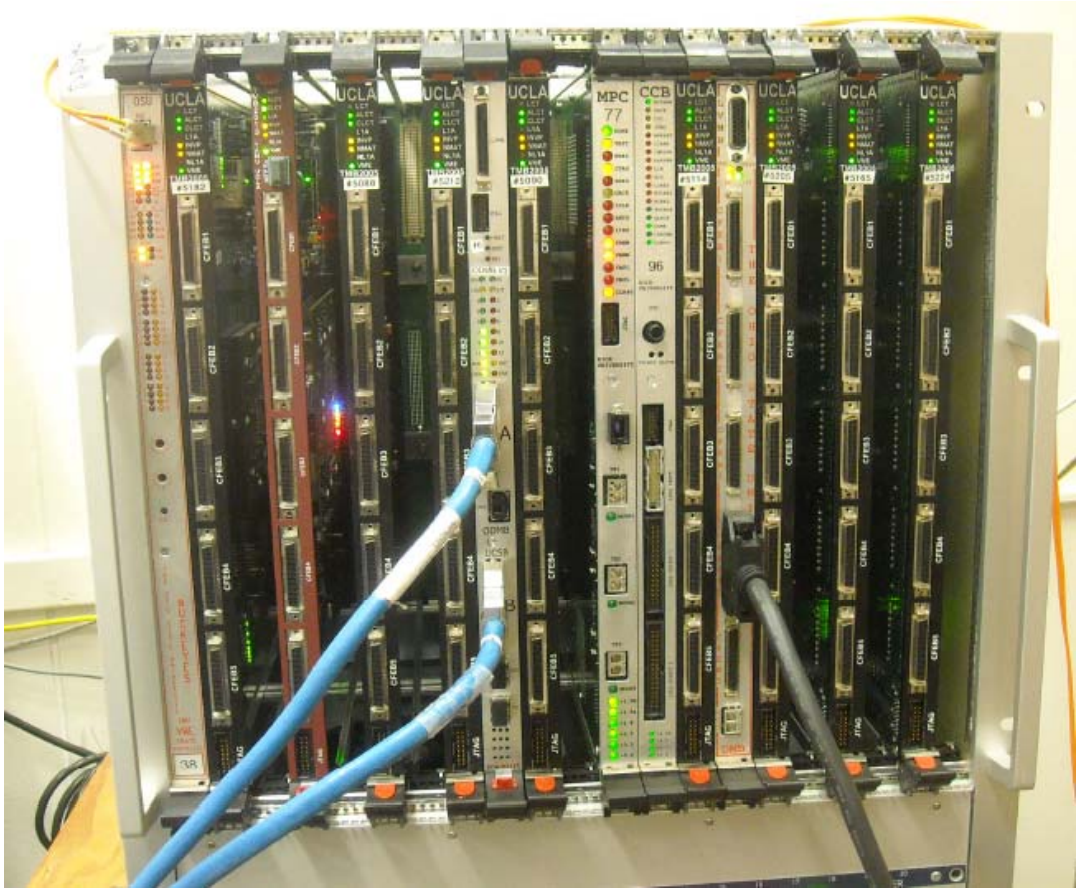




Muon Port Card Testing Step 1

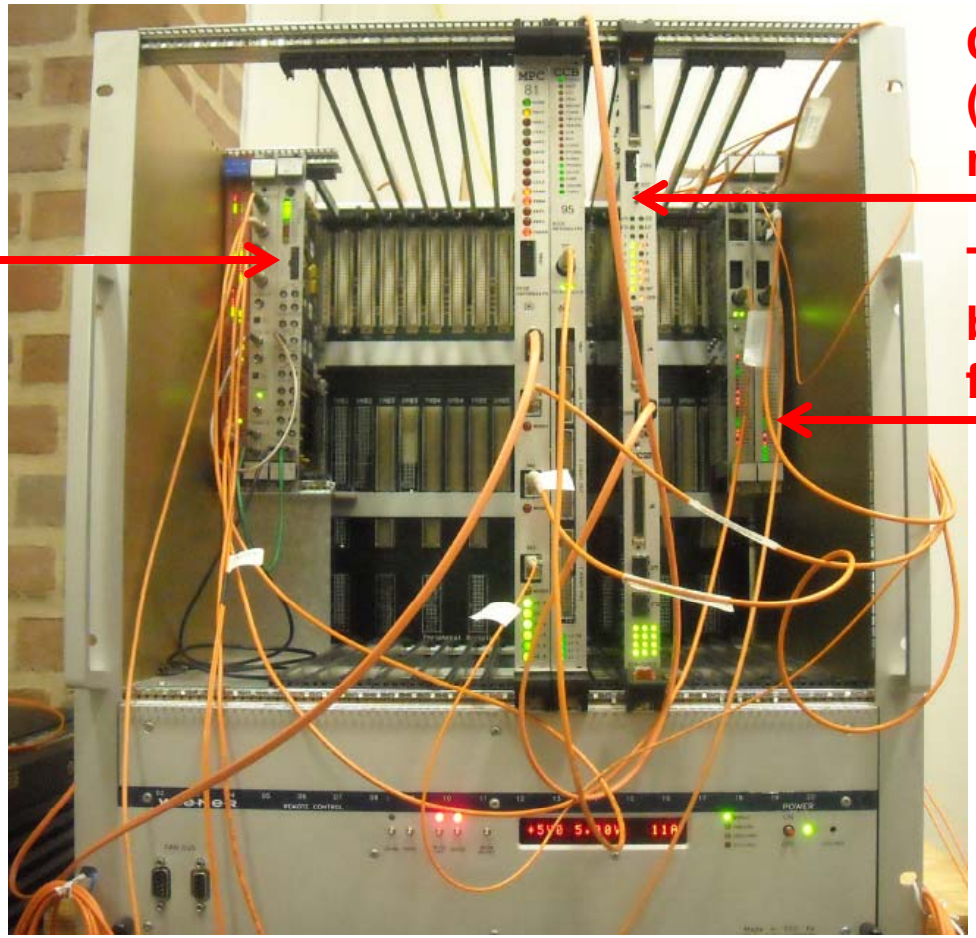
- Program two XCF32P PROMs via Xilinx JTAG cable
- Check QPLL, clocks and other critical test points with a scope
- Run basic VME write/read test

Muon Port Card Testing Step 2



- Run “9 TMBs - to - MPC” data transmission test in the fully loaded EMU peripheral crate. Verify “safe window” of data latching. This test allows to check most of the FPGA inputs and outputs.

Muon Port Card Testing Step 3



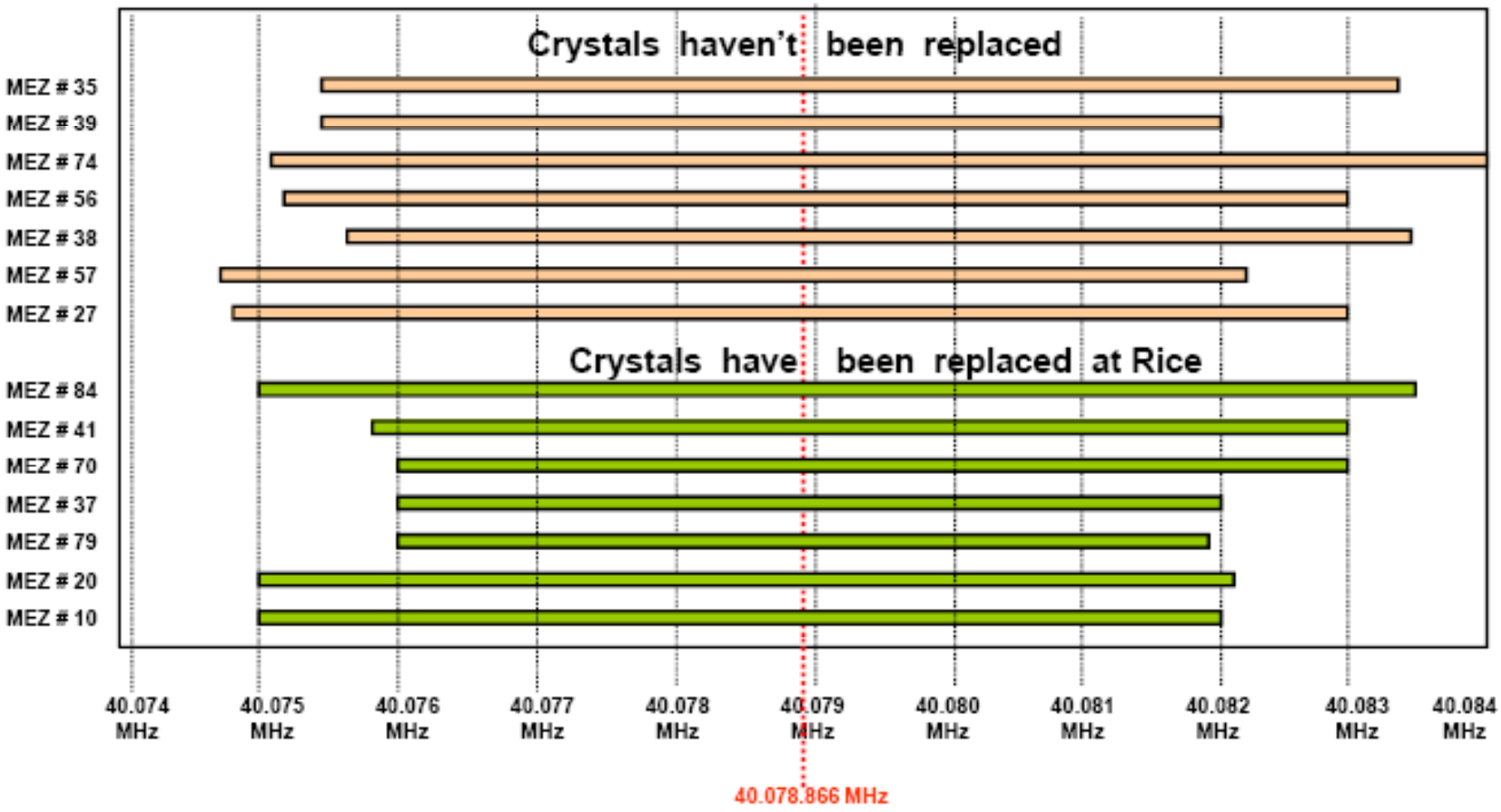
- Run optical data transmission tests of three old" and 8 "new" links (PRBS and random patterns, verification under VME control)

Progress and Issues Discovered

- Quality of PCB assembly is very good
- 2 out of 84 Avago 12-channel optical transmitters had problems
- 1 out of 85 QPLL3 was replaced
- 42 out of 85 custom 160.314MHz crystals have been replaced (symptoms: QPLL doesn't produce 40M/80M/160M clocks or/and doesn't lock). All replacements work well. Seen similar problem with the UCSB ODMB ver.3 boards (3 out of 10 crystals were replaced).

  Response from Pactron: ***This part used on Rice and UCSB projects are very low MSL (Moisture Sensitivity Level) parts which are sturdy. We re-visited the thermal profile that was used to build these boards and they look very nominal. The part is a RoHS compliance part which can withstand 260°C peak max reflow temperature – our reflow peak temperature was about 235°C (reflow profile attached). Since we are seeing this failure across 2 projects and the parts came from the same source – it would be good to send the failed devices to the factory for failure analysis.***

QPLL Locking Range



Optical Tests

New optical data transmission format

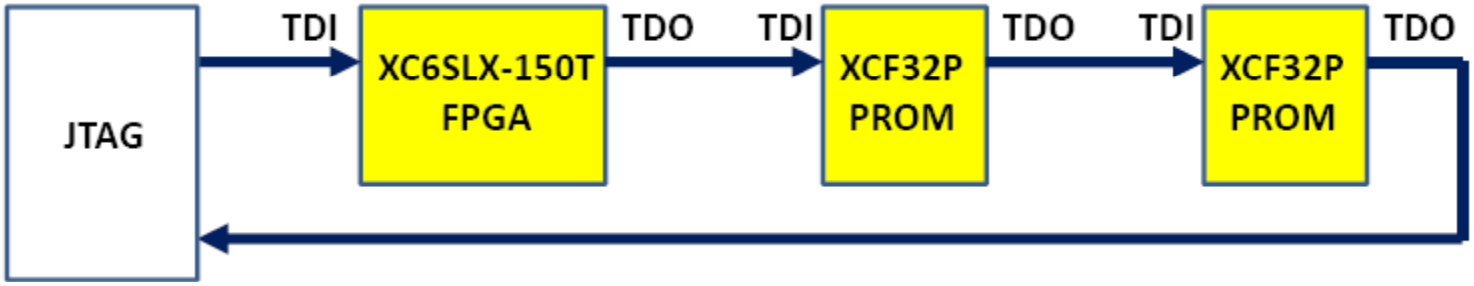
Fbr	CSC	Frm	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	2+1	0	1	Wire Group1							Half-Strip1							
		1	0	Wire Group2							Half-Strip2							
		2	0	SE	BX0	BC0	VP2	VP1	LR2	LR1	CLCT Pattern1				Quality1			
		3	0	Wire Group1							CLCT Pattern2				Quality2			
2	3+1	3	0	Wire Group2							CLCT Pattern2				Quality2			
3	4+1	3	0	Half-Strip1[6:0]							CLCT Pattern2				Quality2			
4	5+1	3	0	Half-Strip2[6:0]							CLCT Pattern2				Quality2			
5	6+1	3	0	HS1 [7]	VP1	LR1	Quality1				CLCT Pattern2				Quality2			
6	7+1	3	0	HS2 [7]	VP2	LR2	Quality2				CLCT Pattern2				Quality2			
7	8+1	3	0	SE	BX0	BC0	CLCT Pattern1				CLCT Pattern2				Quality2			
8	9+1	3	0	Spare			CLCT Pattern2				CLCT Pattern2				Quality2			

Bit Error Rates

Test	BER per link, 3 "old" 1.6Gbps optical links, 2 x 100m + 1 x 10 m fibers	BER per link, 8 "new" 3.2Gbps optical links, 8 x 100 m fibers
PRBS	$< 2x10^{-13}$ (PRBS-7)	$< 10^{-13}$ (PRBS-7, PRBS-15, PRBS-31)
Random patterns	$< 4x10^{-10}$	$< 1.6x10^{-10}$

Firmware

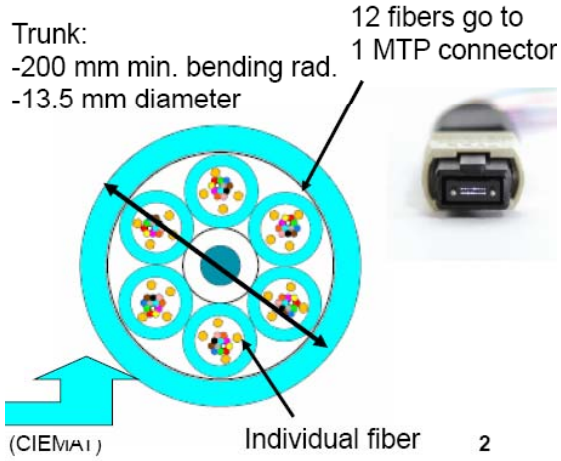
- Xilinx ISE 13.4 development system
- ~40 minutes to implement the project
- Present design occupies ~25% of the Spartan-6 resources, all 8 existing GTP links are used
- Specification is available at http://padley.rice.edu/cms/projects.html#mpcmez3
- 2 XCF32P PROMs (direct access via JTAG); Master SelectMAP mode (clock provided by the FPGA)



- It takes ~17 minutes to program mezzanine PROMs via the VME bus
- FPGA reload from PROMs (dead time):
  - 156 milliseconds (FPGA internal 26MHz oscillator)
  - 108 milliseconds (external 40MHz oscillator on the mezzanine card)

Optical Cables for P.5

- Trunk cable with 4 connectorized cords (similar to one proposed for the DT upgrade). Each cord has 12 fibers. Need 36 cables for 60 peripheral crates, one spare cord per crate. All details in the Technical Note
  CERN EDMS No. 1296847, Reference ELG-OPTFIB-EN-0007



- Purchase order ($81.3K CHF) has been placed through CERN in April 2013. All cables (27 100 m long cables and 9 100+m ones) are at CERN. Installation by a CERN team is being planned.

- Example of the proposed labeling: CSC/MPC+/1/2-3/S1D05/X5U41
  (YE+, Sector 1, Station ME2 and ME3, start rack S1D05 end rack X5U41)

Plans

- Expect to get a uTCA hardware from UF next week. Purchased a new PC (same Dell PowerEdge R320 as being deployed at CERN).
- Have 7 baseboards at Rice and received 5 MPCs from CERN (904) on January 31st. We have 12 upgraded baseboards in total, 8 of them shipped to CERN on February 5. Full link test at this moment is possible only at Rice.
- Run a slice test with 5 upgraded MPCs at p.5 (verify QPLL locking, old optical links) before full installation. Need to be able to read out the CSCTF.
- Installation of all mezzanines at p.5 in late spring - early summer
- Installation of 36 new optical cables in spring

Backup Slides

Optical Power Budget

■ To calculate the worst-case estimate of power budget (P_B), one needs to subtract the minimum receiver sensitivity (P_R) from the transmitter power (P_T): $P_B = P_T - P_R$.

■ For the Avago AFBR-810 transmitter the P_T = -1.5dB and for the AFBR-820 receiver P_R = -11 dB at 10Gbps rate. Our links operate at a lower rate of 3.2Gbps where the estimated P_R = -13 dB. Then P_B = -1.5dB – (-13dB) = 11.5dB

■ After calculating a link's power budget one can calculate the power margin (P_M), which represents the amount of power available after subtracting attenuation or link loss (LL) from the power budget (P_B).

- The average LL values are 0.5dB for connector/splice;
- Higher-order loss in MMF of 0.5dB;
- Fiber attenuation of 1dB/km.

We expect to have one either 2- or 4-way passive splitter along the optical distribution tree. 2-way splitter means 10log(0.5) = -3dB loss and a 4-way splitter means 10log(0.25) = -6dB loss. Assuming 6 connectors/splices in our link and one 4-way splitter we have:

$P_M = P_B - LL$ = 11.5dB – 0.5dB x 6 – 0.5dB – 0.1dB (100 m fiber) – 6dB = 1.9dB

A P_M greater than zero indicates that the power budget is sufficient to operate the link.

Irradiation Tests (Summary)

XCF32P PROM

- Irradiated with 1 MeV equivalent fluence at ~10.5 *10^{12} n/cm^2 at the TAMU cyclotron in April 2013
- Equivalent to ~30kRad, or 30 years of LHC exposure in ME1/1 area
- Device was read back; not a single bit change, as expected

XC6SLX-150T FPGA

- Irradiated at the UC Davis 66 MeV proton cyclotron in April 2013
- Irradiated with 1 kRad at a rate of ~1 Rad/sec (convenient to detect SEU):
  - 5 to 15 seconds between SEU
  - Average dose to get an error ~13 Rad. With the accumulated fluence of 3*10^{11} protons/cm^2, the cross section of SEU is 75 / 3x10^{11} = 2.5x10^{-9} cm^2
  - Assuming 10-year fluence of ~10^{11} neutrons per cm^2 [1] at full LHC design luminosity, the worst case SEU rate would be 2.5x10^{-9} cm^2 x 10^{11} neutrons/cm^2 / 5x10^7 sec = 5x10^{-6}, or 1 SEU in ~ 5.5 hours per device [1] http://cmsdoc.cern.ch/~huu/tut1.pdf
- Irradiated with 100 kRad at a rate 360 Rad/sec
  - Many upsets
  - FPGA survived the test

Avago AFBR-810 optical transmitter

- Studied by the SMU group (Dallas TX) in 2012-2013, reports available
  - Survived up to 150 kRad
  - SEU rate was comparable with the one for SNAP12 devices (being used on ODMB and OTMB boards)