Summary of SciFi electronics review

16^{th} January 2013

Review report

Electronic Review (held on the December 11, 2013)

https://indico.cern.ch/conferenceDisplay.py?confId=285938

Reviewers : Federico Alessio (CERN), Luciano Musa (CERN), Jose Francisco Toledo (University Valencia), Ken Wyllie (CERN)

General comments (a few extracts)

- The proposed SciFi FE architecture is compatible with the global upgrade architecture
- The proposed implementations all seem feasible but many parts of the design are still very preliminary
- Some important technical decisions still have to be taken and other aspects of the design cannot start until these are defined
- The system performance should be simulated together with the TELL40 code and the TFC commands
- No potential "shows-stoppers" were observed, but there are some items whose development and verification is critical for the schedule
- The SciFi group is asked to converge on the final quantities of common components (GBTX, VTTx/VTRx, GBT-SCA, DC-DC convertor, ST linear regulator)

Since the review: PACIFIC (SciFi Front End Chip)

A few extracts from the PACIFIC section:

- The PACIFIC design is advancing well
- A complete set of specifications is missing and should be compiled immediately
- The preparation for testing should be carefully planned and scheduled, and manpower identified
- The precise bias circuit that will be used for the SiPMs was not shown in the meeting and is not described in the documentation
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- we propose that the SiPM short-circuit failure mode is taken into account in the design
- The sensitivity of the PACIFIC design to power supply noise (power-supply-rejection ratio) should be carefully simulated
- The electrical characteristics of the flex cable between PACIFIC and the SiPM should be extracted and included in the model used for simulating the front-end

1st PACIFIC prototype

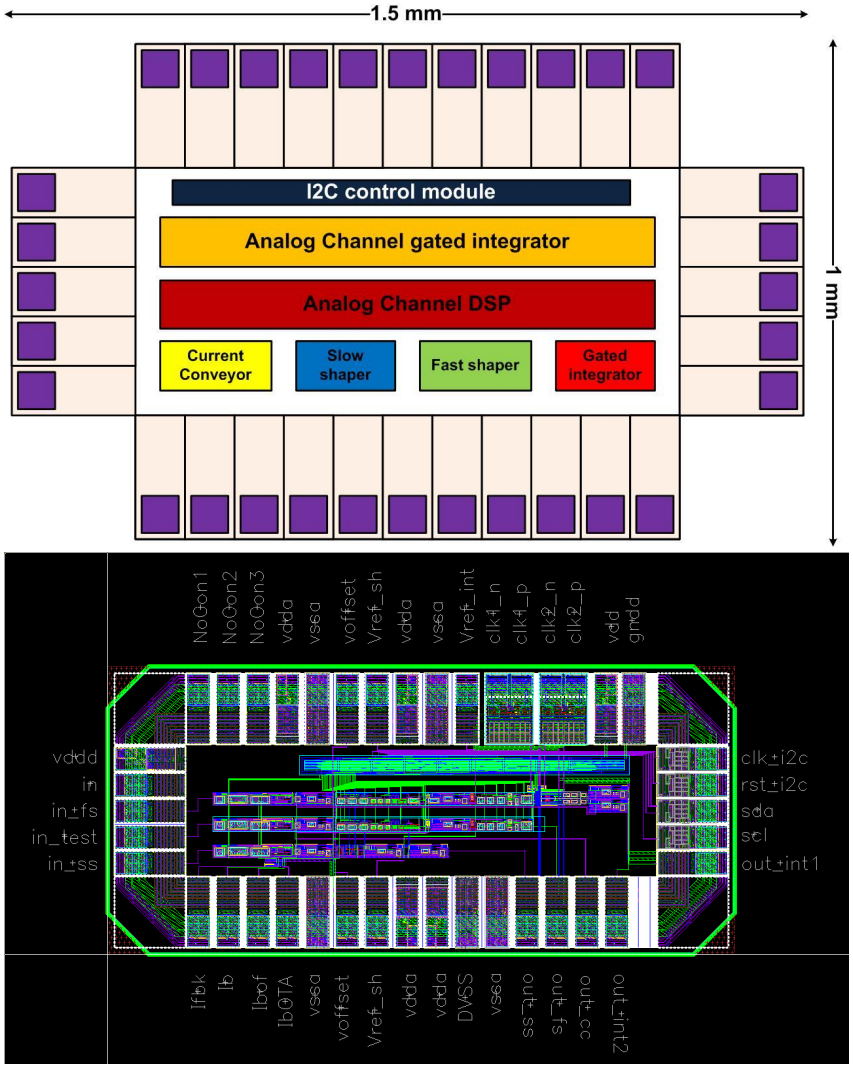

Figure : PACIFICr1

- Submitted the 18th of November via CERN and MOSIS (Laboratoire de Physique Corpusculaire (Clermont-Ferrand), Institut de Ciències del Cosmos (Barcelona), Instituto de Física Corpuscular (Valencia), and Ruprecht-Karls-Universität Heidelberg)
- Final size:0.872x1.902mm
- Prototypes received in January
- Tests ongoing

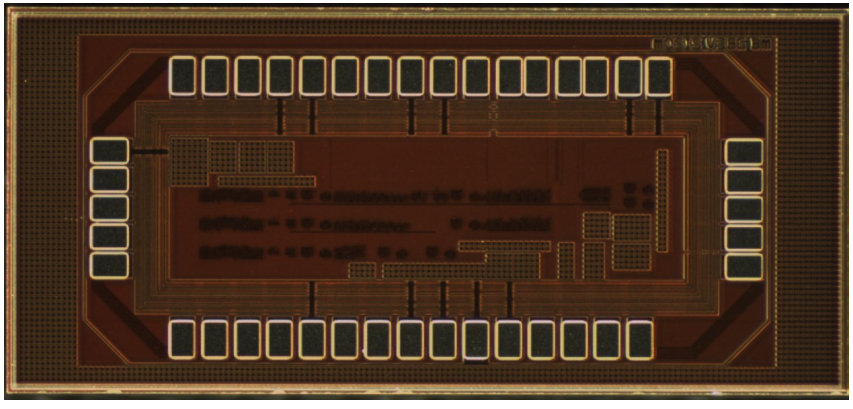

Figure : PACIFICr1

Since the review: Choice of the digitization scheme

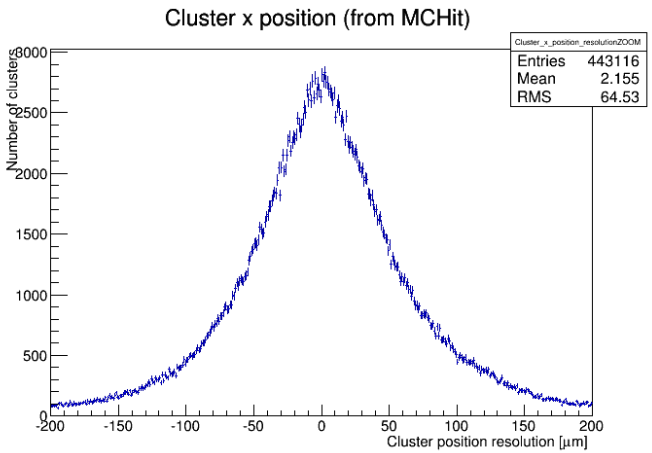

Figure : Hit resolution (linear 6 bits)

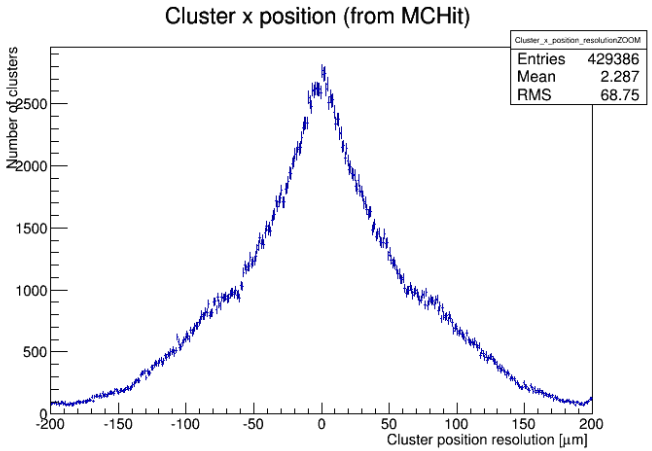

Figure : Hit resolution (non-linear 2 bits)

Study

- Resolution of the hit position with 6 bits digitization (linear scale) and 2 bits digitization (non-linear scale)
- Geant4 simulation
- No spill-over
- Study with 4×10^6 clusters
- Resolution computed as the mean channel position from hit - mean channel position from clustering
- Thresholds used:

Neighbour	Seed	High	Sum
1.5PE	2.5PE	4PE	4PE

Results

6 bits digitization:

- RMS hit resolution: $64 \mu m$

3 thresholds (2 bits):

- RMS hit resolution: $69 \mu m$

Both case shows a resolution bellow the required $100 \mu m$

$\Rightarrow$ 3 Thresholds (ease the PACIFIC design)

Since the review:PACIFIC design

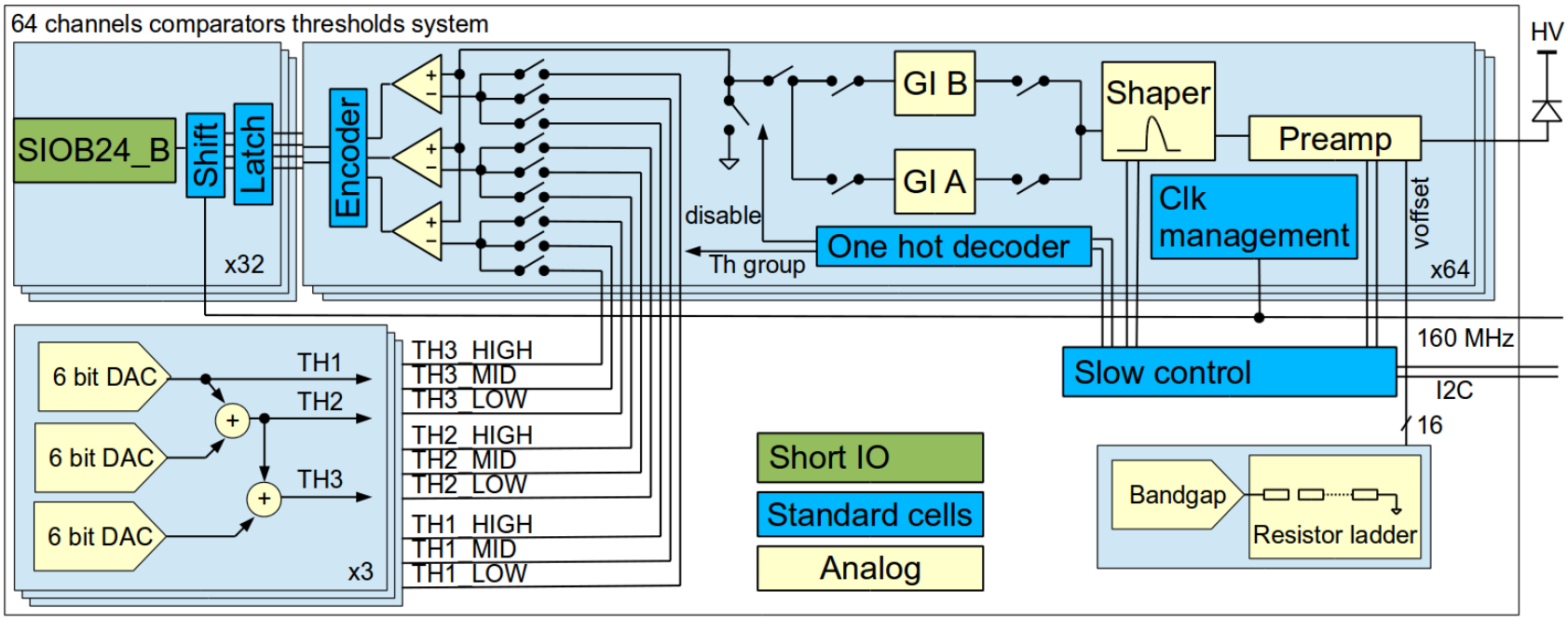

Figure : PACIFIC design

All the choices have been made:

- Fast shaping with gated integrators
- 2 bit non-linear digitization scheme
- Common thresholds/64 channels
- Per channel voltage control

From the review

A few extracts from the FE section:

- The modularity of the FEB should be rationalised (PACIFIC and clustering FPGA on different PCB)
- The use of commercial-off-the-shelf components in the FEBs must be assessed carefully together with the expected radiation levels in the environment
- The SciFi group are reminded to consider operational aspects as part of the decision process, for example the impact on the down-time of the system if SRAM-based FPGAs (and memory scrubbing) are considered
- single-ended I/O may require SSTL signaling due to the high data rate (128ch x 6 bit x 40 MHz makes approximately 30 Gb/s). Simultaneous switching noise may become a concern. Alternatively, LVDS or other gigabit-per-second differential standards may reduce the switching noise but also increase the I/O count
- the required buffer size in the FPGAs has not been defined yet. Simulations that include worst case events must be carried out
- The SciFi group should carefully study and document the clock distribution on the FEBs. Multiple clocks will be required.
- A point-of-load power distribution approach would be advisable and so extra board area should be considered for the small readout board
- The general power and grounding scheme of the FEB should be studied, including the different possibilities for local regulation
- Work on the concentrator algorithms has not yet started. It is recommended that this is done together with development of the AMC40 firmware to arrive at an efficient and cost-effective solution for both ends of the link.
- The low-voltage power supplies currently used for the Outer Tracker can be used for the upgrade. However, it is not yet certain if the quantity is sufficient

Front-end board design

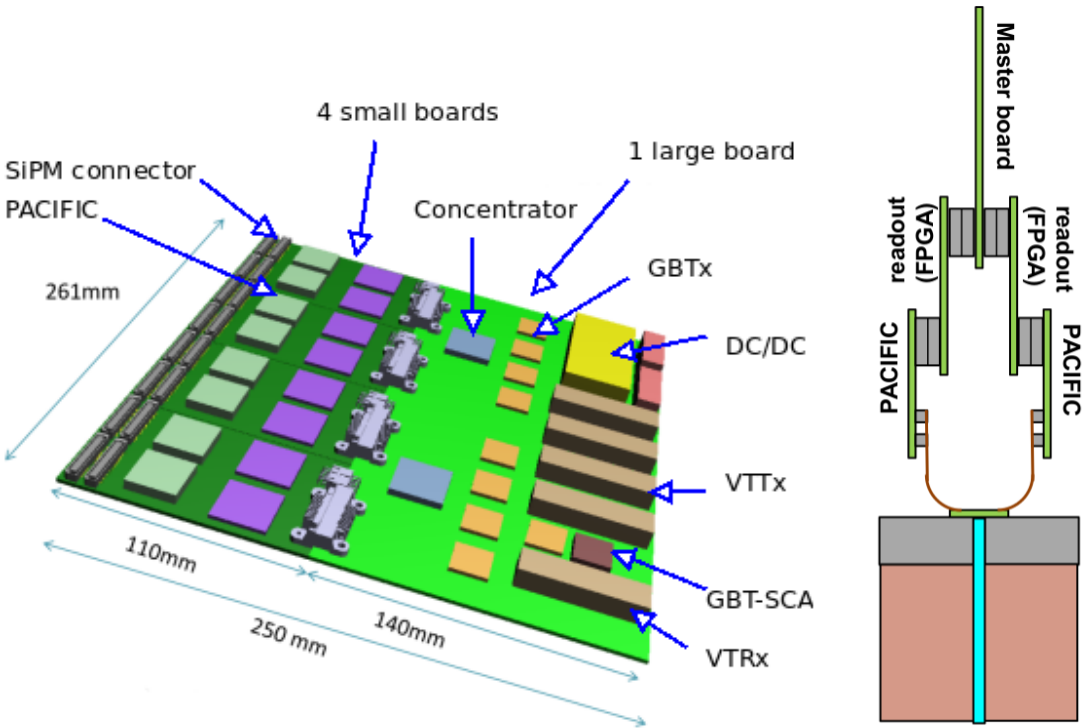

Figure : Possible front-end board design (*Magali and Wilco*)

Since the review

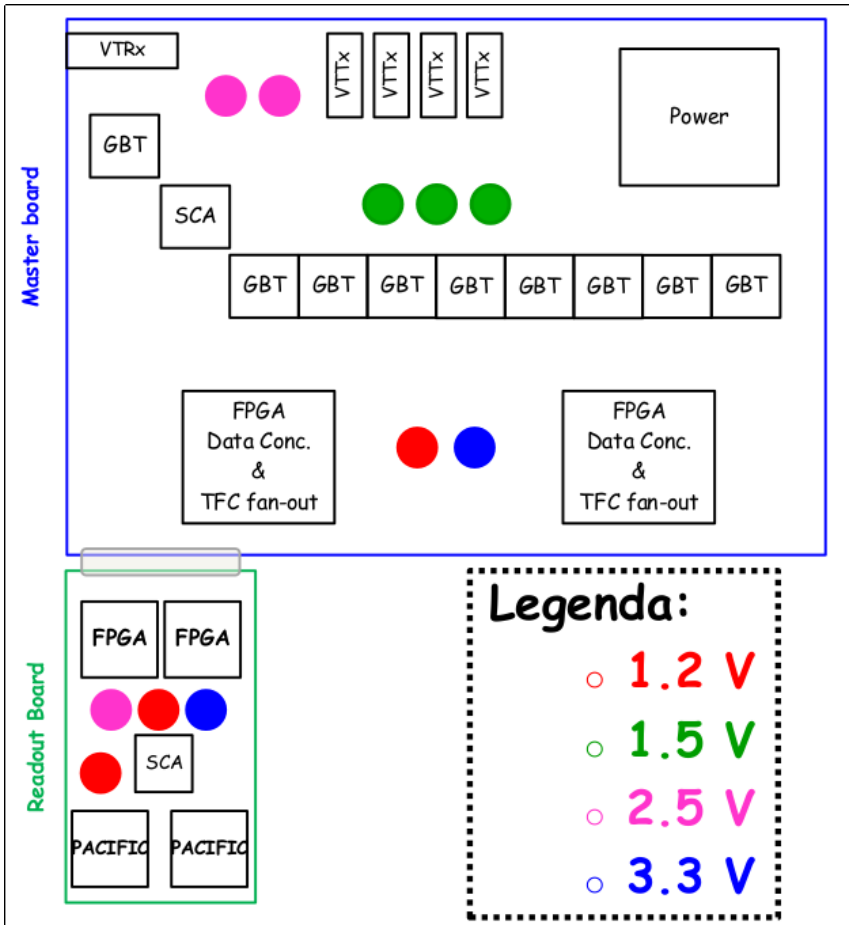

Figure : Possible front-end board powering scheme (*Antonio and Wilco*)

- FE board powering scheme design is ongoing
- Far from final (measurement with DC/DC converters needed)
- A batch of DC/DC from the pre-production will be ordered

From the review

A few extracts from the manpower & planning section:

- The schedule was presented. This meets the experiment schedule but is aggressive and depends very much on the PACIFIC. It is recommended that resources are optimised to minimise the development time of the PACIFIC as much as possible.
- The next chip submission in May 2014 is planned to have 8 or 32 channels. A submission with the full 128 channels would follow later. The reviewers recommend that the SciFi group carefully consider the option of immediately designing the full 128-channel version.

New PACIFIC development plan:

- 8 channels chip in May (test the analog channel and the digital processing)
- Switch to TSMC 130nm
- 8 in Q4 2014 or 128 channels in Q1 2015

Since the review: Test planning

The Conclusion of the *PACIFIC tests meeting* on Jan.10th 2014 @ Clermont Ferrand :

Step1

PACIFIC1 Card

- A simple PCB with PACIFIC1 bonded directly on it;
- All the pads can easily be accessed by test points and soldering pads ;
- An on-board test pulse injection circuit & necessary peripheral circuits;
- Connectors for further SiPM array connection and digital IOs.

Based on the electrical performance test result, a more integrated & complicated PCB

Step2

TEST Motherboard

- Regulators for fixed power supplies and DC voltages;
- on-board ADC;
- SiPM Array connector;
- IC + small FPGA for PACIFIC1 readout and configuration;
- ? ....

Just ideas, we DO NEED the result from Step 1 to decide ....

Figure : PACIFIC test bench (*Snow*)

1st PACIFIC prototype test

Secondary pcb provides control of:

- I2C DACs for voltages setup
- I2C control of channel registers
- I2C clock and reset
- 20MHz clocks for integrators

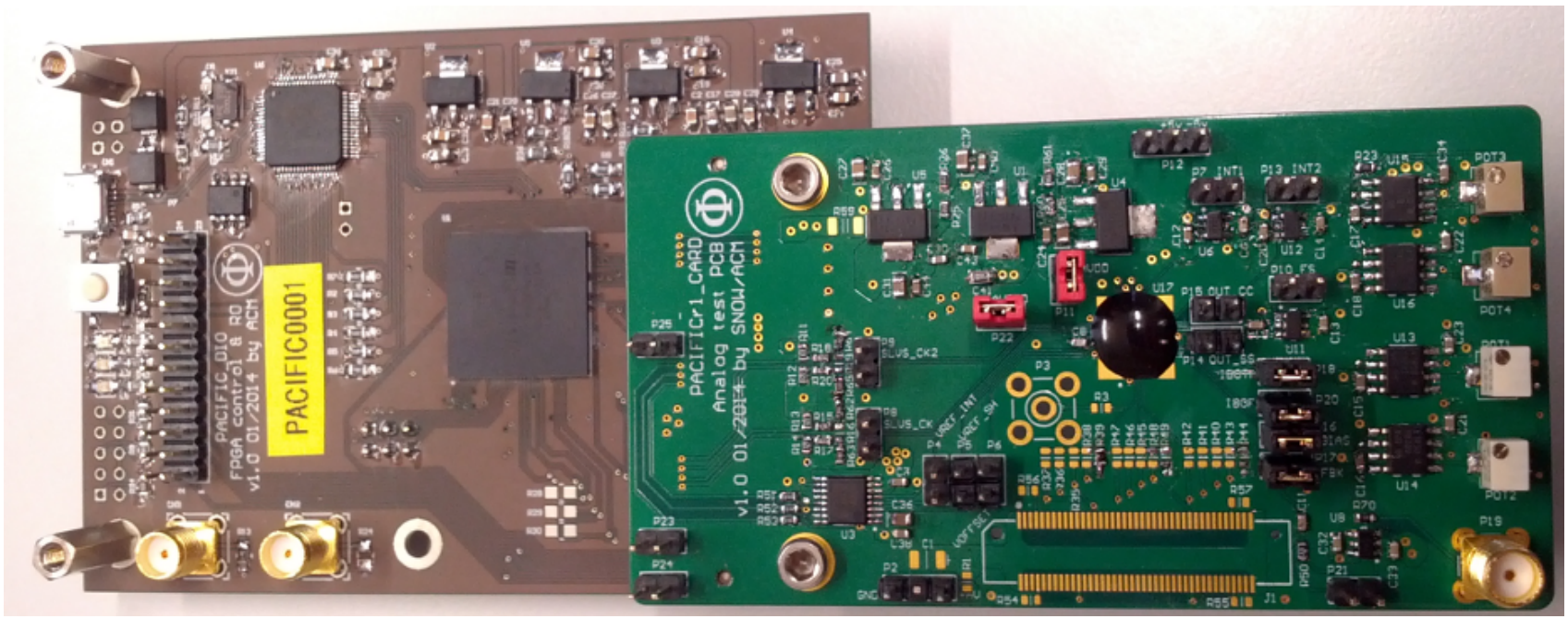

Figure : PACIFIC 1 test bench

1st PACIFIC prototype test

First results: Gain and pole-zero cancellation parameters

- Works as expected

Test of the gated integrator ongoing

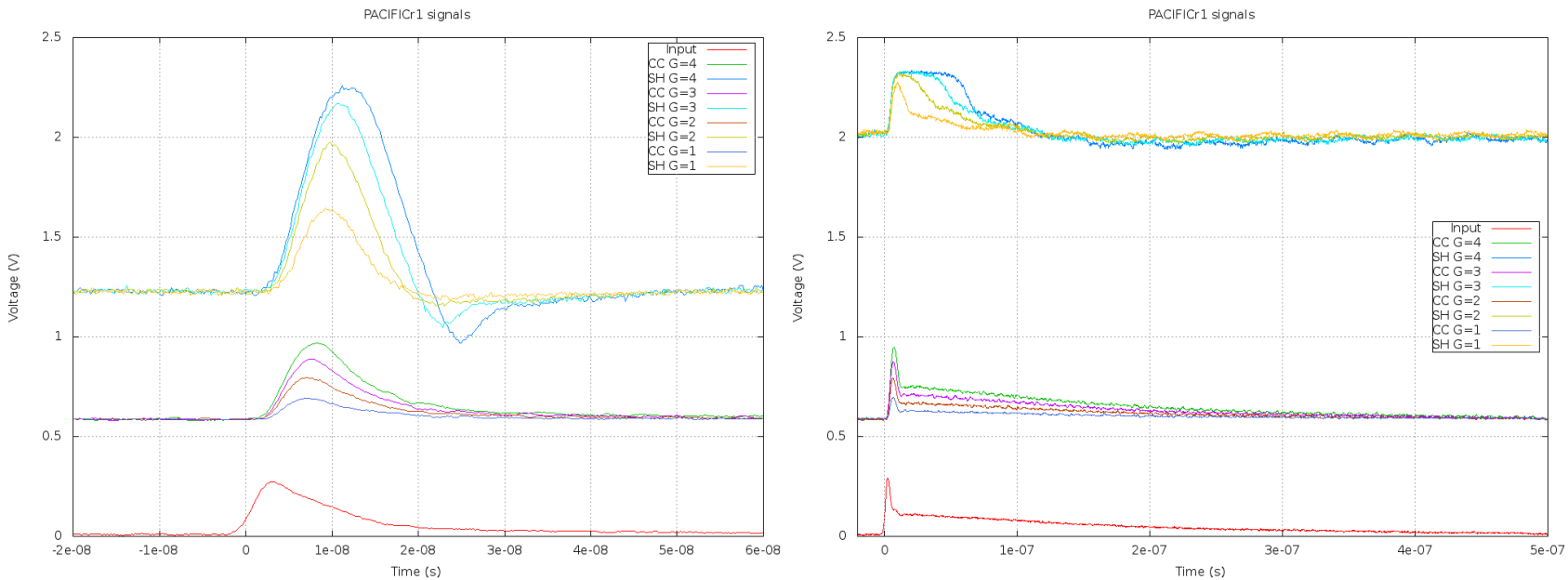

Figure : 4 gain of the current conveyor with two tests signals. Bottom: signal, middle: Current Conveyor, top: Shaper

2^{nd} PACIFIC prototype

PACIFIC 2:

- 8 analog channel from PACIFIC 1
- + Bandgap, DACs, Feedback loop
- + 3 thresholds digitization
- + 160MHz/320MHz serialization