UT Working group response to Report of LHCb UT Conceptual Design Review

14th November, 2013 at Syracuse, USA.

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Review panel:

Federico Alessio (CERN), Tony Affolder (Liverpool), David Lynn (Brookhaven), Mitch Newcomer (Univ. Penn), Ken Wyllie (CERN).

The reviewers thank the UT group for the clear presentations and the constructive discussion during the review meeting.

1. General Comments on Electronics

The proposed UT FE architecture is compatible with the global upgrade architecture. Solutions were presented covering almost all the aspects of the upgrade. The proposed implementations all seem feasible but many parts of the design are still very preliminary. For the missing items (for example, the Data Concentrator), the UT group must specify the functionality as soon as possible to allow the design to start.

No potential "show-stoppers" were observed, but there are some items whose development and verification is critical for the schedule (see below).

The system performance should be simulated together with the TELL40 code and the TFC commands. The throughput of the complete system requires more detailed analysis, in particular if the Data Concentrator is included.

Response:

The integration of the UT data readout with the global upgrade architecture is a challenging task because the granularity of the detector requires the GBTx to be split into several sub-frames associated to different ASICs. A system optimization is under way. We are focusing on the mode without data aggregation in the data concentrator board because of the risk of including many FPGAs performing complex functions in a region with limited accessibility and relatively high radiation levels for commercial electronics.

System integration aspects always impact on the performance of the front-end circuit. Given that the SALT is currently under design and hence still open for optimisation, system issues should be investigated immediately with existing prototypes and fed-back into the SALT design.

The radiation levels expected in the hottest parts of the detector appear to be well known. However, the levels in the area of the 'balcony electronics' are very roughly estimated. These levels are critical for the choice and evaluation of components on the balcony boards. The UT group should contact Matthias Karacson (Gloria Corti) to request simulation data specific to the location of the UT electronics.

We have now a detailed simulation of the radiation level surrounding the detector area. The only regions "safe" for commercial radiation tolerant electronics are the sides of the detector away from the y=0 axis.

No documentation was prepared in advance for the review. This will be essential for the design of the new components and the overall system so should be started immediately. This is particularly relevant for the design of SALT. In general, it is recommended to provide a full list of requirements for the system and the chip. This can then be used as a checklist to evaluate the completeness of the designs, allows easy communication between designers and can help in making certain design choices.

The requirements have been documented in several talks and are being collected in a single document. Some of the parameters needed to evolve with the system design. For example, power consumption optimization may be achieved by relaxing some of the requirements on the DSP complexity.

The UT group is asked to converge on the final quantities of common components (GBTX, VTTx/VTRx, GBT-SCA, DC-DC convertor, ST linear regulator) by the end of this year. Production of many of these is planned to start in 2014.

This task is difficult because of the evolving data flow architecture design. However with the baseline model presently considered, the numbers are:

component	# required
GBTx	1480
VTTx/VTRx	680/160
GBT-SCA	230
ST linear regulator	2900

Many details of the system have to be decided soon and this requires precise input from the different aspects (ASIC, hybrid, cable, balcony). Working meetings must be started dedicated to these issues, where the system details can be worked through. The panel recommends these meetings occur on a regular basis.

The meetings are indeed ongoing as often as required to solve specific problems. The system optimization is the key R&D item and thus requires time to be implemented properly.

2. SALT chip

The design of the SALT chip is progressing well but to a very tight schedule. However, it is clear that it is based on an evolving specification. The original specifications, which concentrated on the analog requirements, covered a wide range of detector capacitances for all the SALT applications at that time. These should re-written to concentrate solely on the UT.

We have restated the specifications specialized on the UT. In particular, measurements on prototype detectors have lead us to imply that Cd<15 pF is a safe assumption.

For scheduling reasons, an attempt must be made to have a complete working chip from the first submission. All effort must be made to make this succeed. Intermediate submissions with fewer channels/functionality should be minimised.

The digital functionality has not yet been specified. This is critical for the design, and should be documented immediately. This needs urgent action on the precise definition of the data-processing algorithms and their porting to RTL.

It is clear that the blocks designed and tested so far have met or exceeded their design goals. However it would be useful to re-examine the specifications and optimize the design for the refined understanding of the detector system. In particular the designers should be given a reasonable upper limit for the detector and stray capacitance of the sensor and interconnects.
Given comments during the meeting a safe number would be 20pF instead of the 35pF currently specified.

Measurements on prototype detectors demonstrate that Cd<15 pF is a safe assumption.

It is understood by the reviewers that any change in functionality can have significant schedule implications and so design changes should be motivated by a demonstrated improvement in the physics potential of the UT.

1. The Sensor Capacitance needs to be specified accurately to allow ASIC designers to accurately optimize power consumption.

2. The current 50keV dynamic range of the front end will need to be checked and specified. It may be useful to have more than one range for different parts of the detector. These could be bond-wire selected or programmable after power-up.
   The dynamic range requirement has been changed to 30Ke, better suited to the thickness of the UT detectors. We chose not to implement programmable gain to avoid introducing another level of complexity in the design.
3. The return to baseline of the shaped signal seems quite important and could be aided by a shaping function with an uncompensated zero that causes a slight overshoot. The price of an effective increase in threshold for 10-20ns may be worth considering as it is likely to reduce the data following a pulse of interest. Can this be of benefit to the power consumption?

At the moment this option is not pursued in view of the successful implementation of the return to the baseline specifications with the analog processor implemented in the first prototype.

4. The decision on the bond-pad and channel pitch must be made soon.
   The channel pitch has been fixed to be 73 μm.

5. Spillover has been minimized in the analog domain by complex shaping. Is spillover correction after digitization still considered?
   Yes, in the TELL40 processor
6. There was some discussion on the response of the SALT to large charges. This should be modelled and simulated with the analog front-end circuit. How often is this expected to happen? If the shaper output takes time to return to zero in such cases, will this be translated into hits (and hence data bandwidth) for a number of clock cycles? Will this use up significant bandwidth? Digital spillover correction would be useful in these cases.
   The digital spillover correction should be able to correct for this.
7. Does the 6 bit ADC data create undue overhead?
   a) In power consumption? 1.8mW/channel (Analog preamp and shaping) per channel is approximately 2-3 times larger than necessary for a binary system. Some of this power may come from the large capacitance requirement and fast return-to-zero.
      An analog front end electronics implies a higher power consumption than a binary one. However, the ADC has very low power (~0.35 mW/channel), taking into account the single-to-differential converter stage, the overall additional power consumption is ~0.7 mW/channel.
   b) In data flow? What percent of data flow off chip is 6 bit ADC data? Would it be possible to add a binary data mode to the SALT chip where each transferred address would indicate a strip signal above a defined threshold? A sparsified readout might specify a leading address and the number of channels above threshold so that several contiguous strips could be identified as one address plus a few bits
      This is an illustration of the bandwidth partition in the UT readout:

	DataRate (Gbps)	Percentage (%)
Header for non beam-beam crossing	438	20.4
Header for beam-beam event with no hit	729	34.0
Header for event with hit	409	19.1
Hits only (7-bit Channel ID, 5-bit ADC)	568	26.5
Total	2144	100

Most of the bandwidth is not occupied by the ADC information, which is a valuable monitoring tool. Concerning the clustering of the ADC information, studies have shown that we can save a few % of bandwidth on hits, but header requires more bits to specify length, with 0 net gain.

8. This continuous ADC sampling approach could be beneficial in reducing data from spurious noise by requiring more than one sample over threshold or even some primitive multi-sample integral value before sending digitized data off chip. Is there any provision for post fabrication tuning of the zero suppression algorithm?
   No, except from tuneable thresholds

9. The ADC uses dynamic logic. Dynamic logic is widely accepted to be more susceptible to SEUs than static logic. Will this be investigated? Is an alternative to dynamic logic possible?
   A test is planned for early June to assess the overall radiation resistance and the vulnerability to SEU of the current ADC prototype. This test will be repeated with the implementation with the TSMC technology.

10. The contents of the data packet corresponding to the 'Synch' command should be decided.

    It has been accomplished. Documentation is under way

11. Is a 'hard-reset' pulse for SALT required? If so, where will this be generated?

From the ASIC point of view it is not important to have hard reset. Power-On-Reset and Hard Reset pad with pull-up will be implemented. The pad may be not connected, however it may be very useful to have this connection.To avoid long cables, in case we decide to have Hard Reset, it may be generated locally by GBT-SCA chip

12. For the SLVS driver, the drive current should be configurable. This has proven to be crucial in other applications. The range of adjustment should allow the current to be set to at least twice the standard SLVS value of 2mA. Resistor selection or the use of an on-board 6-8 bit DAC should be used to set the SLVS current.

This is considered in the design, we will add DAC in SALT

13. The signal shape can be much improved by using pre/de-emphasis in the SLVS driver. The need for this should be evaluated by testing the existing drivers with prototype cables.
    Prototype cables are going to be available in mid-may. These tests will be performed then.

14. For the SLVS receiver, what is the 3 sigma input offset uncertainty? This can be found by monte-carlo simulation but requires proper setup of the transistor and resistor properties in the schematic.

15. It should be possible to transmit only one "clock" to the SALT chip, at 40 MHz. An on-board low power PLL can be used to generate the required digitizing and data clocks. A programmable delay block should be used to align the outgoing data with the GBTX eLink receivers. OK

16. The TFC interface to SALT should be defined. This will require a rationalization of which bits are absolutely required. Some savings are possible, and it is possible that the complete command can be handled by a 320 Mbit/s link (8-bits per 40 MHz cycle). With the worst-case cable delay as presented, time adjustment of this frame should be implemented in the SALT to correct for these delays and guarantee that the command bits are properly allocated to the 40 MHz cycle. This can be a configurable synchronous delay based on the 320 MHz clock.

Done, this will be documented in the SALT specifications

17. The SALT group should re-use and borrow existing blocks as much as possible. Blocks such as a voltage regulator and PLL have already been identified. Another example is an I2C interface, with triplicated logic, which is available from CERN. Other blocks, such as DACs, can probably also be found.

This advice is good and will be pursued, the SALT designers are currently planning to adopt an existing design for the linear regulator, memory block may be necessary for data buffering. In addition e-ports are CERN IP.

A good estimate of the digital power consumption of the SALT must be made as soon as possible.
This is really important and has not yet been achieved but it is a top priority of the UT electronics group.

18. What calibration will be required for the SALT? What will be required in-situ during detector operation and how often will calibration be required?

    Pedestal/noise calibration will be performed more frequently (frequency to be determined with experience with the prototypes), gain calibration can be done only during technical stop.

19. The SALT must have the ability to individually delay each of the TFC bits in units of 25ns. This is foreseen to allow full flexibility in time-alignment. A range of 16 clock cycles is the minimum requirement as defined in the global specifications.

A FIFO of depth 16 will be added at TFC commands input, so each commands may be delayed up to 16 clock cycles individually

20. An up-to-date estimate of how much data is needed for configuration should be provided for reference for the ECS group. This should be used together with the ECS protocol, including the GBT-SCA, to calculate the time required to configure the SALT and for calibration.

    Done, it will be described in a separate document.

21. At the time when the first full SALT chip is available, a fully functional test and readout system must be available. This implies a system capable of handling the full bandwidth. This is not trivial and requires significant preparation time. This will have to include full ECS/TFC functionality.

    This is well under way, the critical path item for our project is to have a 128 channel SALT chip.

22. There is no error detection/correction on the eLink outputs of SALT. Is there any risk of errors? What steps are being taken to mitigate errors? Will the downstream system be robust to data errors? This should be tested, and recovery mechanisms implemented if necessary.

    Agreed, this is ongoing work, error detection on the header is included.

23. The design of SALT, hybrid and the mechanics/cooling should now progress together hand-in-hand with good communication between designers. In particular, the pad layout of SALT should be carefully optimised at an early stage by the chip and hybrid designers.

    Agreed, this is ongoing work

24. In general, the design techniques to ensure radiation tolerance should be immediately implemented. A complete programme of tests to ascertain the radiation hardness of the existing SALT blocks must be established, and planned. This requires a number of actions, including designing hardware and booking radiation facilities, so has to start immediately.

    Agreed, this is ongoing work

3. Hybrid, Data Transmission & Balcony Electronics

1. A hi-tech hybrid technology was presented. The reviewers understand this is motivated by the large number of signal tracks required. This proposal should be better understood, including issues like delivery time. It should be investigated if a more standard flex technology can be used after the number of signals is optimised (see below).

   Now we are focusing on a more standard technology.

2. The hybrid design is novel (flex hanging outside of sensor). Relative realistic prototypes are needed to understand hybrid assembly and hybrid mounting to cores.
   Ongoing R&D, the flex circuits and the sensors are supported by a thin carbon fiber structure in an option being pursued.
3. QA of hybrids with sensors needs to be understood and planned, especially if thermal cycling/shock testing is needed.
   In progress, a separate document will describe this.
4. The targeted glue thickness (50 um) on between hybrid and stave will require precision surfaces on hybrid and core with tapes. Tests are needed soon to see what is practical and thermal simulations and material calculations are needed to determine the effects of thicker layers.

5. A stiffener for the hybrid is missing. The hybrid-sensor assembly (i.e. module) should be tested before being mounted onto the stave.

6. A full electrical schematic for the stave should urgently be made as a baseline design. This would likely require a working meeting of those working on ASICs, hybrids, balcony electronics, and slow controls. This would facilitate a common understanding among those involved and should lead to a common optimization of the design. Issues of bandwidth and trace count as well as voltage drops are all interrelated. One goal of such a design would be to limit the numbers of traces in the bus such that a standard kapton circuit technology could be used.
   In progress
7. A first routing of hybrids and cables must be made urgently in both standard and Hi-tech technologies prior to place and route of the SALT. Details of this routing should be used for the optimal positioning of bond pads on the SALT.

8. The UT group should carefully study and document the clock distribution on the hybrids. The use of multiple clocks (40 MHz, 320 MHz) should be rationalized and carefully studied at the interfaces where data changes clock domain. Techniques to minimize the number of traces should be used, such as an embedded PLL within the SALT.
   In progress
9. A number of hybrid designs are proposed, each with a different number of SALTs (4, 8, 16). The UT group should examine the possibility to keep the maximum hybrid chip count at 8. A solution for this by using glass/aluminium pitch-adapters was proposed by one of the reviewers and should be investigated. This reduces the number of different components required for prototyping, production and testing. This may also allow a better matching of the chip aspect ratio with the hybrid dimensions.
   Now we have only 8 & 4 SALT hybrid design
10. It was stated that SALT chips in low occupancy regions of the detector will use fewer eLinks than the hotter chips. Unused eLinks would be disabled. This has clear advantages for saving power, but it may be prudent to physically connect all eLinks of all SALT chips to the hybrid and cabling, even if they are not all enabled. This would introduce redundancy and allow some extra margin if detector occupancies (and hence bandwidth) are higher than predicted. It should be investigated if this is feasible in terms of track routing.

11. The plan for developing a custom cable plant is in a very early stage and, given the schedule that calls for production to begin in 2015, technologies with reasonably short lead times should be exploited if possible. Particular attention needs to be paid to the lines that will carry data at 320Mbps. To avoid the need for iteration on complex terminations and the possible interplay with the drivers and receivers it would be optimal to have the line resistance not much higher than 10% of the

termination resistance along with attention on the driving and receiving end to keep the stray capacitance low.

In progress

12. The proposal to use a test board with configuration and flexibility to understand clock and data transmission between the hybrid and balcony electronics seems very important both for testing cables and hardware. Prototypes of SALT blocks use the proposed SLVS drivers, and it should be understood if these can be used for data transmission tests.

    This is a possibility and we are planning tests in the summer

13. While parallel powering seems like a good idea for the geometry of the UT, care needs to be taken with the LV power cabling. In the extreme case shown of driving 16 SALT chips over the longest length power cable, the current requirement of more than 10 Amps would dissipate 100 Watts of power if the resistance of the power and return lines totalled just 1 ohm. If the cable resistance can be limited to 1/4 ohm and the load limited to 8 chips, the power loss would be closer to 6 watts which seems much more manageable. It would be useful to place a limit on the cable power dissipation based on the safe 10 year operating conditions.

14. Delivery of power to the hybrids should be checked with the ASIC technology specifications. The acceptable power drop needs to be checked against maximum allowable voltages at ASIC. Is it possible to have transients on power up/down which can put dangerous voltages on the ASIC? What is the maximum allowable voltage with different regulator choices? How will the power be separated?

15. A complete grounding and shielding scheme needs to be developed and a group should be given responsibility to ensure that each element of the system observes these rules. Since the system is complex, simple tests can be implemented to validate that all pieces in the system conform to the basic connectivity requirements. The existing plan for LHCb should be consulted (http://lhcb-elec.web.cern.ch/lhcb-elec/html/grounding.htm).

16. To the maximum extent possible, supplies should be floating and no current should flow between the Balcony electronics and the UT front end. HV returns should be filtered in a similar way to the incoming HV to avoid external noise entering there. The low side power potential (loosely gnd) of the Balcony electronics should be at the same potential as the UT detector reference voltage. This common potential between the two parts of the readout should be established and maintained by a network of conductors that do not return or equalize DC supply current between the front end and balcony electronics. These may serve the purpose of shields on cables between the two.

    These considerations are included in the design of the HV/LV distribution

17. The use of commercial-off-the-shelf components in the Balcony modules should be assessed together with the expected radiation levels in the upgrade environment. Will radiation tests be required? These can take a long time and should be planned immediately.

    The philosophy that we adopt is to use commercial devices only where the radiation is expected to be <100KRad during the nominal data taking time.

18. The proposed data concentrator functionality on the balcony electronics is a new concept and is motivated by data decoding issues in the TELL40 (see below). This concept should be developed further with some urgency, as it can have a big impact on the SALT requirements. The functionality can maybe be implemented in an FPGA. This should be carefully studied based on better estimates of the radiation levels in this area.

The current default is to do the data concentration in the TELL40, this alternative is studied to investigate the cost/performance ratio in the two solutions.

19. If an FPGA is used for the data concentrator, how will it be programmed?
    JTAG
20. The requirements for bulk power supplies should be determined. The general LHCb philosophy is to re-use the existing power supplies. This will introduce boundary conditions on the design of the upgrade power distribution and the parameters must be carefully examined. The availability and quantity of the power supplies must be checked.
    Done
21. Will the power parameters change through the lifetime of the detector? For example, will adjustments for radiation effects change the power consumption? This should be estimated and included in the calculation of the limits of the power system.
    The innermost sensors will have higher leakage current, this is taken into account in the power supply segmentation.

4. TFC, ECS and TELL40 processing

1. The data format from SALT has been optimised to minimise the number of links. This has an impact on the number of links that can be accommodated by a TELL40 FPGA, especially for the low-occupancy regions where many independent SALT chips will be aggregated onto a single GBTX link. The decoding of these independent data streams buried within GBTX frames will require significant FPGA resources, and hence an increase in the number of TELL40 units and the subsequent cost. This is a problem already identified by the TELL40 group and communicated to the UT community. The Data-Concentrator has been proposed to solve this problem by accepting data from low-occupancy SALTs and building larger event packets before transmission to the GBTX links. This has clear advantages but introduces cost and complexity to the balcony electronics. It is not obvious that this will be more cost-efficient than buying more TELL40s. The UT must look at these two scenarios and understand which is optimal.
   We consider the TELL40 processing option baseline, but we are investigating the alternative option

2. The mechanism in the TELL40 to add the extra bits to the BXID should be studied and documented.

3. The TFC commands should be discussed with the TFC group and a decision made on which bits are necessary. The use of the BX-veto should be clarified in terms of the SALT functionality.

4. The implementation of a TFC fan-out is not obvious. This should be investigated.

5. The current scenario assumes one 'TFC-command-bus' connects to four SALT chips in a multi-drop SLVS scheme. This should be investigated.

6. The ECS distribution has been optimised for compactness and a minimum number of links. It should be clarified that this does not introduce long configuration times for the complete system, for example in the use of the I2c busses from the GBT-SCA.

7. The DCS should be designed to run independently from the TFC system.

8. Monitoring and safety systems should be studied and designed into the system. The parameters to be monitored should be decided soon so that they are included in the system design.

Points 2-8 have been studied and will be documented separately.

5. Manpower, Budget and Scheduling

We have a detailed WBS for the UT project, that is currently being scrutinized by the LHCb management and has been endorsed by the UT PIs.

The plans for ASIC submissions (and production) and sensor development seem plausible if no major changes are envisioned but when combined with the very early stage of the hybrid and cable development the schedule seems very tight. New technologies should be avoided unless they can be done in parallel with already proven techniques.

Given the tight schedule of the project, a strong active management structure is needed to coordinate activities and enable decisions. A full-time coordinator for each of the different aspects (eg mechanics, sensors, electronics) is strongly recommended. A clear line of responsibilities and milestones need to be better defined.

Since the schedule is heavily reliant on the SALT availability, all effort should be made to arrive at a working chip as soon as possible. This means not only in the design work, but also specifications and testing preparation. Prototypes have already been delivered to one institute outside Krakow. Can other institutes also make use of prototypes? (for example, for data transmission tests discussed above).

It was mentioned that the first request for funding of the SALT ASIC was turned down. What kind of contingency planning is in place for funding this chip development?

The test procedures to verify the SALT functionality should be clarified (eg laboratory tests, irradiations) and planned well in advance. This includes the design of electronics required specifically for testing, which will probably have to be replicated in a number of institutes. Manpower for the testing should be identified soon.

The design of items in a coherent manner to allow realistic systems tests as early as possible is extremely important with the limited contingency in the schedule. Tests should include as realistic conditions as possible (real cable lengths, balcony electronics, power supplies, etc) with three or more overlapping stave parts.

The engineering effort for all aspects of the project must be assessed more carefully and checked against the available manpower.

6. Mechanical Review Summary

The mechanical design of the Upgrade Tracker (UT) was presented in a series of talks focused on an overview, on stave design, on thermal stave simulation, and on integration issues. The main elements of the mechanical system are the stave, the frames, and the “box” enclosure. Only the stave was presented in any detail as the other elements have not yet reached the stage of a conceptual design.

Production is scheduled to begin in approximately two years from the date of this review. Successful completion of the mechanical portion of the UT will require active and aggressive management that focuses on quickly converging to a final stave design. Resources to initiate designs of the frame and box should be quickly identified. We note that at the moment manpower primarily consists of a single physicist at Syracuse and an engineer at INFN; these need to be supplemented with additional engineering and technical help as soon as is possible.

We below comment upon or make recommendations on major elements of the mechanics.

Stave design

The stave design follows developments from Atlas and in principle should work with a couple of caveats. The snake pipe design may have problems with extra pressure drops or internal pressure forcing the pipe to straighten. We recommend also modeling a straight pipe design similar to what was presented but with the carbon foam optimally placed for maximum cooling. Also, if the pipe and cooling with the snake pipe does work, it is worth considering a mirror image design in which the pipe enters from the other edge of the stave so that the pipe more closely approaches the beam pipe cutout region in the middle of the stave. The team should focus on quickly resolving the pipe design as this impacts the stave construction.

Consider whether the cutouts in the rohacell core are worth the effort in terms of radiation length savings. Also, one needs to consider that rohacell is hygroscopic and whether this will create problems in the different environments that the stave will inhabit from construction to installation.

Confirm the radiation hardness of rohacell to the expected upgrade fluencies.

Methods of measuring the change in shape of the stave when chilled needs development.

No mechanical simulations were presented. A vibrational frequency analysis is suggested and understood in terms of stave bending stiffness. The impact of the mounting method and its impact on the first vibrational mode should be simulated. If there are any data on the vibrational spectrum of the area in which LHCB sits these should be made available.

Bonding of pipes to carbon foam should be studied more. Might be able to improve uniformity and reliability.

Thermal simulations

The thermal simulations are nascent and will need to be refined. The environment inside the “box” needs specification so that convection and radiative power transfer can be included.

The radial dependence of detector current in the innermost sensor should be modeled.

The simulations should show the margin that the innermost sensors have from thermal runaway after full irradiation and after the correct radial dependence of detector current has been implemented.

An optimized modeling of a straight pipe design with the thermal foam optimally located is suggested.

Power generated in the bus cables should be included in the simulations as soon as a bus tape preliminary design in generated.

Assembly of modules and bus tape onto stave

Hierarchy of alignment and placement precisions needs to be made more explicit. It isn’t clear what precisions are needed for placement of modules to core and core to frames. This will impact the complexity of the assembly process and the assembly methods that are chosen.

Sensor survey precision needs specification and a method of surveying needs development. The stave is a long object that does not fit onto typical optical metrology machines.

Mounting of the modules will likely be problematic and will likely be the critical step in the assembly. Atlas experience with 10 cm x 10 cm sensors shows significant bowing, both concave and convex. Additionally, the stave surface due to the bus cables may not be flat. Development of a module mounting scheme and practical testing should take place earlier rather than later and should be concurrent to the stave design/construction project.

The gluing of long kapton bus tapes onto the stave surface may have difficulties with regards to alignment and bubbling. Development of this method should similarly be begun sooner rather than later.

Schedule and resources

Timelines and scheduling for stave, box, and frame R&D were not presented. A fully resourced schedule with milestones is urgently needed.

QA

A fairy comprehensive and standard list of QA procedures was presented and seemed reasonable. Details of the QA procedures will emerge as the designs mature.

Other

The mechanics for the frame insertion and removal was not presented. Can the existing mechanism be re-used or is this another development project?

The U-V tilt and its impact on the global frame needs to be worked out more.

Shipping and handling of hybrids and staves needs to be developed more; can cause bigger issues.

7. Response to Mechanical Review Charge

Responses to the specific questions posed in the charge to the committee are below (*in italics*).

The reviewers should assess the following aspects of the proposed system:

- Are the specifications clearly stated? *Soft (i.e. not quantitative) specifications for the stave were presented. More quantitative specifications should be developed, e.g. bending stiffness. No specifications on the frame (e.g. weight, stiffness) or the box (e.g. thermal isolation) were presented and need to be developed.*

- Is the detector concept likely to meet the specifications? *We see no fundamental problems with the overall design.*

- Are the assembly and integration procedure clearly outlined? *Some conceptual assembly of the hybrid and module to the stave was presented. There were clearly problems with the lack of a stiffner for handling the module and mounting it onto a stave. The assembly and integration onto the stave needs further development, and assembly of staves onto frames needs to begin development.*

- Are sufficient tests being planned to ensure that the components can handle the radiation levels? *Max radiation levels were specified in several talks as ~20-30 MRad and several 1 x 10^{14} n_{eq}/cm^2 (although one talk specified as high as 100 MRad). There was no mention of radiation testing of mechanical components. However, most of the components of the stave should be sufficiently radiation hard if epoxies that have been qualified by Atlas or others are used. One possible exception is the rohacell whose radiation hardness as such levels is unknown to this committee. Demonstrating Rohacell's radiation hardness, in this has not yet been done, should be a priority.*

- Comment on manpower/schedule? *Manpower at present is minimal and should be supplemented. A schedule for the mechanical program leading up to production in 2016 was not presented.*

- Is documentation being prepared sufficiently comprehensive? *This question is unclear. Presumably the question refers to documentation for the TDR. There was no talk describing the documentations being prepared. A reference mechanical document was supplied to the reviewers prior to the review. This document is very preliminary and will need to be more detailed and comprehensive for the TDR.*

The following items of the proposed architecture should be checked:

- Stave design *Addressed in Section 6*
- Mechanical/thermal simulation studies *Addressed in Section 6*
- Integration/test planning *Addressed in Section 6*
- Planning for the critical steps in the assembly procedure *Addressed in Section 6*
- System robustness (eg radiation, detector data, synchronisation....) *This is really not a mechanics question*
- System tests/qualification requirements and tests objectives *Addressed in Section 6*

8. Sensors

Three variations of sensors were presented with effective readout strip pitches of 48 μm, 95 μm, and 190 μm pitch fabricated with n-in-p, n-in-p, and p-in-n technology, respectively. More details of the geometry were not presented as the designs are preliminary. Prototyping will use Atlas07 n-in-p detectors and micron n-in-p as well as p-in-n prototypes.

There is no fundamental difficulty in obtaining radiation hard sensors for the UT project. Radiation studies of n-in-p and p-in-n sensors have been done and the radiation damage effects are well documented. The sensor team must now only choose it technologies, vendor(s), and geometries. We recommend keeping the designs as simple (and standard) as possible.

1. For the innermost detector, we would recommend that the team look into whether overall system simplification is achieved if one uses a half length (5 cm) detector with 95 μm pitch. This would enable a design that limits the maximum number of SALT chips per hybrid to 8. This has the benefit of easing the hybrid layout and the SALT form factor, and eases fan-in layouts.
2. We also suggest the team determine whether there is really any significant cost savings in using the p-in-n detectors, particularly as this will add effort to the

irradiation program and test cycles in the near term, and add complexity later in terms of slow controls, power supplies, and QA.

3. Evaluate that, given the limited time and resources of the sensor team, whether it is advisable to attempt interior fan-ins or just simply use exterior fan-ins with a minimizal radiation length penalty. Else the team needs to rapidly prototype interior fan-ins to determine if issue exists with charge loss/pickup and increased noise from increased capacitance.
4. It may be possible to design the system with just two types of sensors, the shortened inner sensor and a longer n-in-p outer sensor. The cost would be more sensors/stave however.
5. The team should measure load capacitance ASAP for technologies under consideration. ATLAS07 sensors had ~1 pF/cm (not 2 pF/cm quoted from HPK). This is important to enable power savings in the SALT front-end.