PCIe40 design

J.P. Cachemiche, P.Y. Duval, F. Hachon
M. Jevaud, R. Le Gac, F. Réthoré
Centre de Physique des Particules de Marseille

Outline

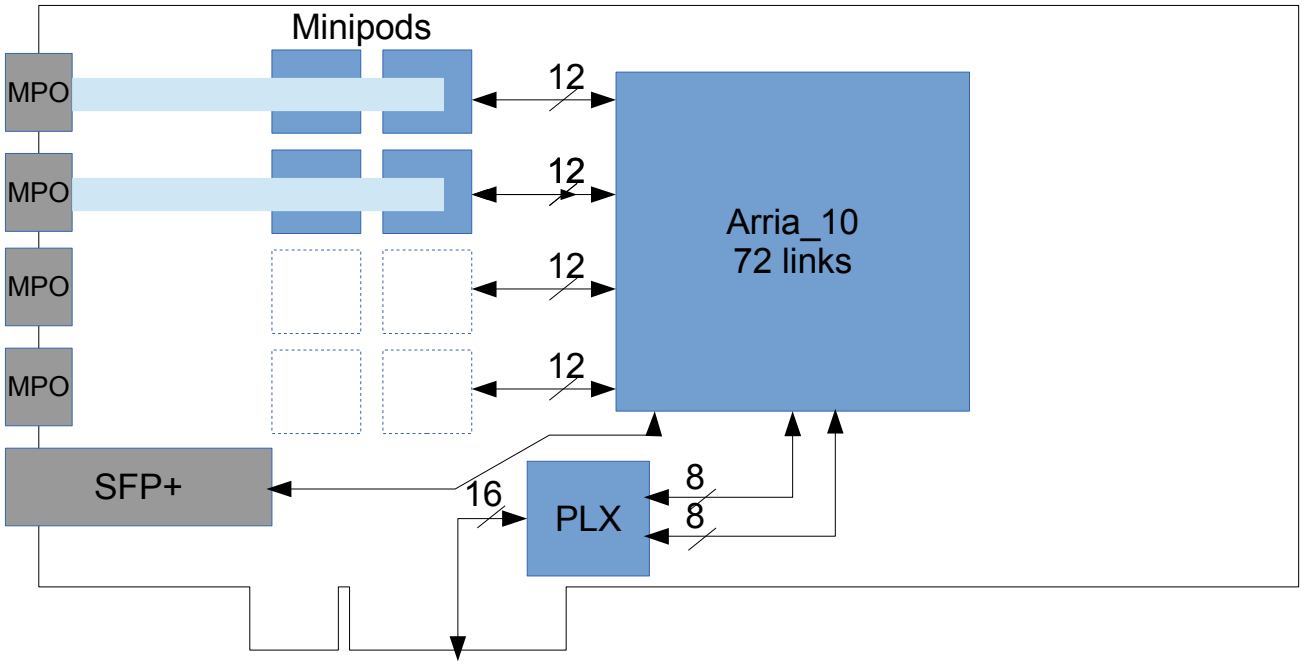
- Foreseen features
- Planned schedule
- Potential risks
- Technical approach

Foreseen features

Nominal configuration:

- *1 bidir link for TFC*
- *24 GBT inputs → limited by PCIe output bandwidth*
  - PCIe GEN3 x16 = 110 Gbits/s
  - 24 GBT wide bus = 107 Gbits/s

Up to 48 bidir links available on board for low luminosity sub detectors → decrease the costs



FPGA

FPGA 10AX115S4F45I3SGES from Altera

- Features

Resource		Product Line								
		GX 160	GX 220	GX 270	GX 320	GX 480	GX 570	GX 660	GX 900	GX 1150
Logic Elements (LE) (K)		160	220	270	320	480	570	660	900	1,150
ALM		61,510	83,730	101,620	118,730	181,790	217,080	250,540	339,620	427,200
Register		246,040	334,920	406,480	474,920	727,160	868,320	1,002,160	1,358,480	1,708,800
Memory (Kb)	M20K	8,800	11,760	15,000	17,820	28,760	36,000	42,660	48,460	54,260
	MLAB	1,050	1,833	2,451	2,864	4,404	5,096	5,788	9,386	12,984
Variable-precision DSP Block		156	191	830	985	1,368	1,523	1,678	1,518	1,518
18 x 19 Multiplier		312	382	1,660	1,970	2,736	3,046	3,356	3,036	3,036
PLL	Fractional Synthesis	6	6	8	8	12	16	16	32	32
	I/O	6	6	8	8	12	16	16	16	16

Product Line	KF40 (40 mm × 40 mm, 1517-pin FBGA)		NF40 (40 mm × 40 mm, 1517-pin FBGA)		RF40 (40 mm × 40 mm, 1517-pin FBGA)		NF45 (45 mm × 45 mm) 1932-pin FBGA)		SF45 (45 mm × 45 mm) 1932-pin FBGA)		UF45 (45 mm × 45 mm) 1932-pin FBGA)	
	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR	GPIO	XCVR
GX 900	—	—	600	48	342	66	768	48	624	72	480	96
GX 1150	—	—	600	48	342	66	768	48	624	72	480	96

Compared performance with Stratix V GX

Power consumption

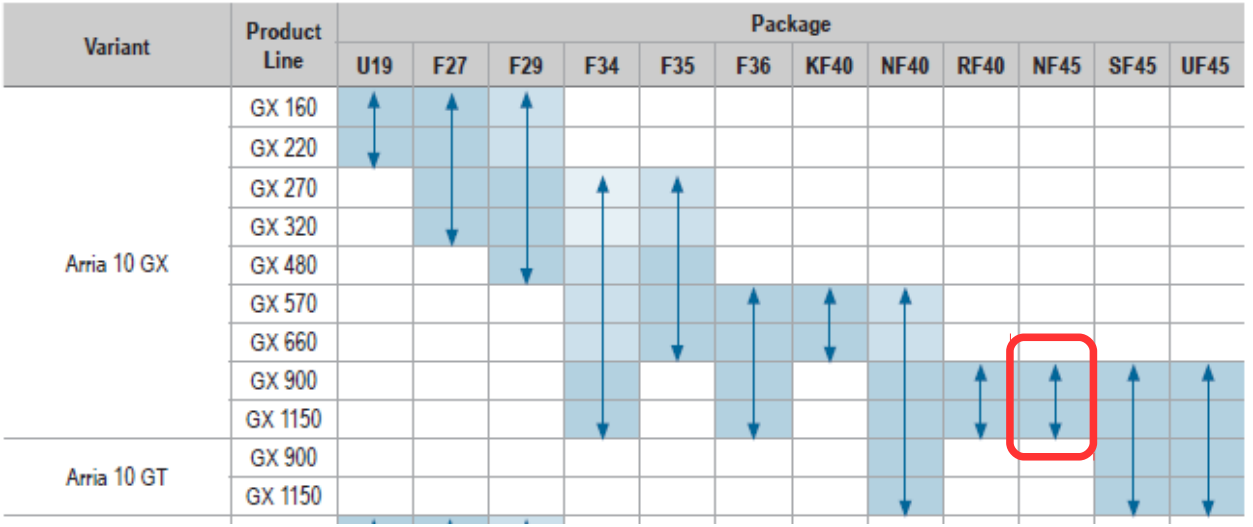
- ~30 % lower that Stratix V GX

Speed and density

	Stratix V A7	Arria 10 GX 115	Improvement
Density	622 kLE	1150 kLE	**1.8**
Multipliers	768	3036	**4.0**
Memory MLAB	-	13 Mbits	**1.3**
Memory M20K	50 Mbits	54 Mbits	
Core performance	500 MHz	500 MHz+	1.0
Transceiver data rate	12.5 Gbits/s	12.5 Gbits/s	1.0
Number of serial links	48	72	**1.5**
Memory interface	1866 Mbps	2666 Mbps	**1.4**
Cross migration	No	Yes: Stratix 10	

Vertical migration

Within Arria 10 family



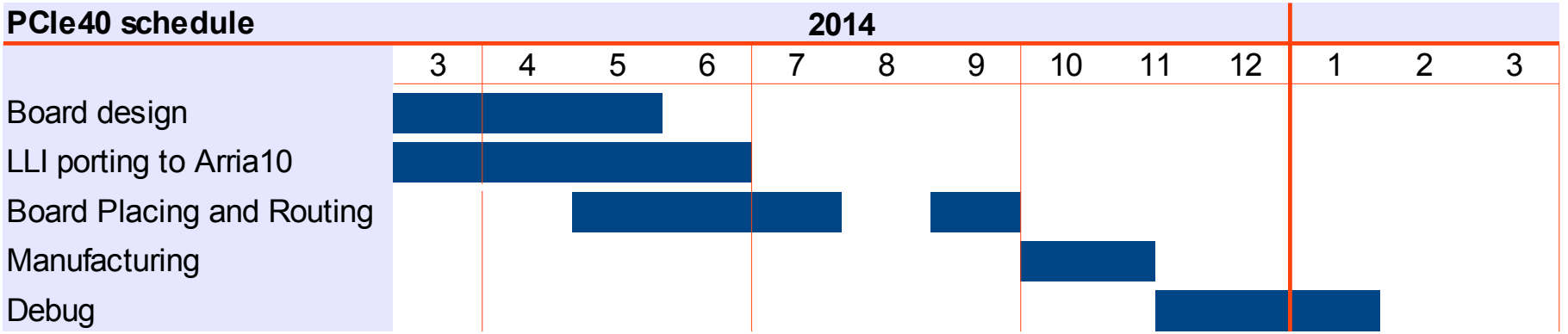
Variant	Product Line	Package											
		U19	F27	F29	F34	F35	F36	KF40	NF40	RF40	NF45	SF45	UF45
Arria 10 GX	GX 160												
	GX 220												
	GX 270												
	GX 320												
	GX 480												
	GX 570												
	GX 660												
	GX 900												
	GX 1150												
Arria 10 GT	GX 900												
	GX 1150												

With Stratix 10 family

- Assured with same density device

Schedule

(Ideal !)



Risks

Power supply dimensionning depends on :

- Firmware (occupancy, toggle rate, operating speed)
  - Not available now
- Available DC/DC
  - Possibly limited by layout
- Cooling capabilities
  - Not known
- Power estimator
  - Not yet available from Altera for Arria 10

Development tool

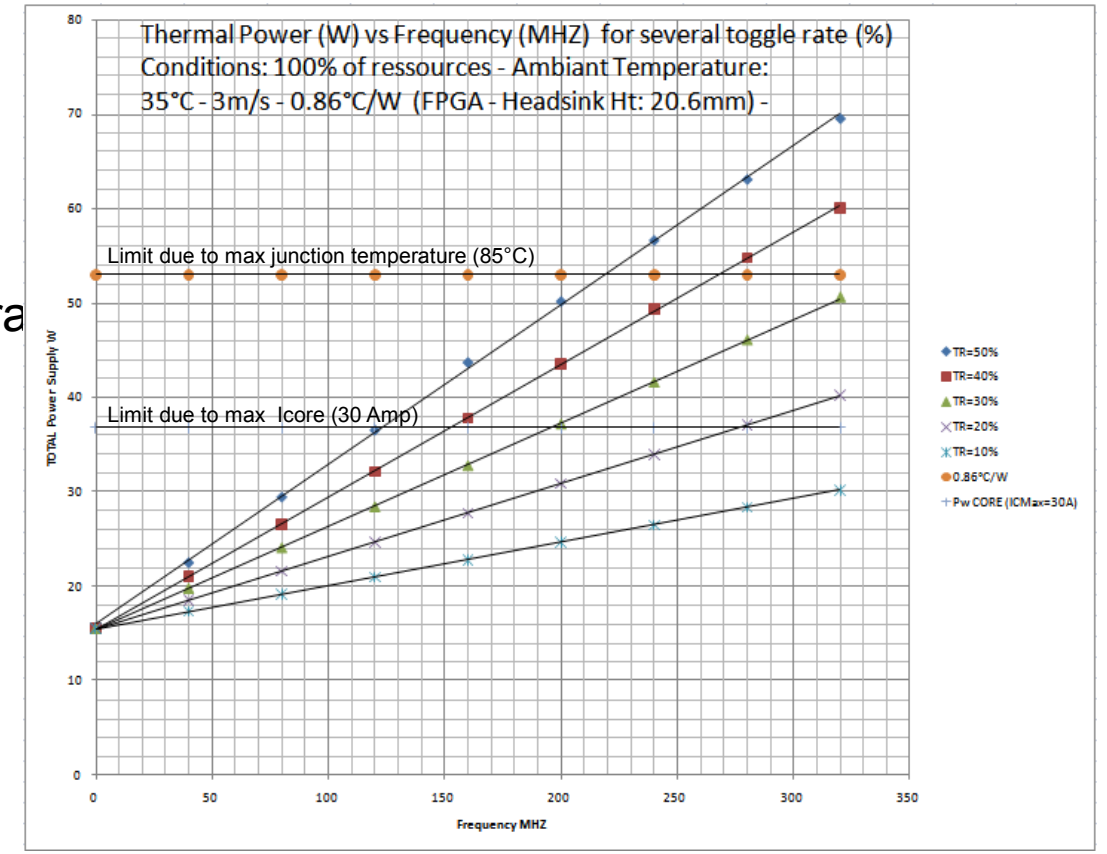
- Stability
- Portability of existing design

PCIe testing

- No physical loopback
- PC = black box

Power	Use
VCC	Core logic
VCCHIP	PCIe Hardware IPs
VCCHSSI	Physical Coding Sublayer
VCCR_GXB	GX receivers
VCCT_GXB	GX transmitters
VCCIO	I/Os
VCCPD	I/Os predrivers
VCCPGM	Configuration pins
VCC_AUX	Auxiliary supply for programmable power technology
VCCA_GXB	GX drivers and CDR
VCCA_FPLL	PLL analog power
VCCPT	Programmable power technology
VCCH_GXB	Block level TX buffers
VCCD_FPLL	PLL digital power
VCCBAT	battery backup

Up to 52 differentiated power sources on a Stratix V



Technical approach

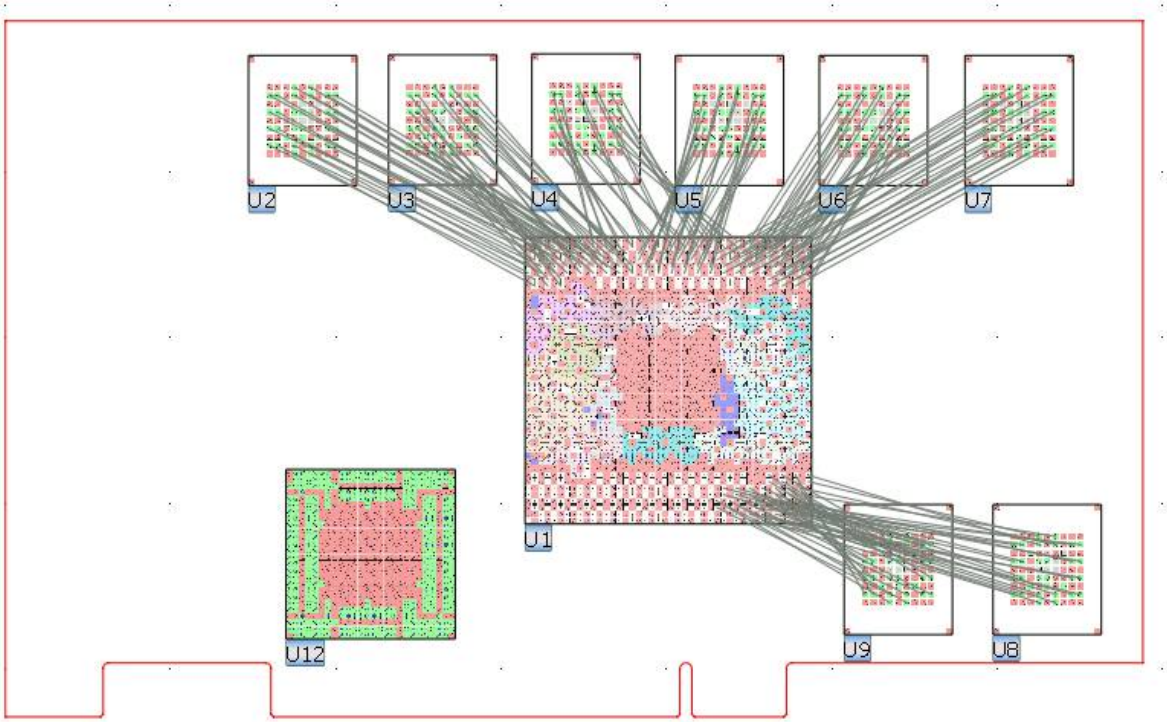
Minimum nominal design

- Limit as much as possible extra functions or new components that would complicate design, routing and debug
- Quickly specify maximum allowed form factor
  - Interaction with the choice of CPU blades

Experimented team at work

- 4 engineers at Marseille
- Can rely on many skills in the collaboration

Very good support from Altera



Standard height, half lenght implementation attempt

Conclusion

Tight schedule for getting an operating prototype by end of year

Staying on schedule requires as soon as possible:

- A realistic estimation of final firmware occupancy, speed and toogle rate
- Specification of environmental conditions (air flow, ambiant temperature)
- Specification of mechanical space available

Draft specification to be released in two weeks