GBTX: Tips for users

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Summary

- GBTX: a brief review
  - Mode/encoding
  - Clock domains
  - Configuration methods
  - Power-up sequence
  - Phase Adjustable Output Clocks
  - E-links
    - How to phase align the data of an e-link group
  - Power consumption example

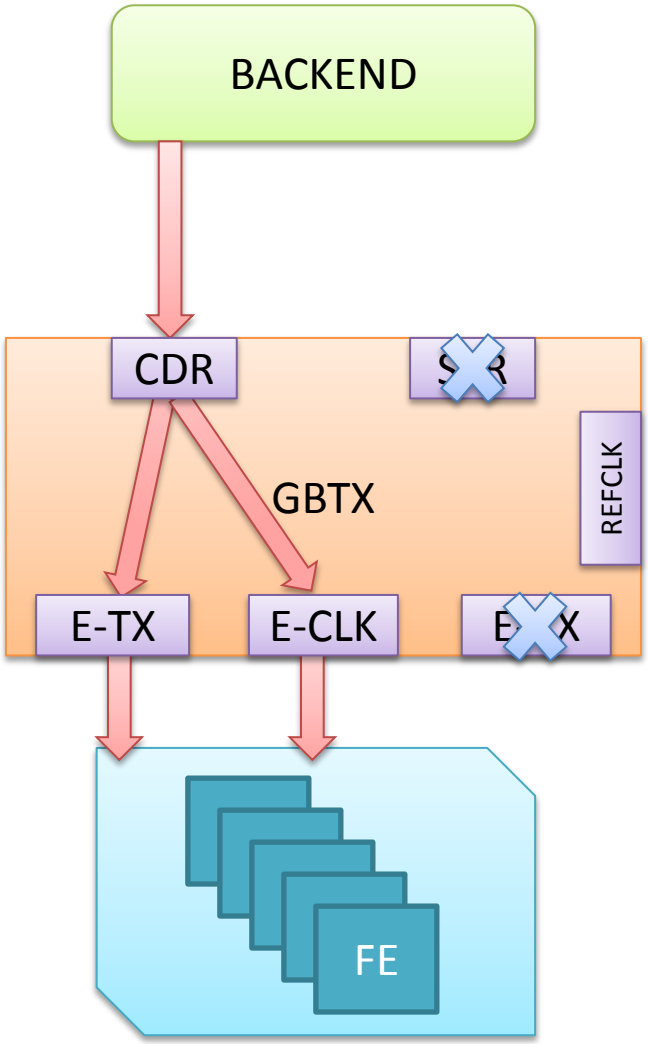
- A simple case-study:
  - GBTX transceiver (“master” GBTX) as clock source for multiple GBTXs transmitters

GBTX: a brief review

- Mode/encoding
  - GBT Frame encoding
    - Uplink and downlink
      - 80 data bits using 5 groups
      - 32 FEC bits
  - Widebus mode encoding
    - Uplink
      - 112 data bits using 7 groups
      - No FEC correction
    - Downlink uses GBT Frame encoding
  - 8B/10B encoding
    - Uplink
      - 88 data bits using 5 ½ groups
      - No FEC correction
    - Downlink uses GBT Frame encoding
  - Slow Control Information (IC and EC channels)
    - Only works in transceiver mode and with GBT Frame or Widebus mode
    - Both present in the uplink and downlink
      - 2 bits for the GBTX's Internal Control (IC) channel
      - 2 bits for EC (SCA link)

GBTX: a brief review

- Clock Domains
  - Receiver mode:
    - The CDR locks to the backend's clock
    - This clock is used for the e-links transmitter and e-links clock
    - The GBTX SERIALIZER can be turned off to save power



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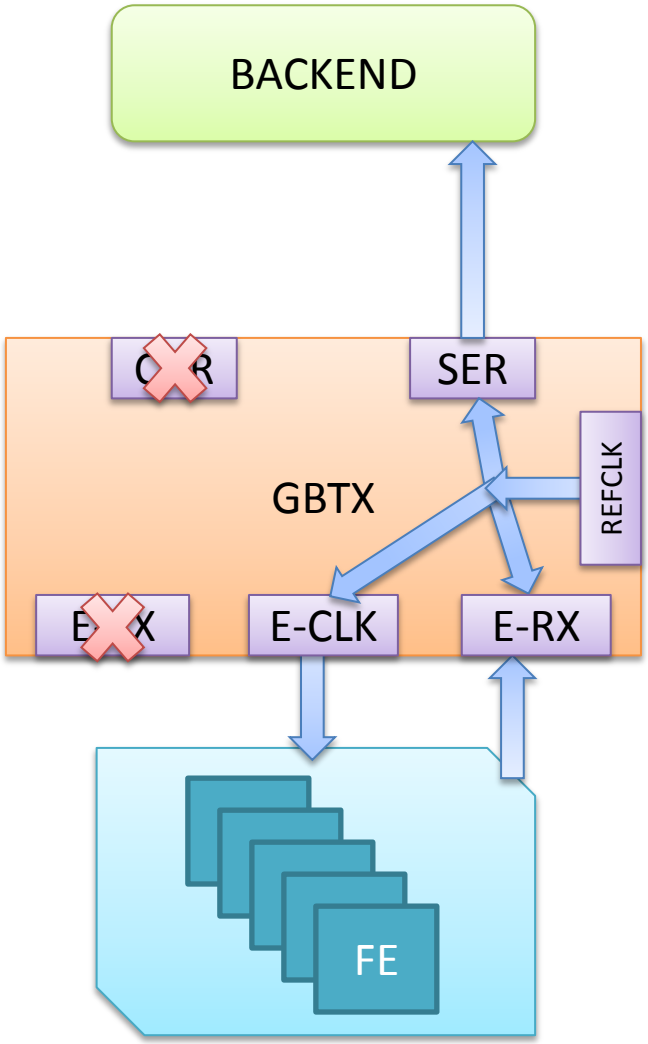
  - Transmitter mode:
    - The transmitter uses the REFCLK as a clock source; turning off the GBTX RECEIVER will save power
    - The EPORT-RX uses the SER clock



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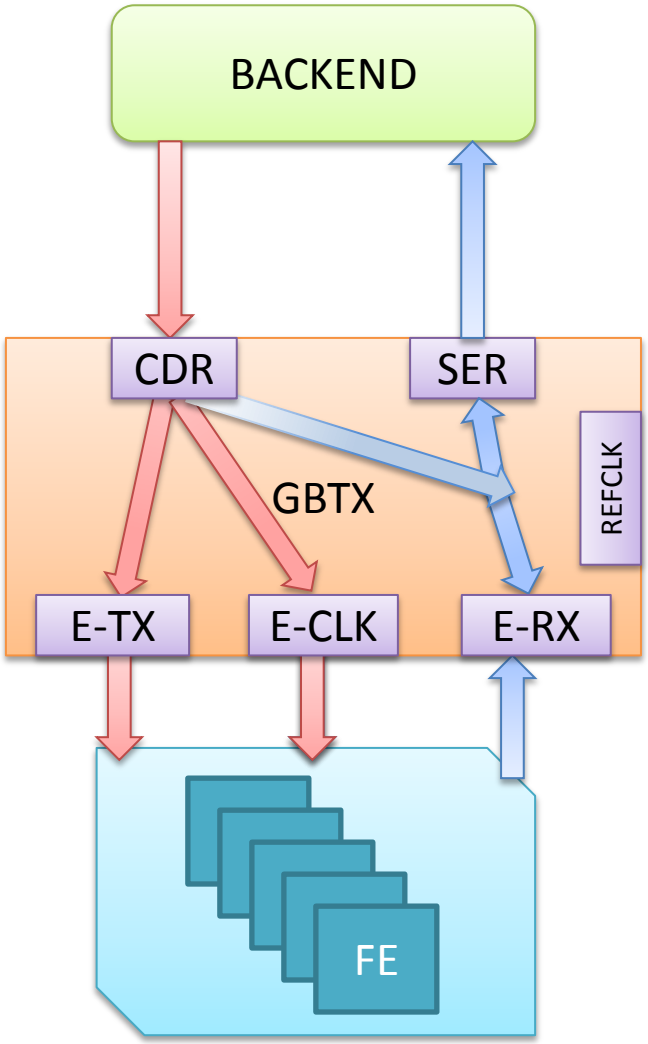
  - Transceiver mode
    - The CDR locks to the backend clock
    - The SER uses the CDR clock and should only present a phase shift
  - The GBTX mode is selected by input pins

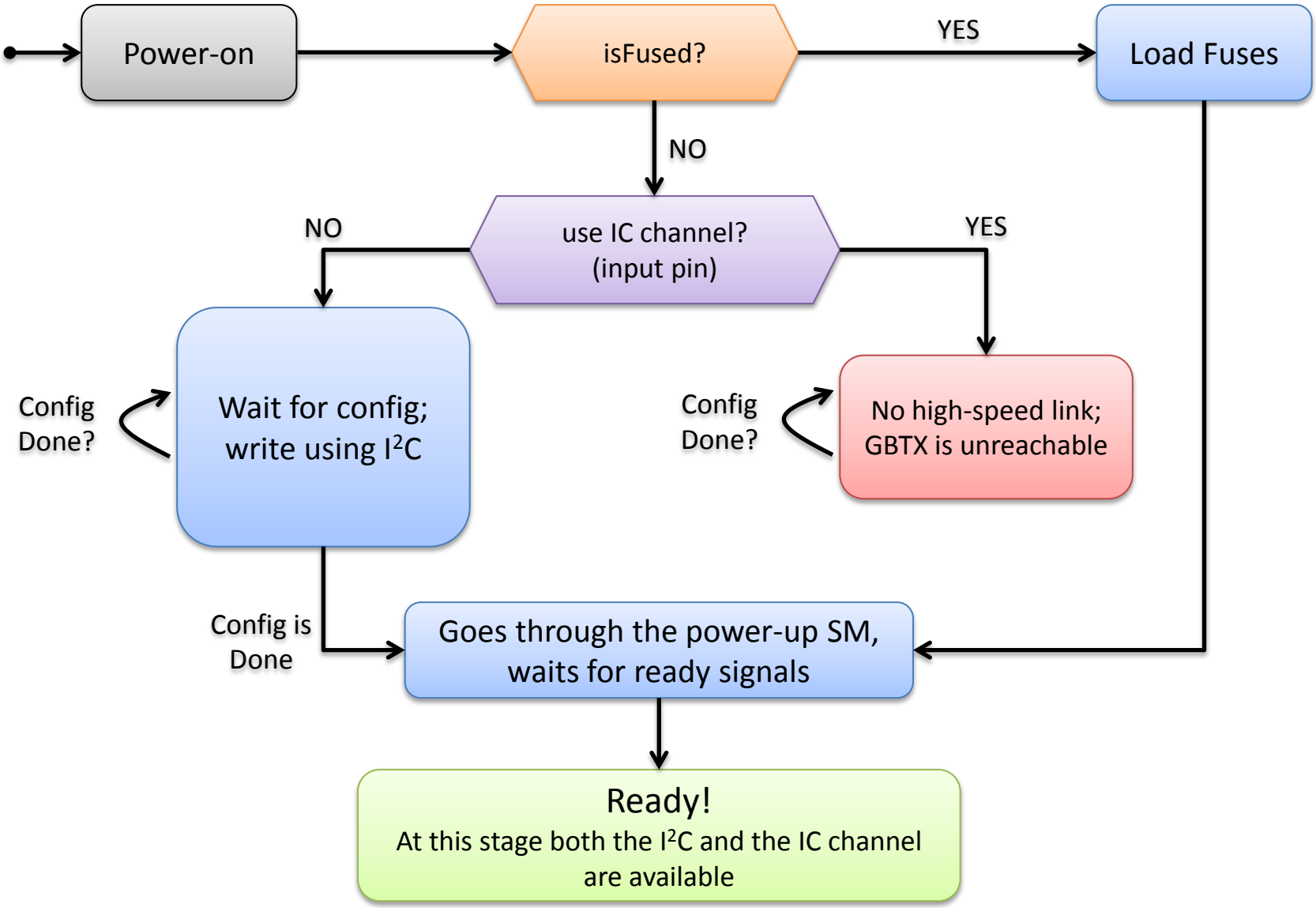


GBTX: a brief review

- Configuration methods
  - There are two methods to communicate with the GBTX
    - I^2C
      - Direct connection using a standard 7-bit addressing I^2C (external pull-up resistors to 1.5V required)
      - Can be connected to the SCA or to an external device for initial prototyping
      - The GBTX is an I2C slave; the address 7'b000_0000 is used for general call
    - Internal Control (IC) channel / External Control (EC) channel (SCA LINK)
      - Requires an high-speed serial link with the GBTX in transceiver mode to work
      - The high-speed serial link can be established using I^2C or by a set of fused values which are loaded after a power-on reset
      - An IC wrapper will be available for the GBT-FPGA for easy read/write access (RAM based)
    - The two methods are mutually exclusive and are selected by one input pin
  - The GBTX provides a two-wire link for the VTRX programming
  - After the optimal configuration settings have been found, the GBTX can be fused in order to have the self-configuration feature enabled (3.3V power supply required for fuse programming)
  - All GBTX in transceiver ("master" GBTX) mode should be fused so that they are operational on power-up

GBTX: a brief review

- Power-up sequence

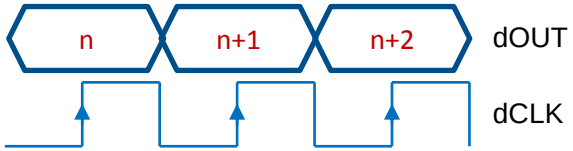


GBTX: a brief review

- Phase Adjustable Output Clocks:
  - 8 programmable clocks
  - 40, 80, 160 and 320 MHz
  - Phase shifts of 50 ps
  - The clock source of the phase shifter's PLL is mode dependent
    - In Transmitter mode, the PLL locks to the REFCLK clock
    - In Receiver mode, the PLL locks to the CDR clock
    - In Transceiver mode, the PLL locks to the CDR clock
  - In receiver/transceiver mode the phase shifter can be used as clock sources for others GBTXs in transmitter mode
  - If phase adjustment of the clocks is not required, the e-link clocks can also provide a stable 40/80/160/320 MHz clock in phase with the source clock. This will help to reduce power

GBTX: a brief review

- E-links
  - Consists of three differential signals
    - dCLK (clock driven by GBTX)
    - dOUT (data line driven by GBTX)
    - dIN (data line from the front-end)



    - Data rate input, output and clock rate can be set independently
      - They can run at 40, 80, 160 and 320 (Mb/s and MHz)
    - Programmable driving current
    - Enable/disable on-chip 100Ω termination

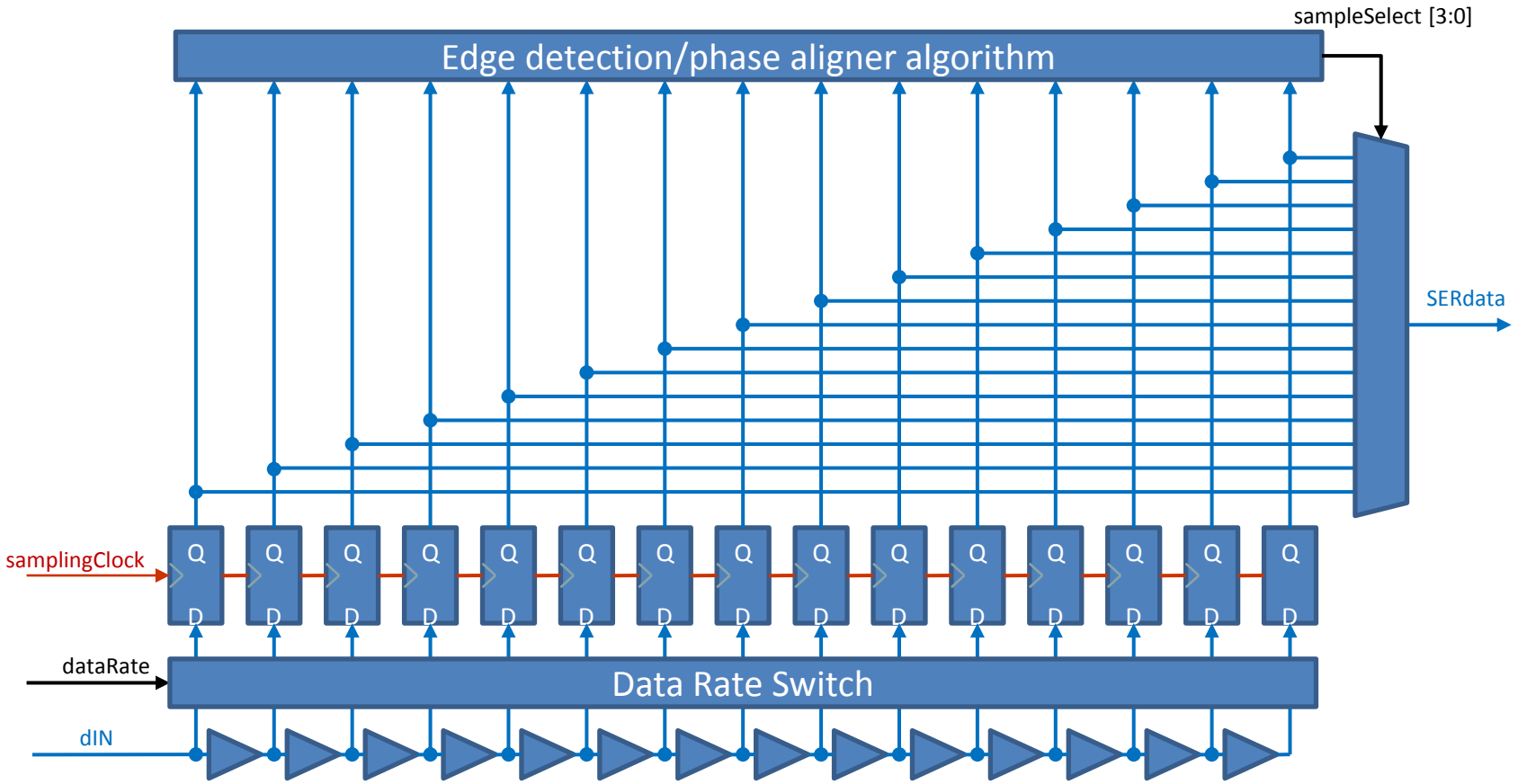
  - Due to the e-links serialization/deserialization architecture, data misalignment (between 40 MHz frame and e-links) can occur (e.g. bit-shifts)

  - Programmable e-link transmitter (eportTX)
    - The dOUT data is driven in anti-phase with the dCLK
    - The front-end should sample the data in the rising edge; dual data rate is also possible
    - Coarse phase adjustment (bit clock) has to be done either in the front-end or in the back-end

  - Programmable e-link receivers (eportRX)
    - Modes
      - Static phase-aligner
      - Automatic phase-aligner
      - Trained phase-aligner

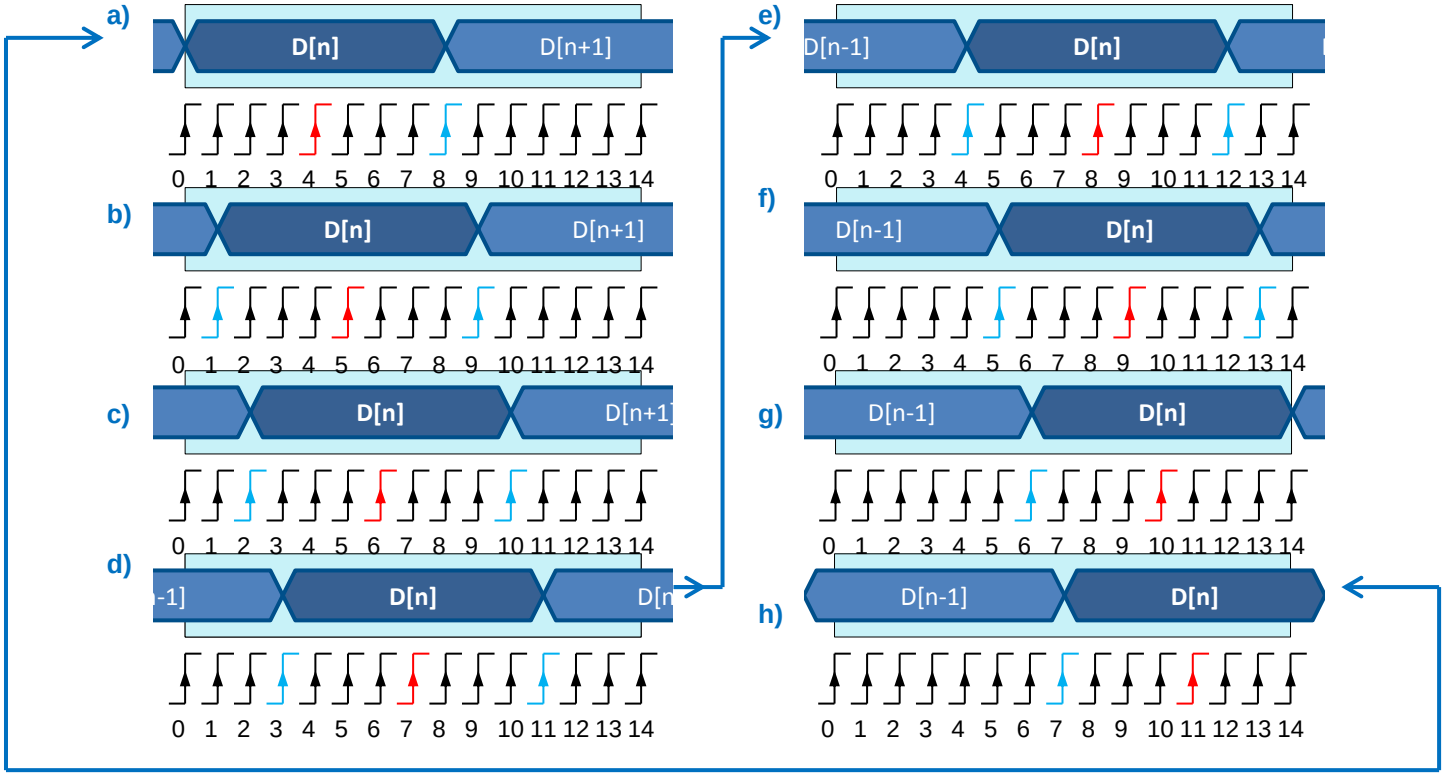
GBTX: a brief review

- E-links receivers (eportRX)
  - The phase aligner value will depend on the line length
  - The data is delayed in order to have a fine-phase alignment (max. delay is $7/4T_{bit}$)
  - There are 15 taps available



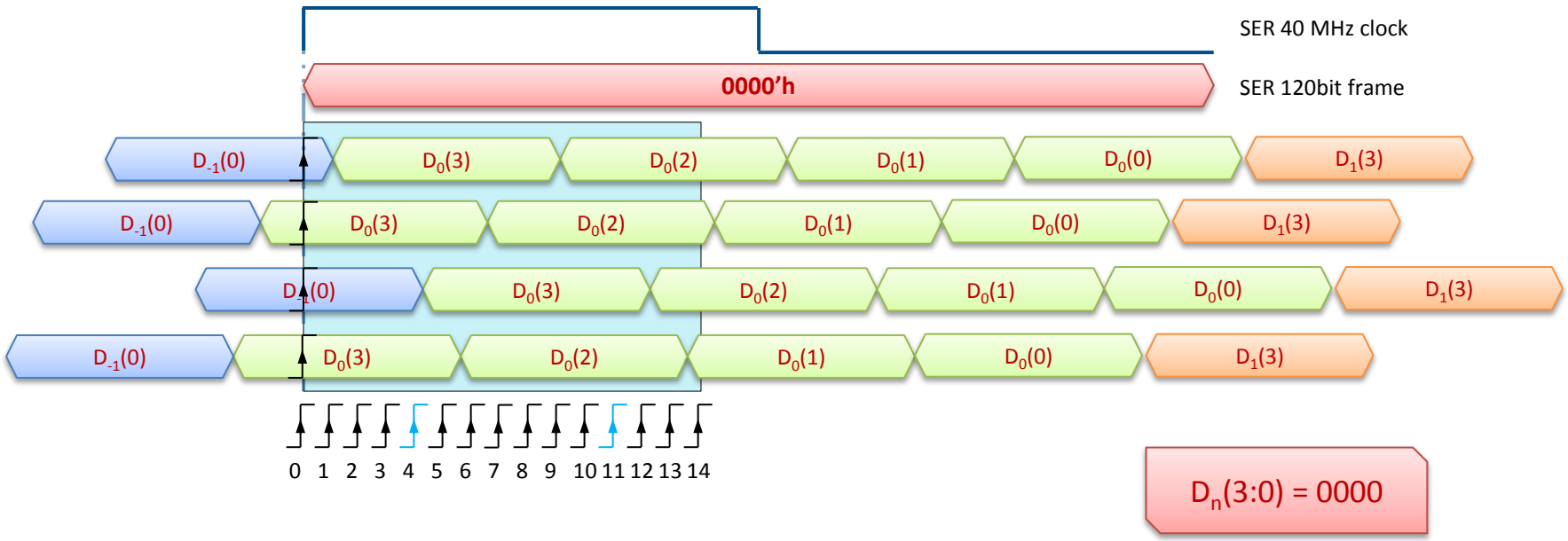
GBTX: a brief review

- E-links receivers (eportRX)
  - Only a fine-phase adjustment (max. $7/4T_{bit}$) is available
  - The automatic phase aligner mode is restricted between the [4; 11] tap
  - After a fixed tap, it can vary ± 3 taps
  - Coarse phase adjustment (bit clock) has to be done either in the front-end or in the back-end
- Automatic phase aligner process:



GBTX: a brief review

- E-links receivers (eportRX) – How to data align a channel?
  - Example:
    - Group at 160 Mbit/s
    - The automatic phase aligner mode is restricted between the [4; 11] tap



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- E-links receivers (eportRX) – How to data align a channel?
  - Example:
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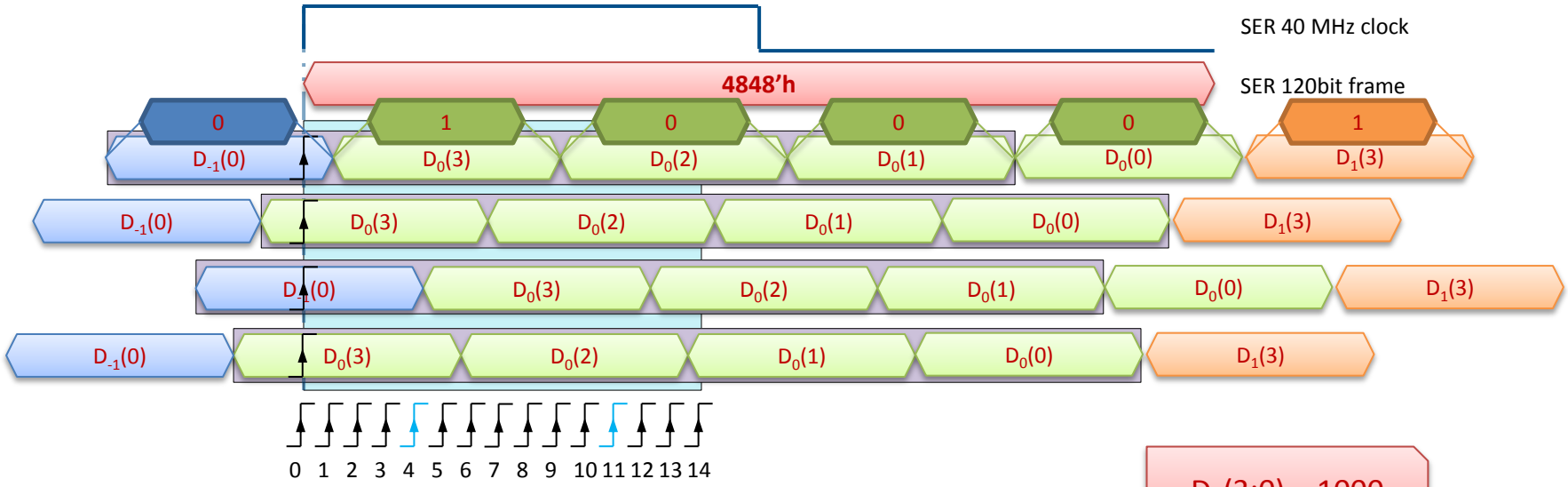
Set the data to b'1000';
This will allow to identify the $D_n(3)$ position



$D_n(3:0) = 1000$

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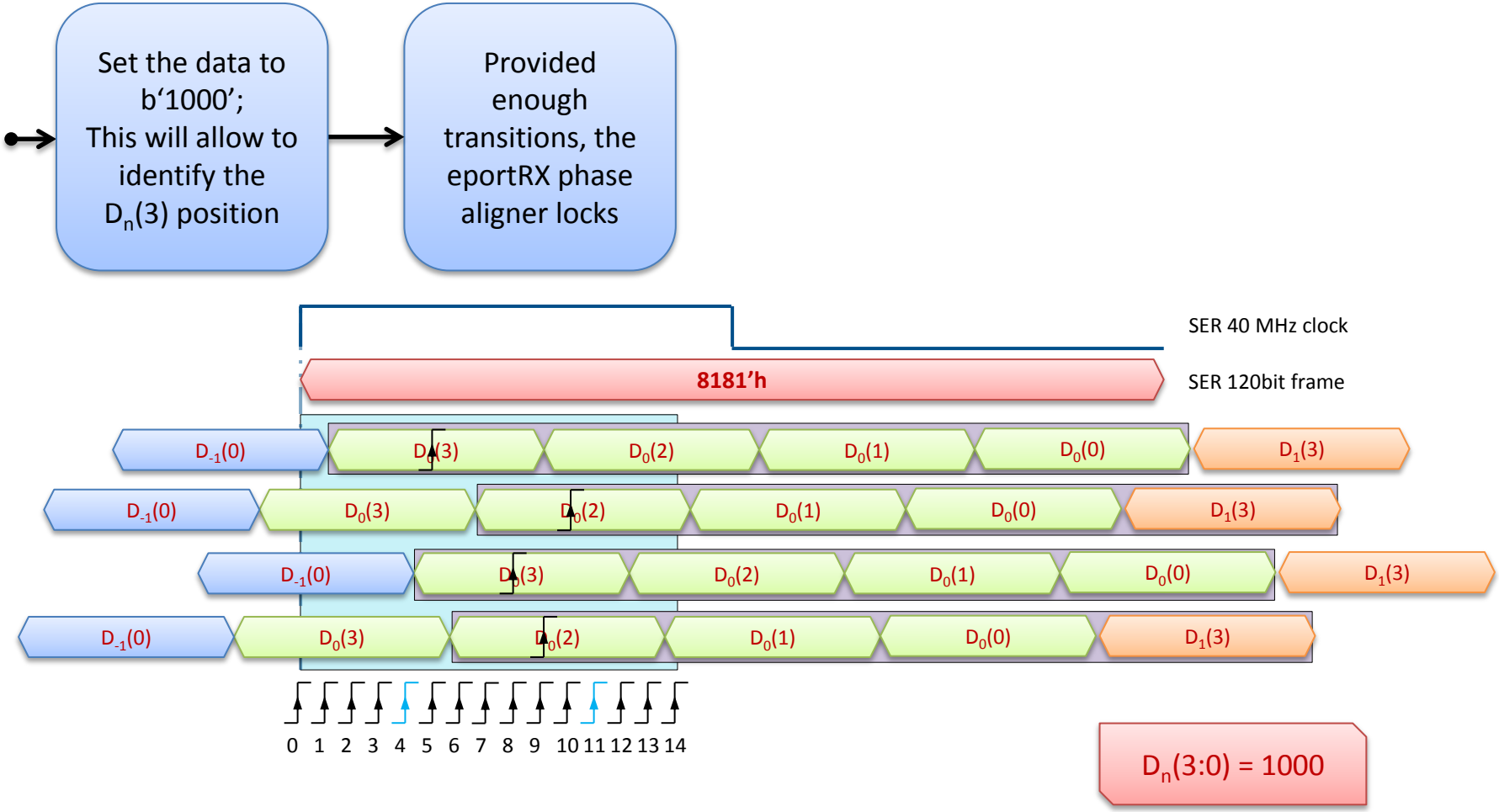

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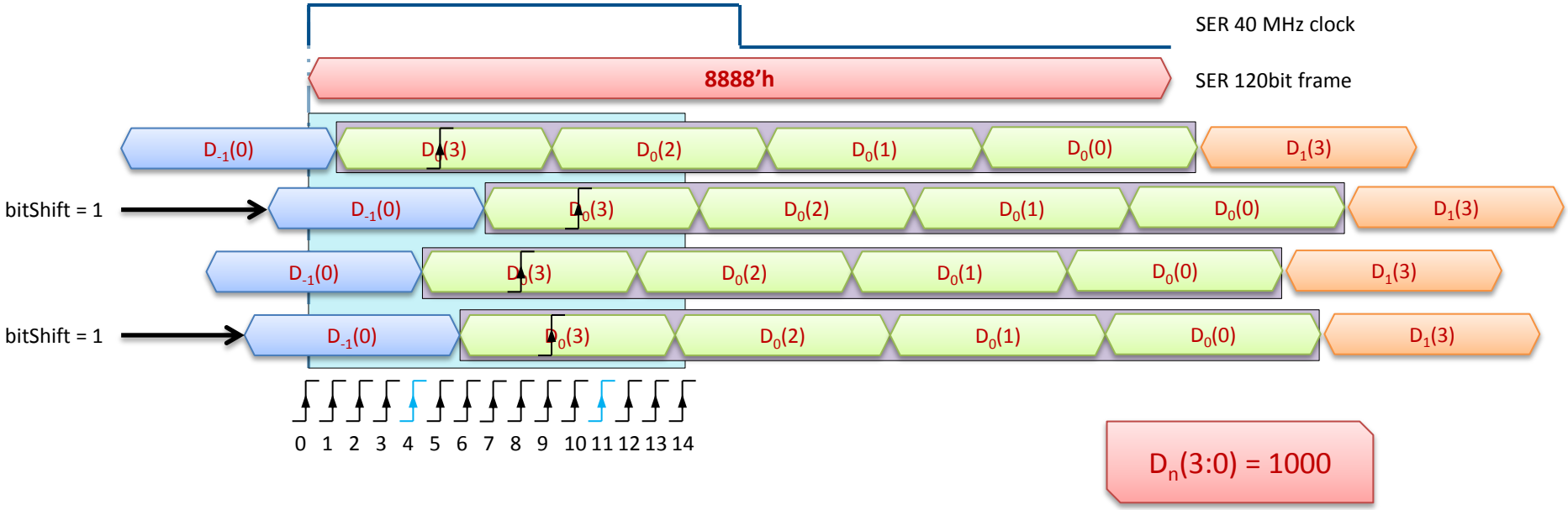

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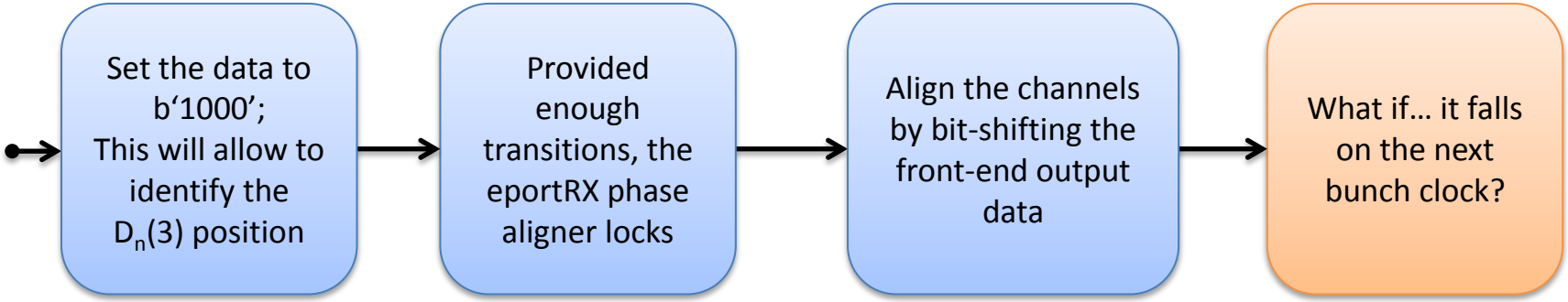
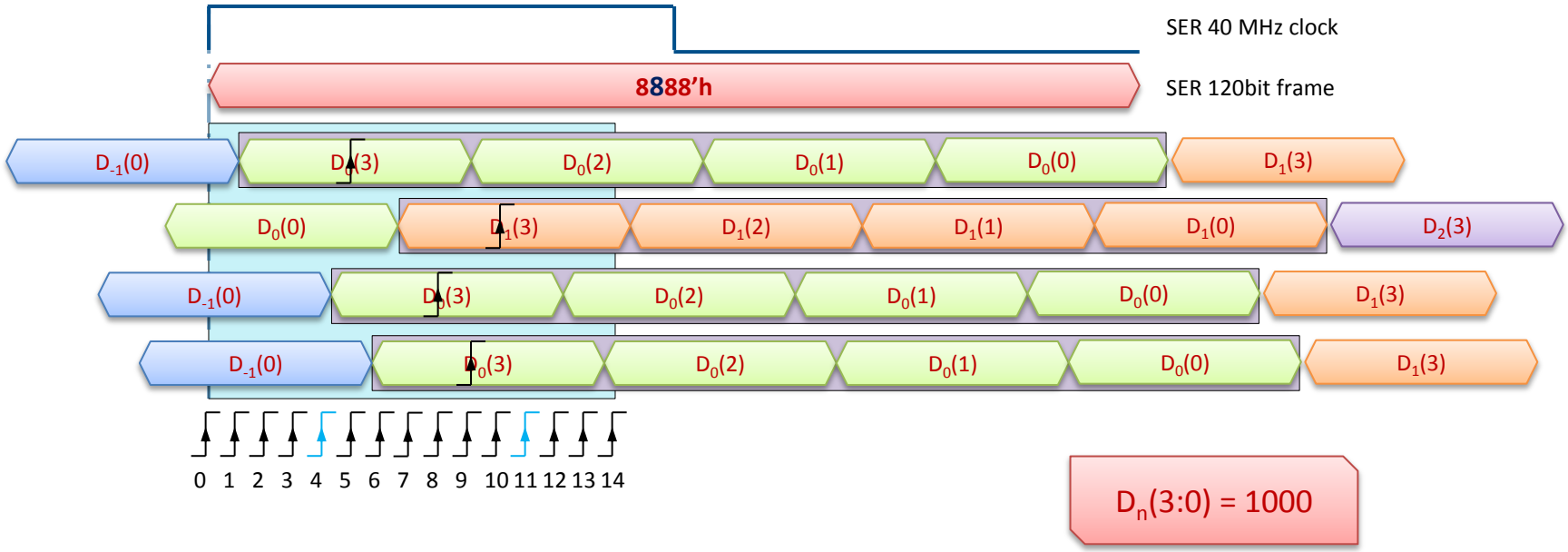
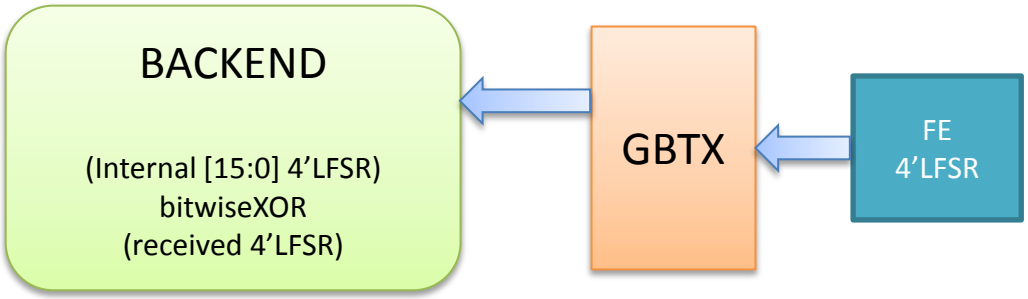


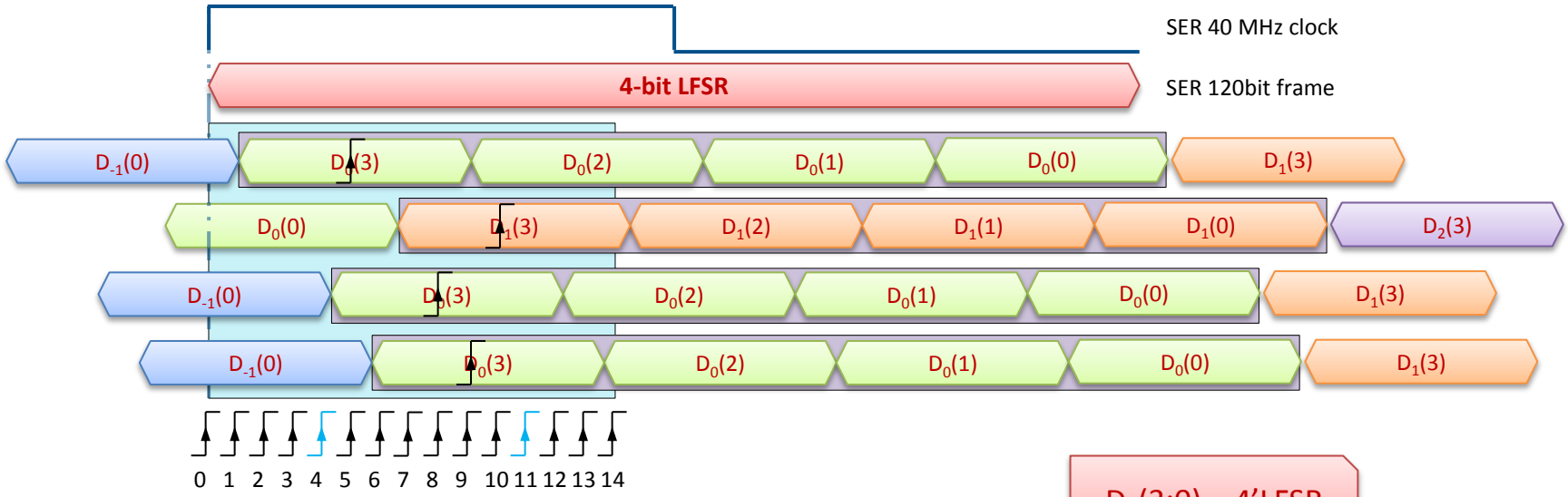


GBTX: a brief review

- E-links receivers (eportRX) – How to data align a group?
  - Example:
    - Implement a 4-bit LFSR pseudo-random pattern (overlaps every 16 words)
    - Use the same pattern in the back-end and perform a bitwise XOR with the received frame
    - Keep shifting the front-end output data until you have bitwise XOR = 4'b0000



What if… it falls on the next bunch clock?



$D_n(3:0) = 4'LFSR$

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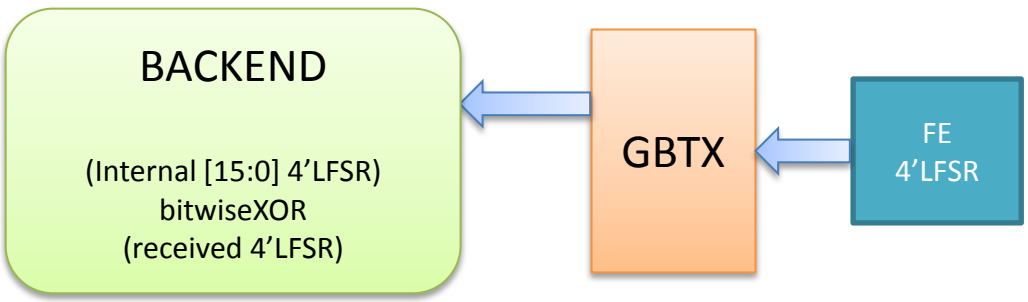

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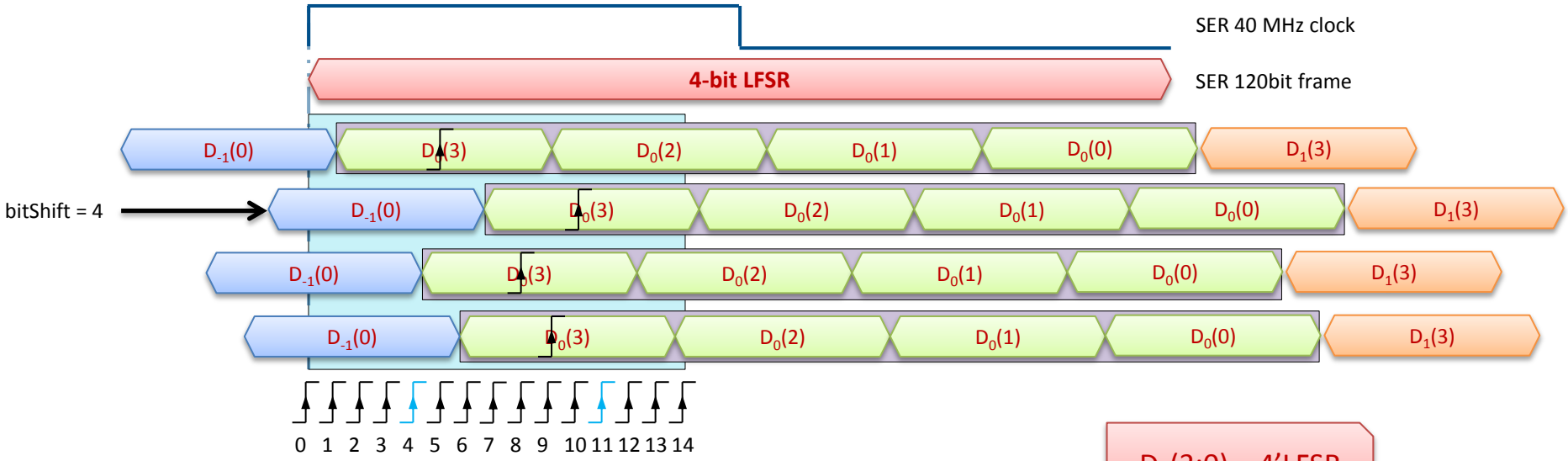

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GBTX: a brief review

– E-links receivers (eportRX) – How to data align a group?

In order to use this method (data rate dependent):

- Add a unique pattern which enables you to identify the e-link MSB to your FE and BE
  - e.g,
    - 10'b *if 80 Mb/s*
    - 1000'b *if 160 Mb/s*
    - 1000 0000'b *if 320 Mb/s*
- Add a 4-bit LFSR pattern for group/frame data alignment to your FE and BE
  - e.g
    - 4LFSR[1:0] *if 80 Mb/s*
    - 4LFSR[3:0] *if 160 Mb/s*
    - {4LFSR[3:0], 4LFSR[3:0]} *if 320 Mb/s*
- Perform the bitwise XOR using the whole group for group alignment
- The eportTX (e-link transmitter) can use the same method
- You only need to do this once – then you can save and reuse the same configuration
  - e.g, use the eportRX trained phase aligner mode
- You can use the SCA to control the I2C channel of your FE

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14

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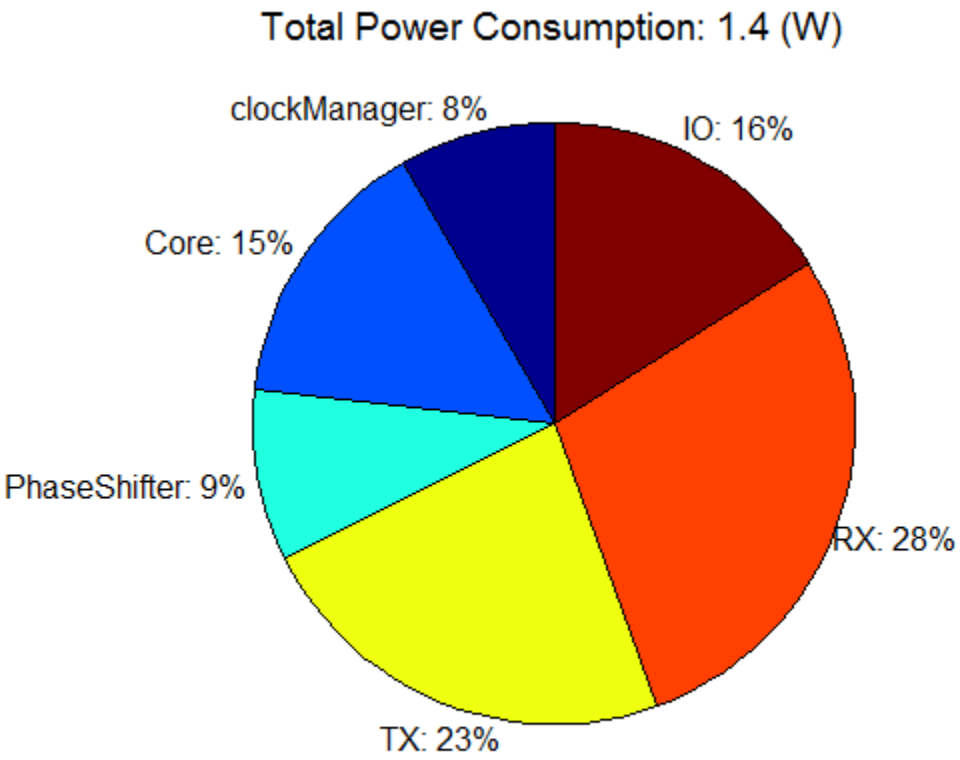
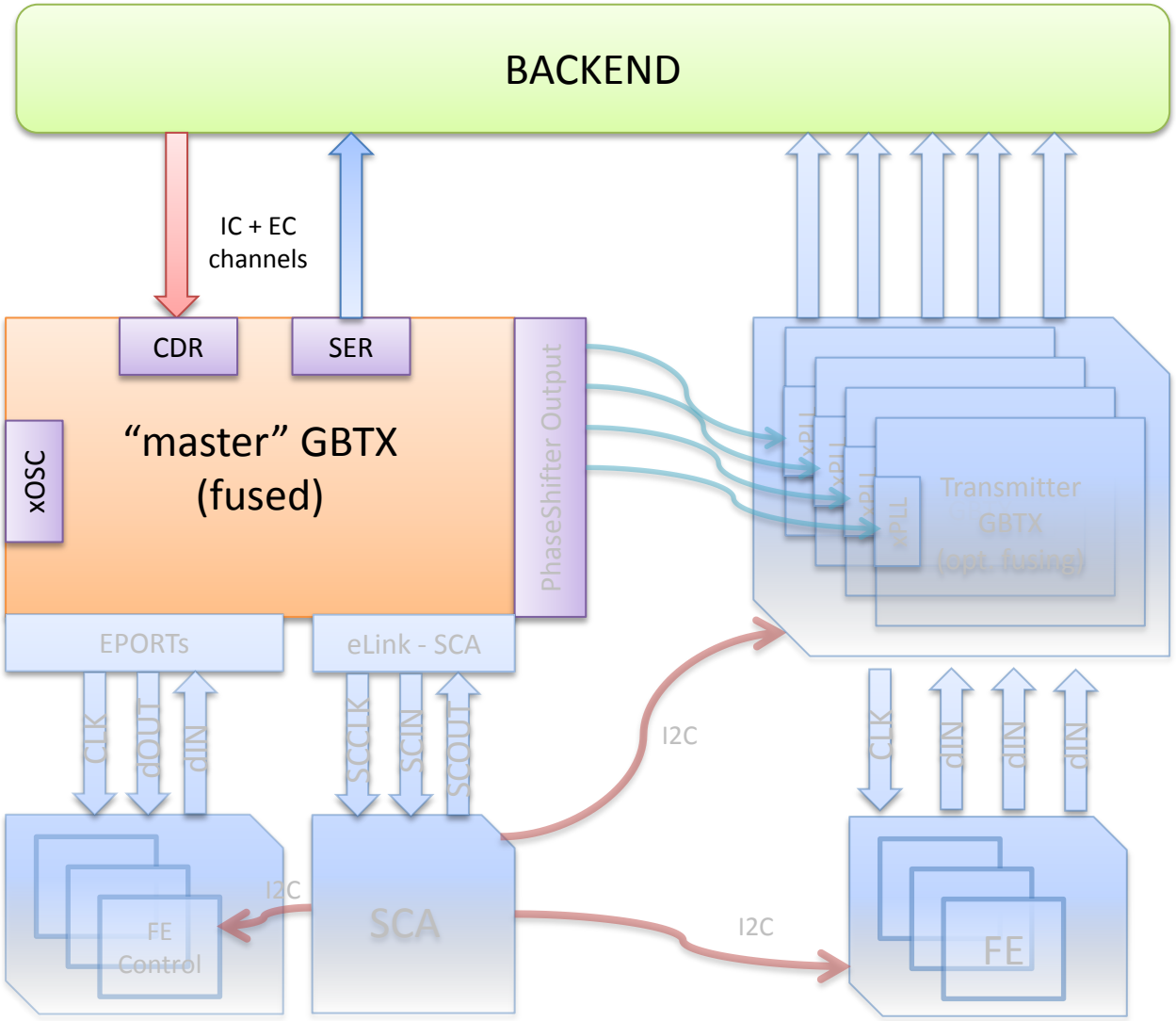
GBTX: a brief review

- Power consumption example
  - Transciever mode
  - GBT Frame
  - All clocks enabled, multiple group data rates, I2C conn



Study-case: GBTX transceiver as clock source

- GBTX transceiver as clock source for multiple GBTXs transmitters



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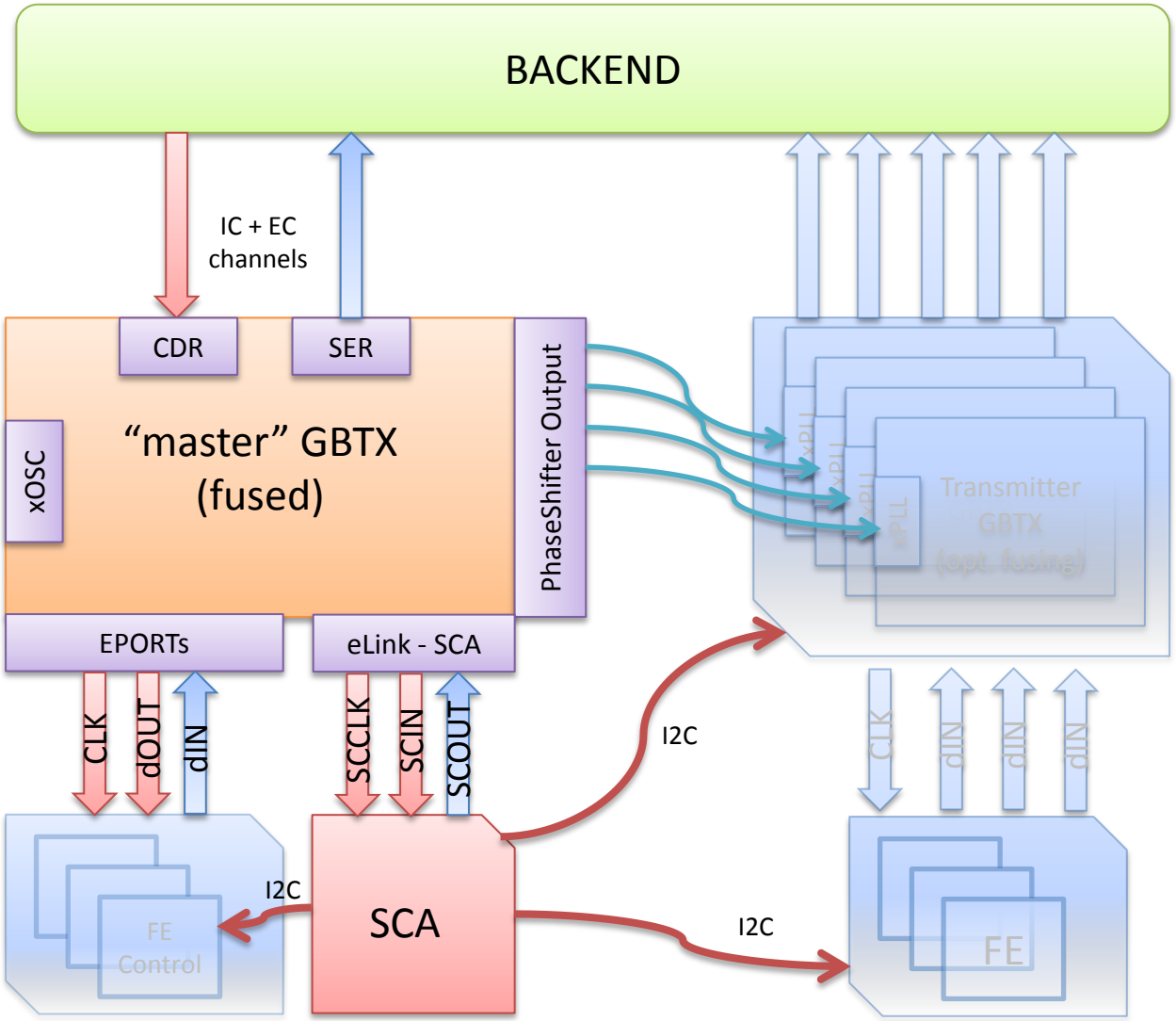

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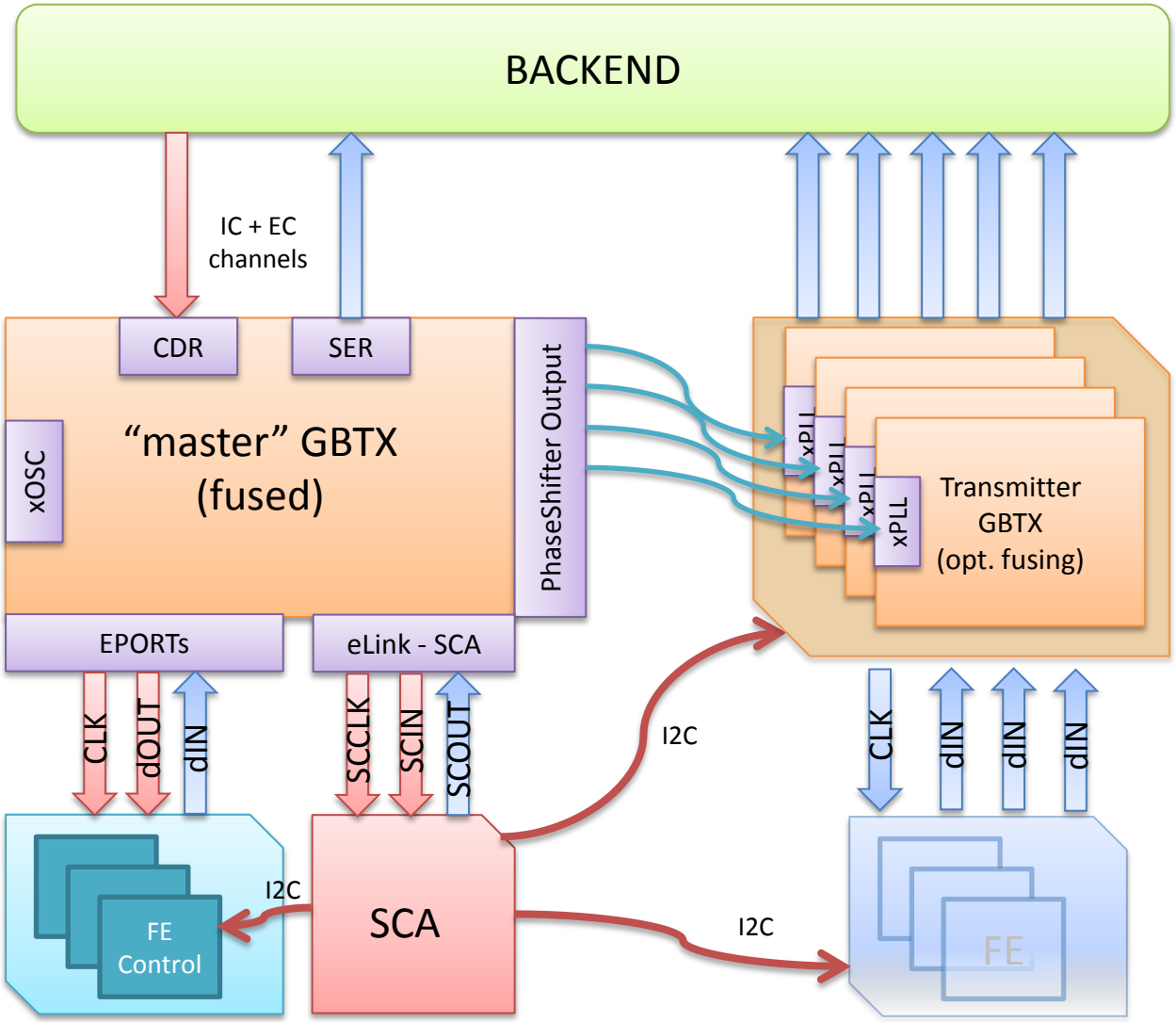

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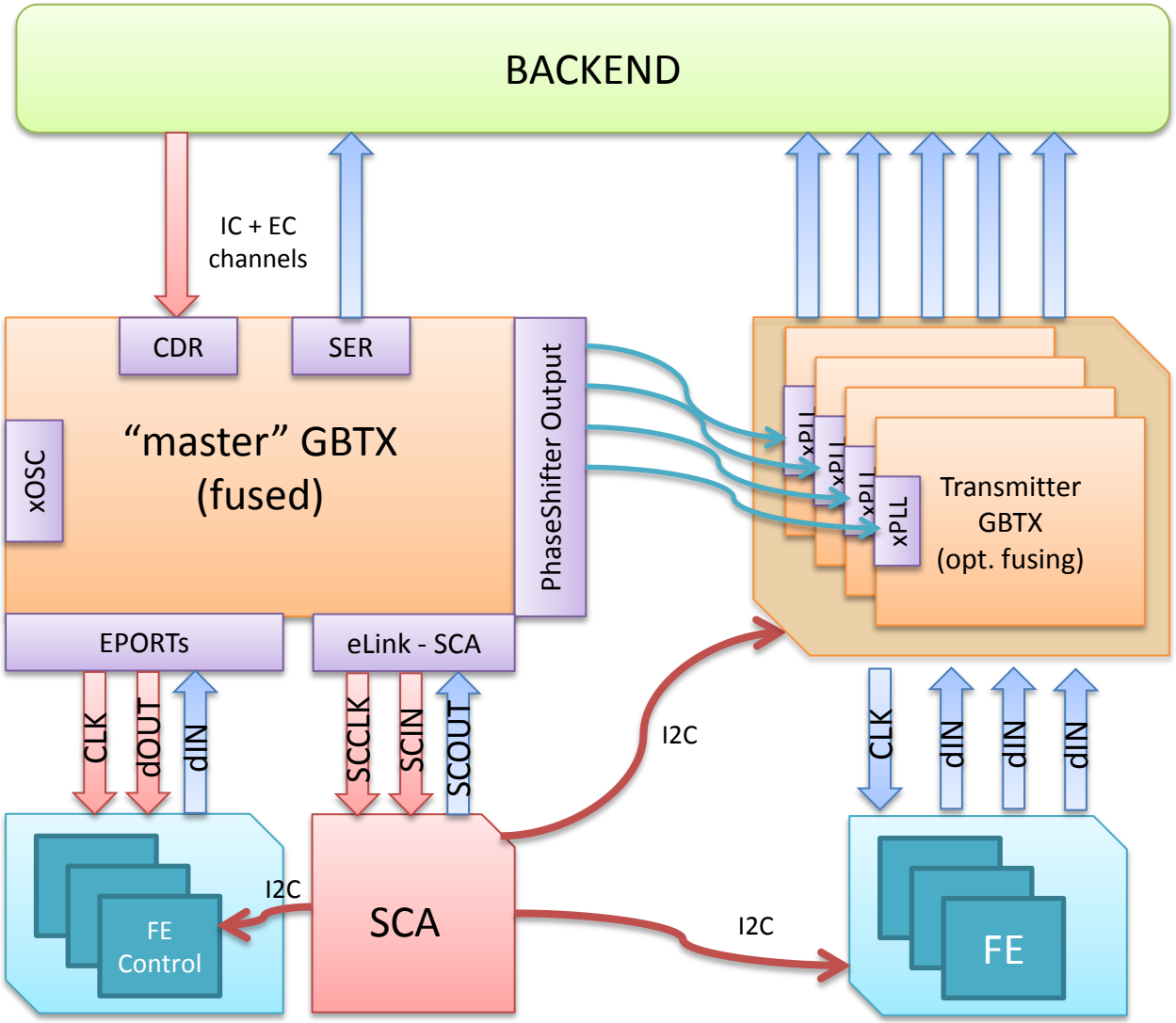

BACKUP SLIDES

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- Align eportRX: find the correct position with the 4'LFSR