GBT Demo Board

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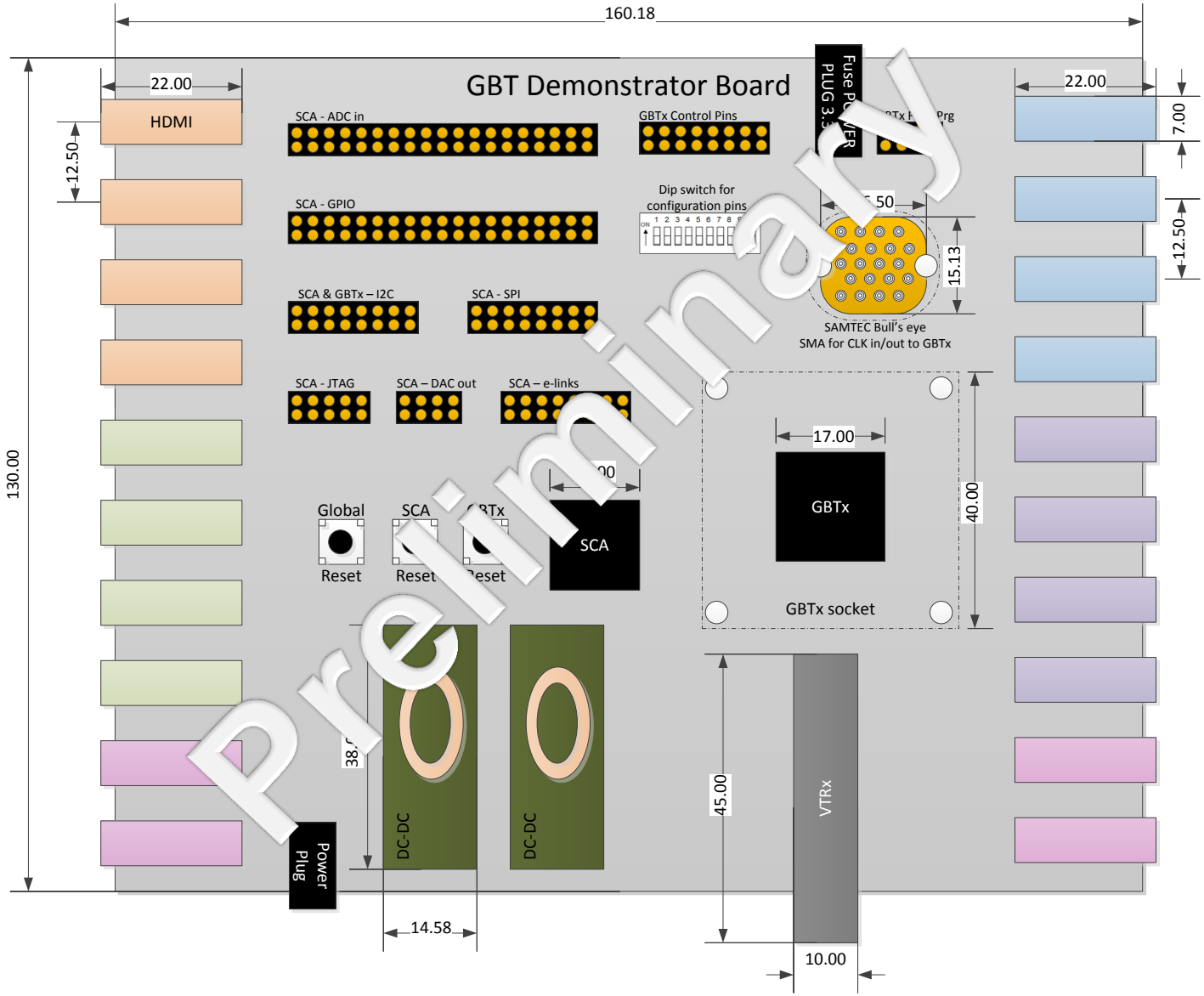
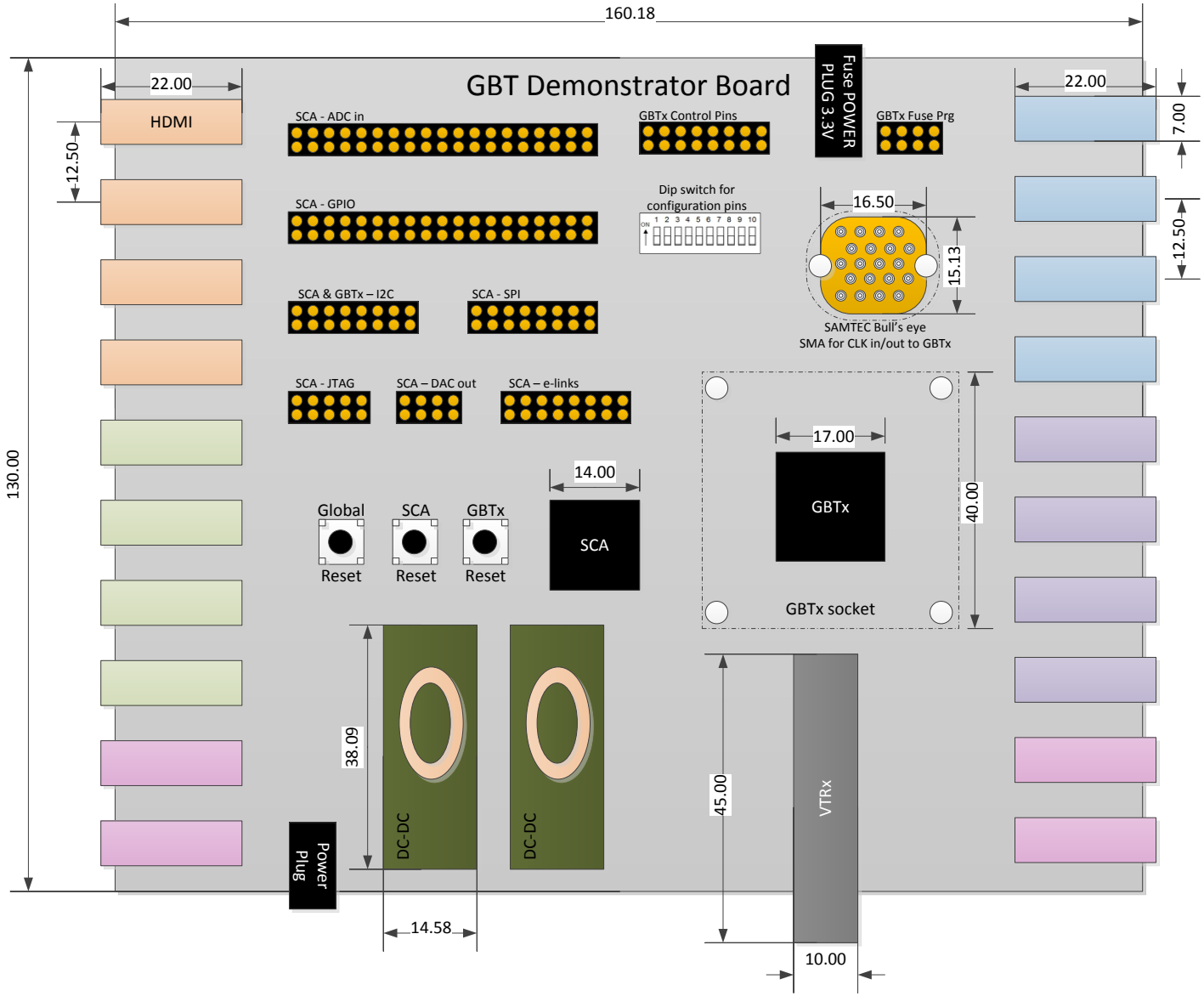
Concept

- **Reference for further designs**
  - Schematics
  - Layout
- **Full scale system test of the GBT chipset**
  - All the GBT chipset ASICs mounted on one single board
    - GBTx
    - SCA
    - VTRx
    - DC-DC
  - Allow extended radiation tests of the full system
    - All the chips located on the same area
- **Characterize the versatile link with the GBTx**
- **Ease the tests of FE chips prototypes with a real GBT chipset**
  - Simple connectivity via HDMI
  - One e-link per HDMI connector
- **Ease beam tests**
  - 100% rad-hard design for beam tests
    - No other active devices
- **Provide a GBTx programmer board**
  - I2C configuration
  - Fuse programming
  - Socket footprint available


GBT Demonstrator Board
160.18
130.00
22.00
22.00
HDMI
12.50
7.00
12.50
SCA - ADC in
GBTx Control Pins
SCA - GPIO
Dip switch for configuration pins
SCA & GBTx – I2C
SCA - SPI
15.13
SAMTEC Bull's eye
SMA for CLK in/out to GBTx
SCA - JTAG
SCA – DAC out
SCA – e-links
17.00
GBTx
40.00
Global
Reset
SCA
GBTx socket
DC-DC
DC-DC
45.00
VTRx
Power Plug
14.58
10.00
Preliminary


160.18
GBT Demonstrator Board
22.00
HDMI
12.50
130.00
SCA - ADC in
GBTx Control Pins
Fuse POWER PLUG 3.3V
GBTx Fuse Prg
22.00
7.00
12.50
SCA - GPIO
Dip switch for configuration pins
16.50
15.13
SAMTEC Bull's eye
SMA for CLK in/out to GBTx
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14.00
Global
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Reset
SCA
GBTx socket
38.09
DC-DC
DC-DC
45.00
VTRx
Power Plug
14.58
10.00

GBTx

Preliminary

- **E-links:**
  - **Full payload** down and up for:
    - E-links x4 (160Mbps) with any Mode (GBT, Wide, 8b/10b)
    - E-links x8 (320Mbps) with any Mode (GBT, Wide, 8b/10b)
  - **Half payload** for e-links x2 (80Mbps)
  - Connection to SCA
- **Clocks**:
  - Ref Clk Input for external synchronization
  - 4 TTC Clk outputs for Bunch Clock deskewing and distribution
- **Control**:
  - I2C connection to access the config & status registers
  - Mode & config pins accessible via dipswitch & header
- **Programmation:**
  - Space & footprint to install a socket if needed
  - 3.3V powering possibility for fuse programming

SCA, VTRx & DCDC

Preliminary

- **SCA**
  - IOs:
    - 4 DAC pins => header
    - 32 GPIOs => header
    - 32 ADCs => header
  - Control:
    - JTAG connector => header
    - SPI connector => header
    - 4x I2C ports => header
    - E-link internally connected to the GBTx
- **VTRx**
  - MM & SM pinouts
- **DC-DCs**:
  - Rad Hard modules
  - 2.5V for the VTRx
  - 1.5V for both the GBTx and the SCA

Plan

- Produce *a few* of these modules for
  - System Testing
  - Radiation Testing
  - GBTx programming

NO MASS PRODUCTION !

- Provide a validated reference design to users
  - Schematics
  - Layout
- Expected
  - Autumn 2014 (together with the chips)