AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

SALT chip design in TSMC 130 nm

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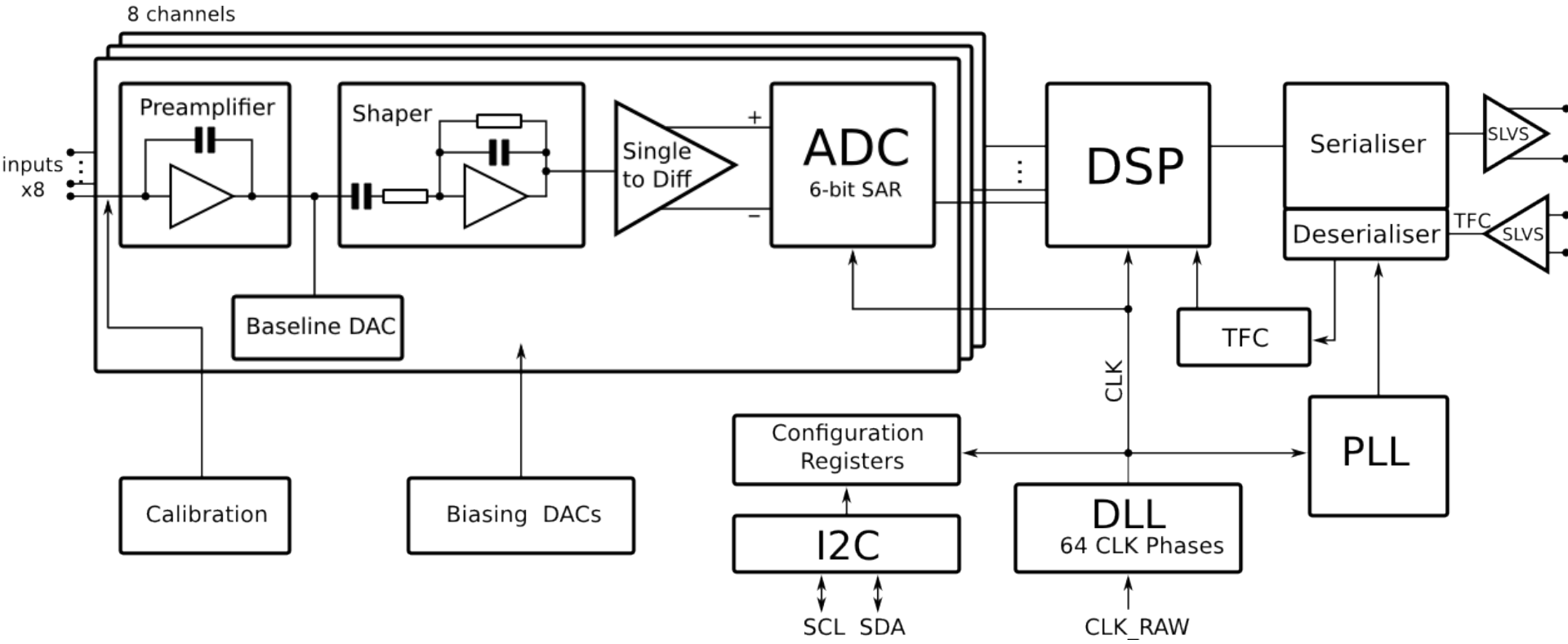
Outline

- Introduction
- Preliminary measurements of first structures in TSMC 130 nm
- SALT ASICs for February submission

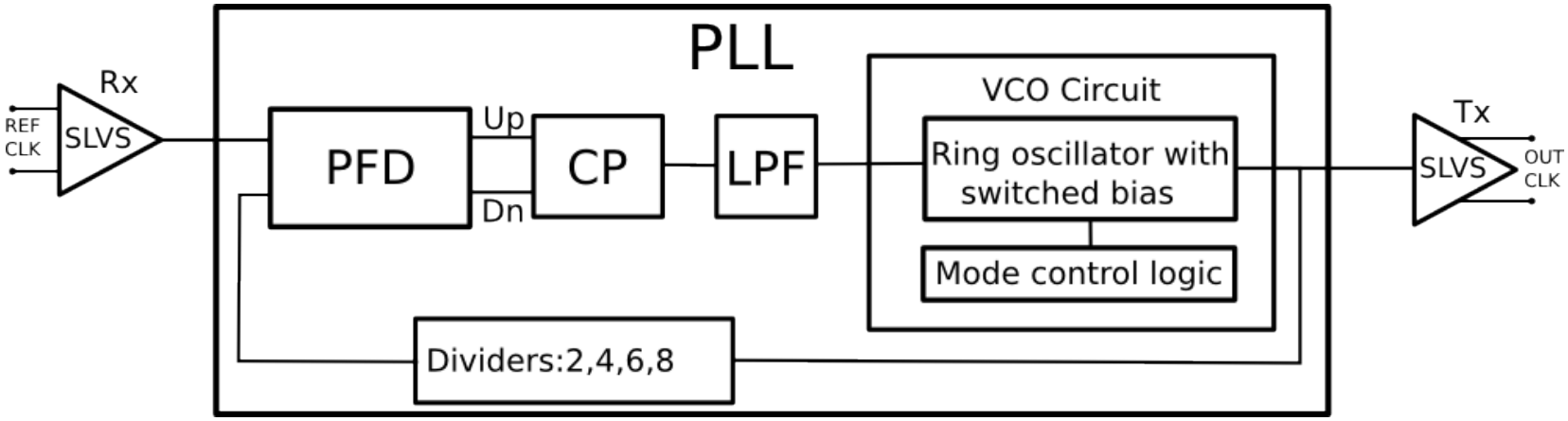
Introduction
The Goal - SALT readout ASIC for UT

Short term goal - SALT8 – 8-channel version of SALT chip



SALT8 architecture has all important features of the 128-channel SALT

1st PLL and SLVS prototypes in TSMC 130nm Architecture/Specs/Results



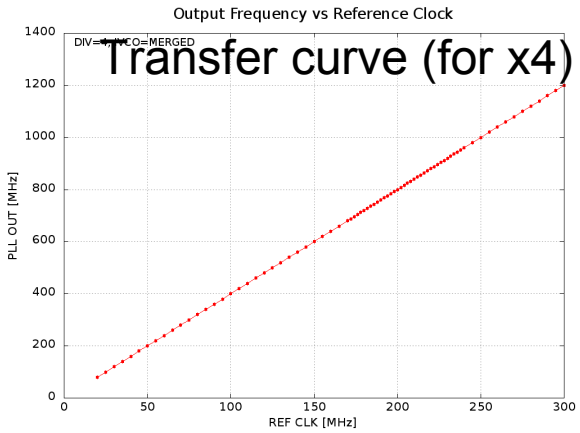
PLL specs/results:

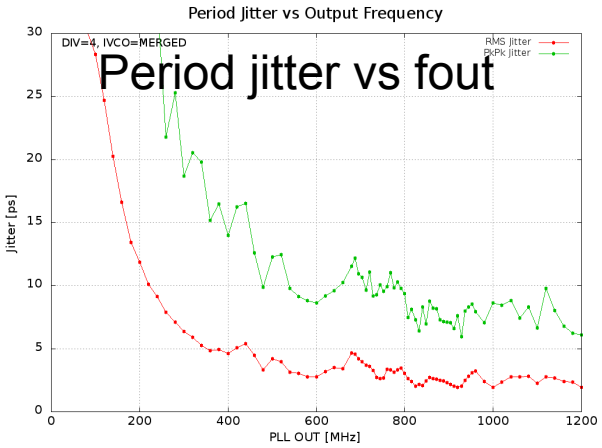
- Input frequency 10-300 MHz
- Output freq. range 80-1200 MHz
- Dividers 2/4/6/8
- Power consumption ~1uW/1MHz
- Measured Period jitter (rms) ~ 3-10 ps (in most of the range)

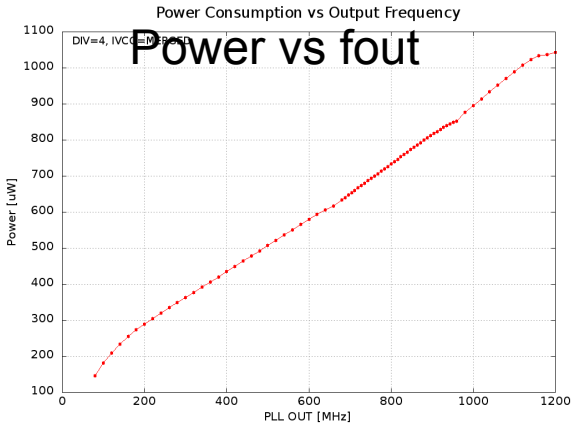
SLVS I/O results:

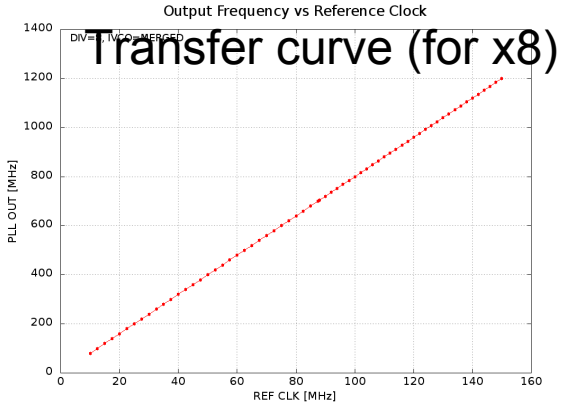
- Verified with PLL measurements (no dedicated meas. done)
- Receiver verified for 10-300 MHz
- Driver verified for 80-1200 MHz

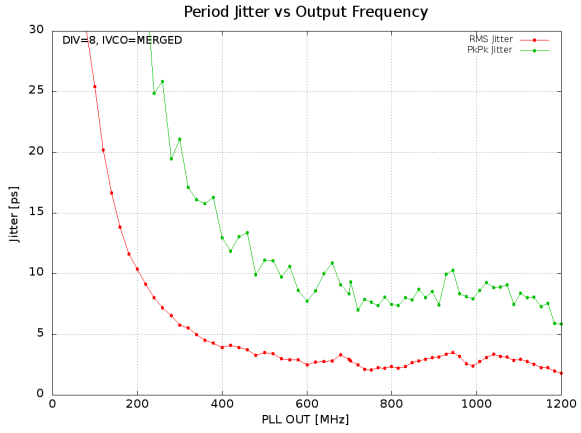
1st PLL and SLVS prototypes in TSMC 130nm
Preliminary measurements

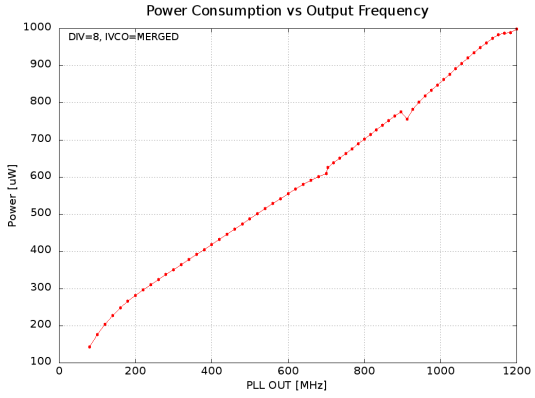










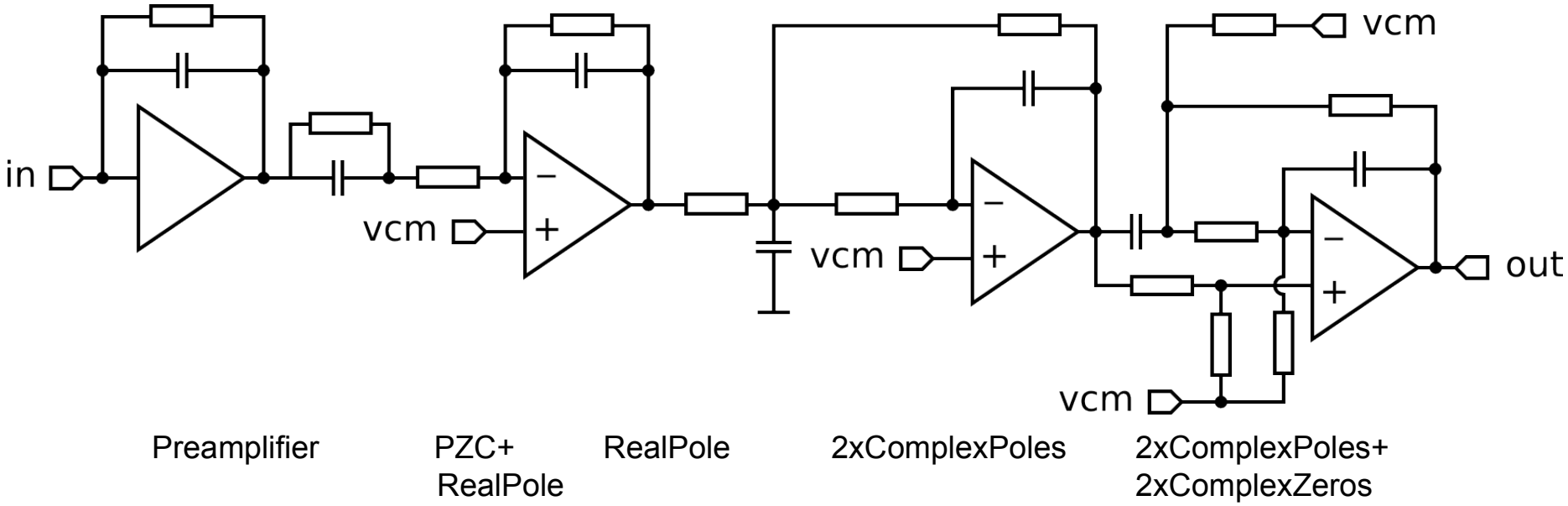


Very good PLL performance, reflected in frequency range, jitter, and power consumption, found in preliminary measurements

- First conclusion: measurements agree with simulations – good!

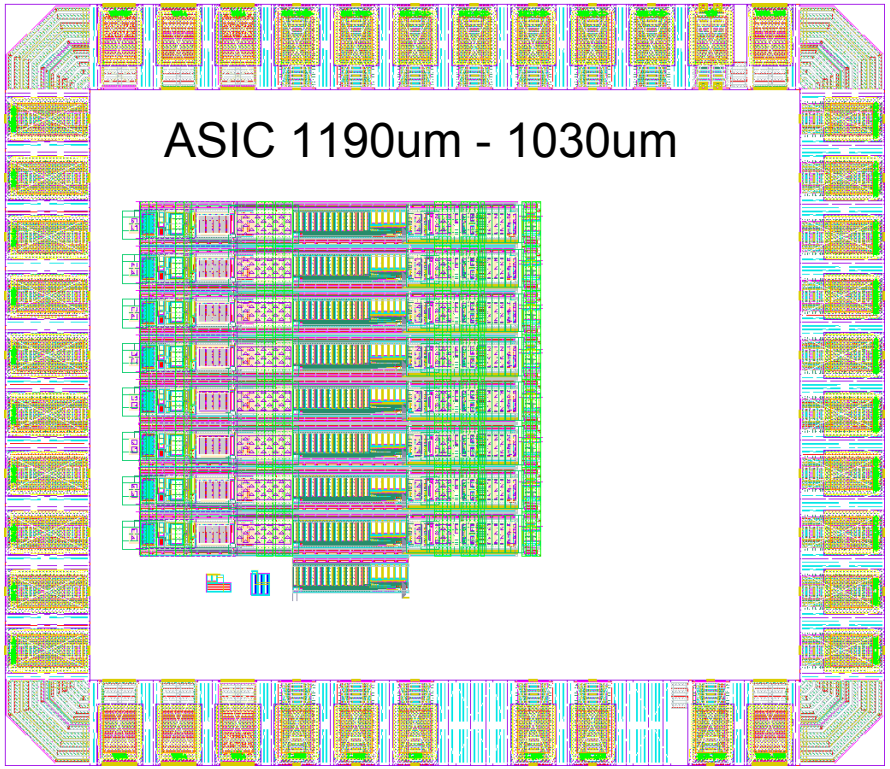
Analog Front-end Architecture

Simplified circuit diagram



With Preamplifier + PZC and three Shaper stages (Integrator + MultipleFeedback + Boctor) the required transfer function can be obtained

8-channel Front-end ASIC

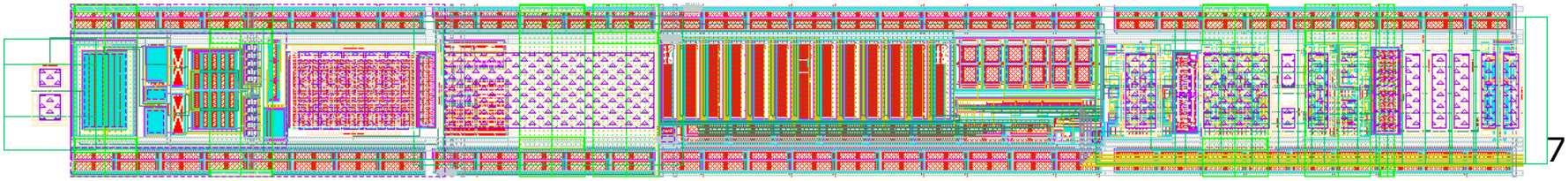


8-channel front-end ASIC:

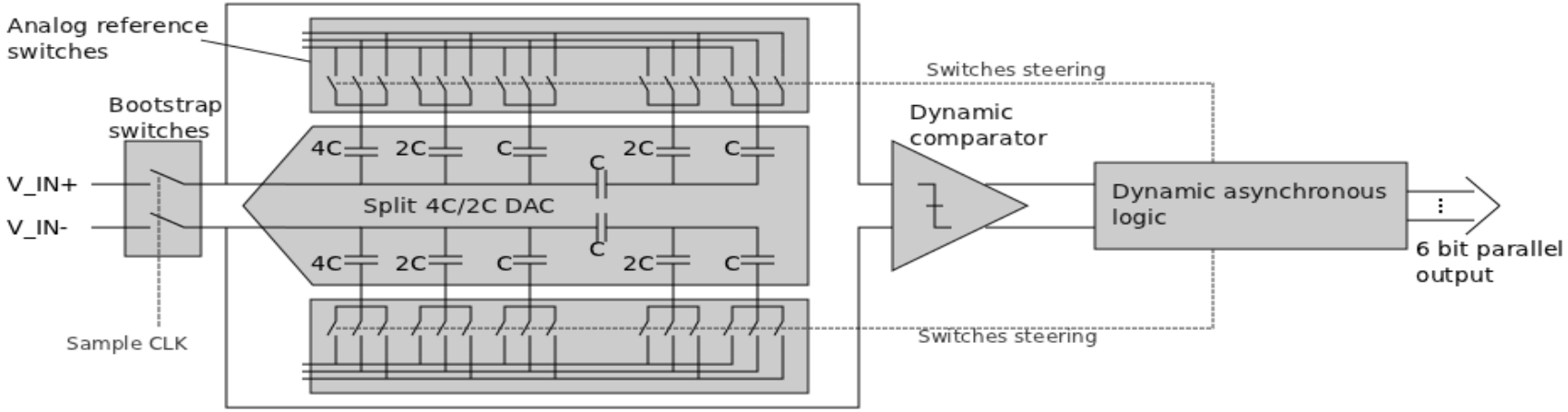
- preamp&shaper completed

  Analog front-end was not yet optimized as it was in IBM...
- DACs completed
- Buffers (to see signal after each stage) completed
- Biasing circuitry in progress
- Chip integration in progress
- Progress ~90% (if there are not technology problems)
- One more week needed

Front-end 530um - 60um



6-bit SAR ADC
Architecture&Design considerations



Architecture of 6-bit ADC

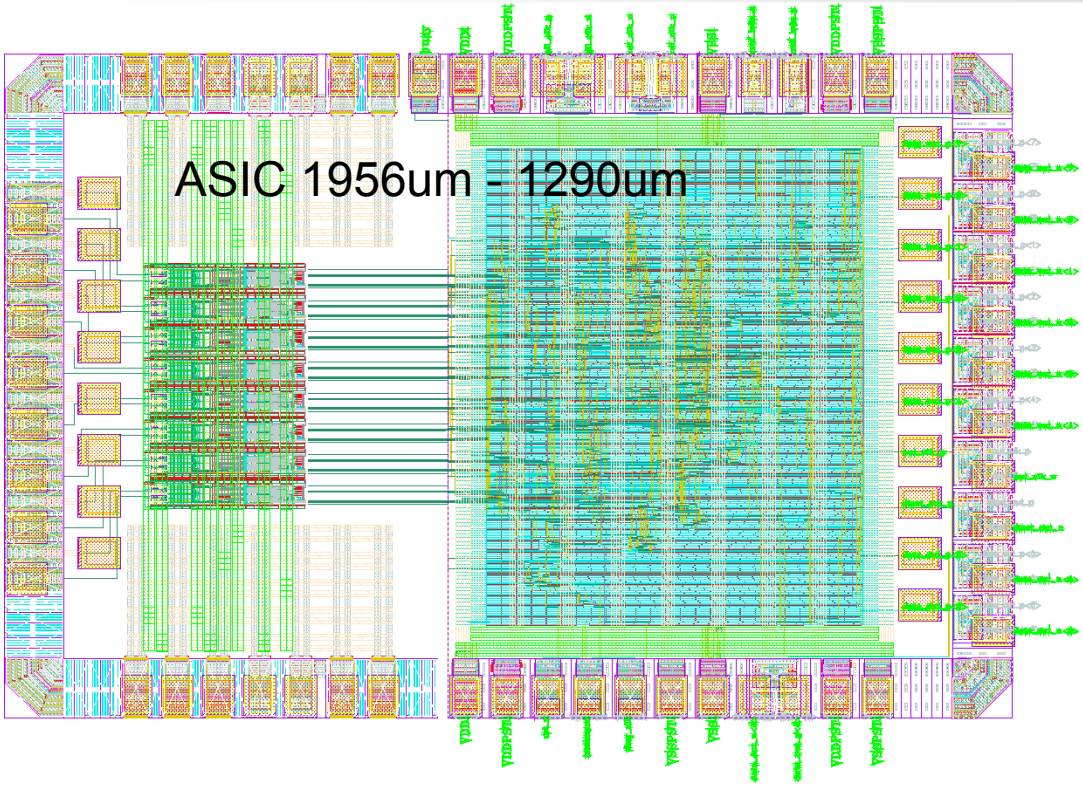
- Differential segmented/split DAC with MCS switching scheme – ***ultra low power***
- Dynamic comparator – ***no static power consumption, power pulsing for free***
- Asynchronous logic – no clock tree – ***power saving, allows asynchronous sampling***
- Dynamic SAR logic – ***much faster than conventional static logic***

Design consideration:

- Variable sampling frequency (up to >80 MS/s) and power consumption
- Power consumption ~0.4 mW at 40 MS/s
- 60 µm pitch, ready for multichannel integration

M. Firlej, T. Fiutowski, M. Idzik, J. Moroń,K. Świentek, "A fast, low-power, 6-bit SAR ADC for readout of strip detectors in the LHCb Upgrade experiment", Journal of Instrumentation, JINST 9 P07006, July 2014

8-channel 6-bit SAR ADC ASIC

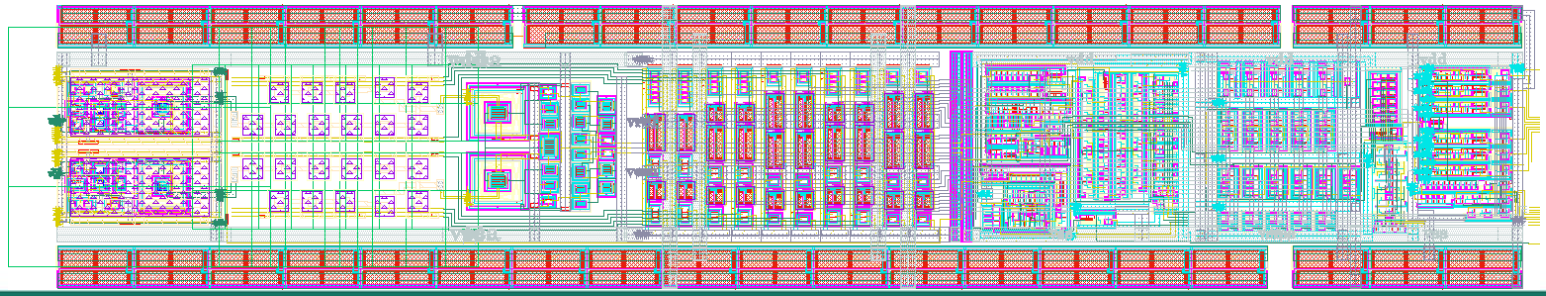


8-channel ADC ASIC specs&simulation_results (after extraction):

- f_{sample} > 80 MHz
- ENOB > 5.9
- Power@40MHz ~0.4mW/chn

Chip completed!

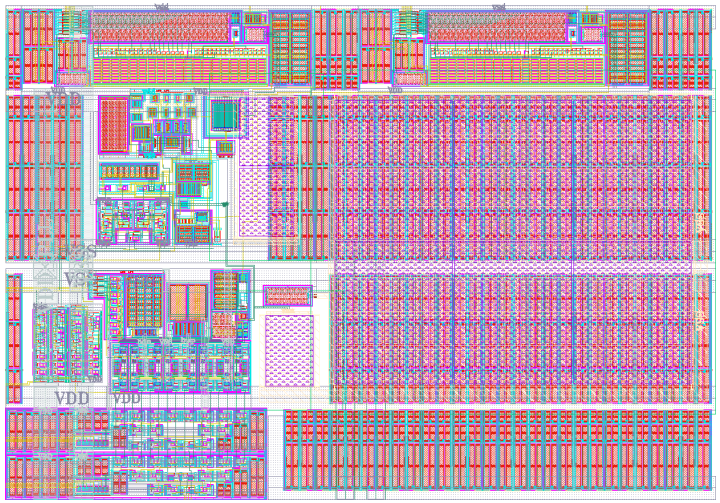
- some filling errors to be discussed with IMEC...



ADC
300um - 60um

PLL, DLL, serializer ASIC

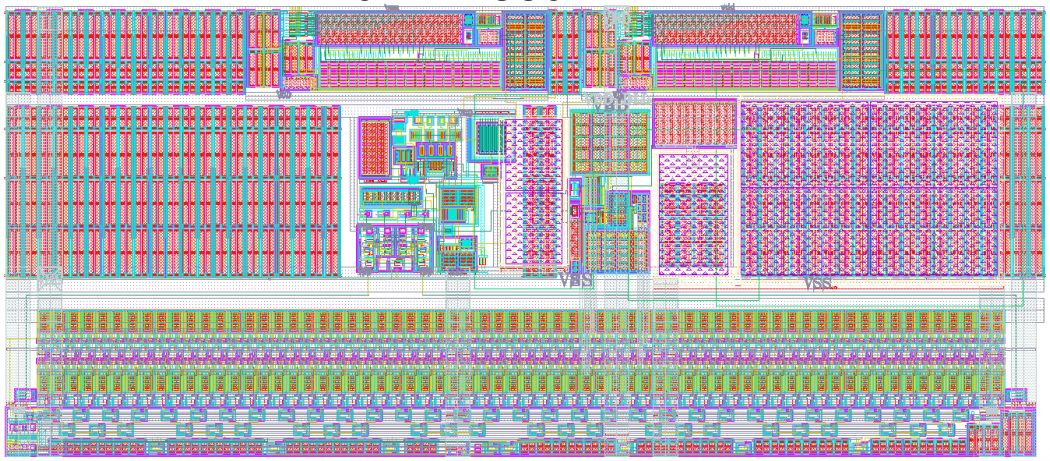
PLL 300um - 210um



PLL features (after extraction):

- Default input frequency 40 MHz
- Output freq. range 80-400 MHz
- Dividers 2/4/6/8
- Power consumption <1mW
- Multiplexing – 2 output phases selected from 16 uniform phases
- Sim. Period jitter (rms) ~ 2 ps
- Power ON/OFF switch

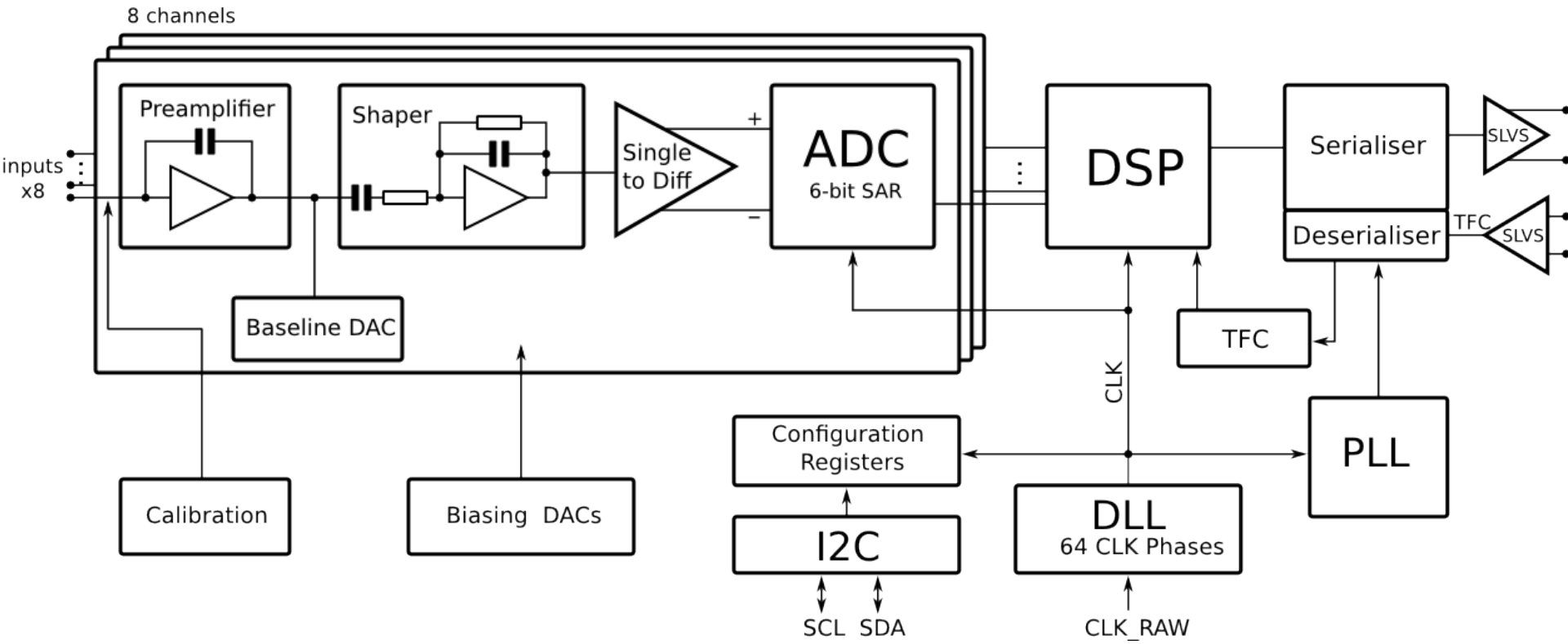
DLL 422um - 185um



DLL features (after extraction):

- Default input frequency 40 MHz
- Power consumption <1mW
- Multiplexing – 1 output phase selected from 64 uniform phases
- Sim. Period jitter (rms) ~ 6 ps
- Power ON/OFF switch

SALT8 – status



A ~month needed to complete SALT8 chip

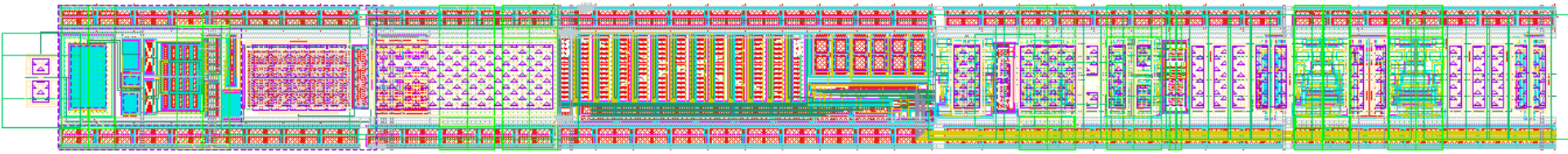
Thank you for attention

Intro
SALT – Specification

- CMOS 130 nm technology
- 128 channels, Front-end&ADC in each channel
- Input Pitch 80 um, Output pitch 100-120um
- Sensor: capacitance 5–20 pF, AC coupled
- Both input signal polarities (p-in-n and n-in-p sensors)
- Input charge range ~ 30ke^-
- Noise: ENC ~ 1000e^- @10pF + 50e^-/pF
- Pulse shape: T_{peak} ~25 ns, very short tail: ~5% after 2*T_{peak}
- Crosstalk < 5%
- ADC: 6-bit resolution (5-bit/polarity), 40MS/s
- DSP functions: pedestal and common mode subtraction, zero-suppression
- Serialization&Data transmission: 320 Mbps e-links to GBT, SLVS I/O
- Slow control: I2C
- Power < 6 mW/channel
- Radiation hardness ~ 30 MRad

Front-end plus Single-to Diff

Front-end & Single-to-Diff 620um - 60um



- To facilitate testing the 8-channel Front-end ASIC will have single ended outputs
- Channels comprising conversion to differential signals will be placed only in SALT8 chip
- Channel with Front-end&Single-to-Diff completed