Summary of WP 8:

Tracking detector power distribution

Marc Weber (RAL) on behalf of participants:

AGH University of Science and Technology
Bonn University
CERN
PSI
STFC-RAL

Outline

The power distribution challenge

Possible solutions

Milestones and schedule

Status of DC-DC and serial powering activities

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Power distribution at LHC

	ATLAS pixels	CMS pixels	ATLAS strips	CMS strips
Number of modules	1744	1440	4088	15148
Total number of channels	80 M	66 M	6.2 M	10 M
Total rack power incl. optical links and cable losses	30 kW	7 kW	45 kW	67 kW
ROIC name and technology	FE-I3 0.25 µm CMOS	PSI46 0.25 µm CMOS	ABCD 0.8 µm bi-CMOS	APV25 0.25 µm CMOS
ROIC analog (digital) voltage	1.6 V (2.0 V)	1.5 V (2.5 V)	3.5 V (4 V)	1.25/2.5 V (2.5 V)
ROIC power consumption/channel	84 µW	40 µW	3.6 mW	2.9 mW
Total ROIC current	3.8 kA	1.5 kA	6 kA	15 kA
Cable length (one way)/resistance (round trip)	~110 m	~50 m	~110 m/4.5 Ω	34-62 m
Power efficiency	~20%	~42%	~50%	52%
Power distribution schemes	IP[4]	PP[3]	IP	PP
Local regulators (near/on-detector)	Yes	Yes	No	Yes

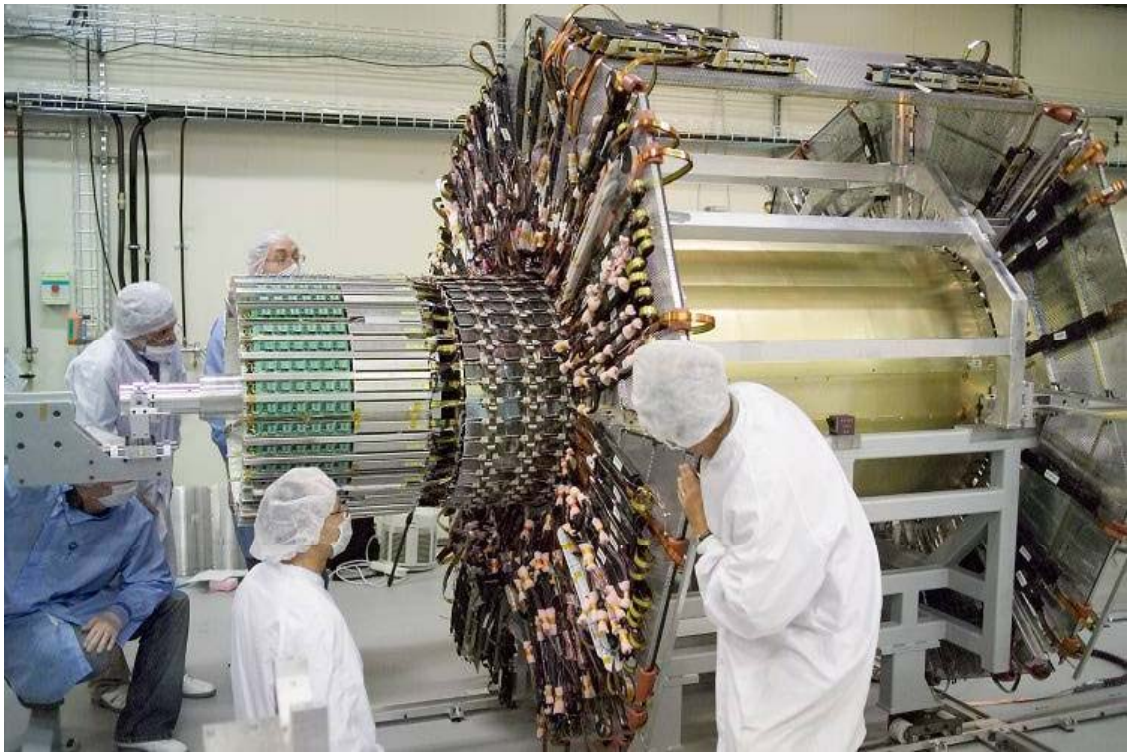
Powering at LHC proved tough and led to undesired performance penalty

Why independent powering fails at SLHC ?

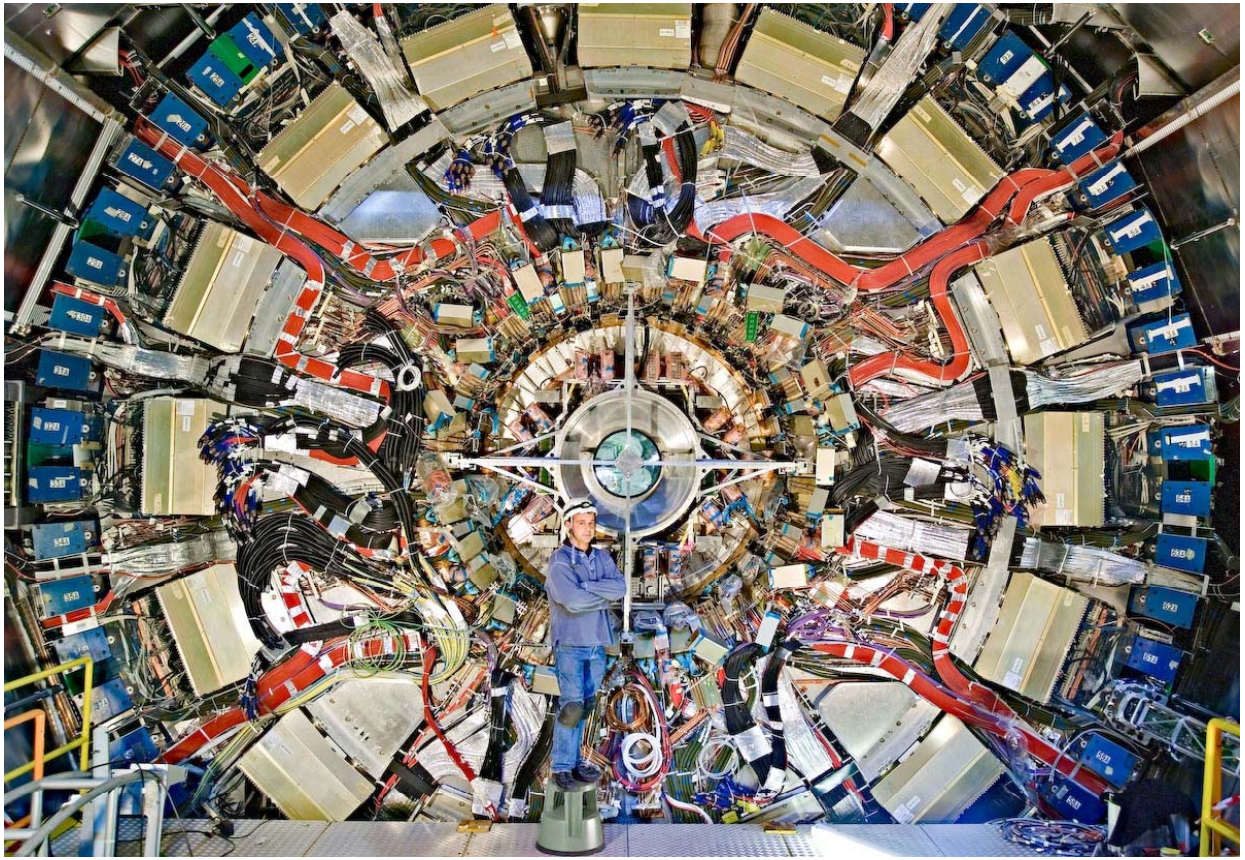
Current per electronic channel ~ constant, but many more channels

1. Don't get 5 or 10 times more cables in
2. Power efficiency is too low (50% ATLAS SCT ⇔ ~15% SLHC)
3. Cable material budget: 0.2% of R.L. per layer (barrel normal incidence) ⇔ 1% or 2% SLHC
4. Packaging constraints

Each reason by itself is probably sufficient for a No-No



Why powering R&D ?



Cannot afford cable pollution anymore and don't need to.
New systems will be much better

(cable number, material performance; packaging; power efficiency)

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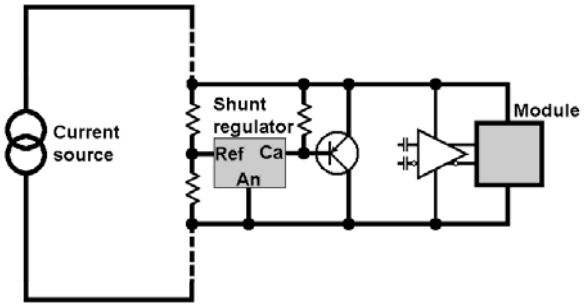
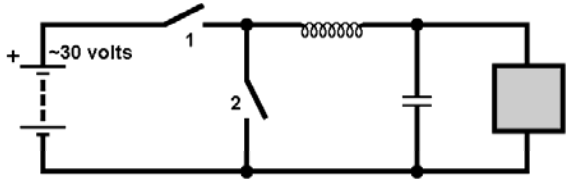
How can we fix cable pollution?

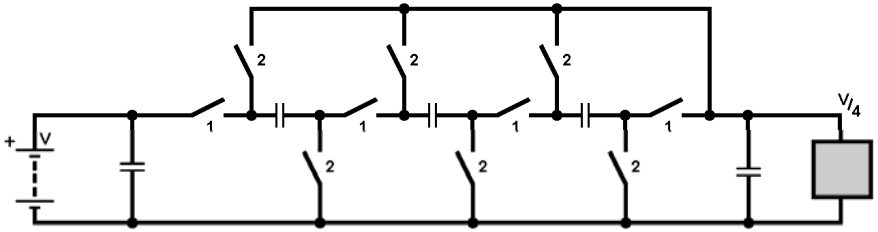
Minimize current through cables by a) recycling current (SP) or b) "high-voltage" power lines (DC-DC) ⇔ both require local PS



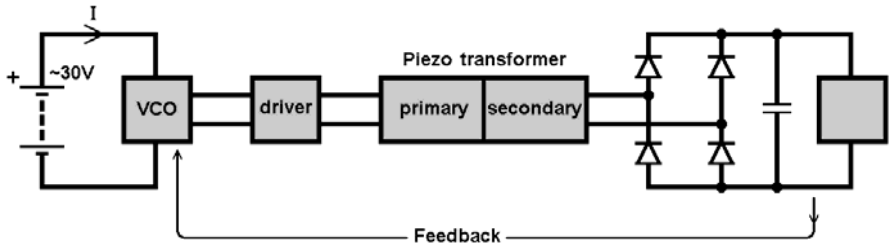
Serial powering



DC-DC buck converter



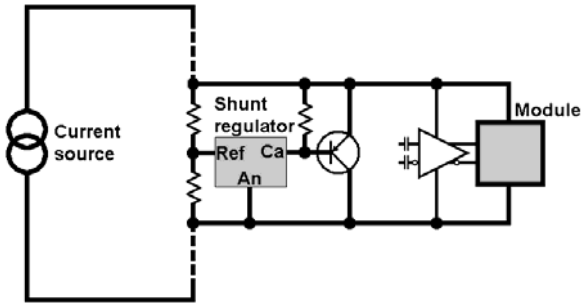
DC-DC charge pump



Piezoelectric transformer

A few comments…

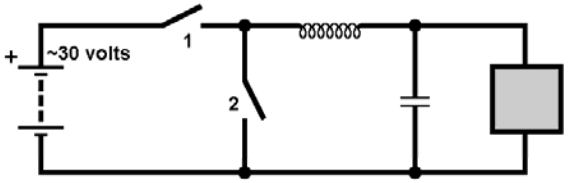
Serial powering:



Send current from module to module; local shunt regulators to define module voltage.

Unorthodox, “crazy”, but elegant. Also used for LHC magnets…

DC-DC conversion:



Conventional approach, lots of experience in industry.

But, constraints of magnetic field, low-mass and radiation tolerance are not met by commercial devices.

New approaches offer remarkable benefits: reduction of cable volume by factor 10-20; increase of power efficiency by factor 2-5…

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WP8 deliverables and milestones

SLHC-PP
Project number 212114
Date: February 1st 2008

DC-DC conversion (CERN, PSI, RAL)

Deliverables task 8.1	Description	Nature	Delivery date
8.1.1	Evaluation report on DC-DC conversion technologies	R	M12
8.1.2	Prototypes and viability report	P, R	M30
8.1.3	Integration in full-scale detector modules	D	M36

Serial powering (AGH, Bonn, RAL)

Deliverables task 8. 2	Description	Nature	Delivery date
8.2.1	Evaluation report on generic serial powering studies and specification of serial powering components	R	M12
8.2.2	Custom serial powering circuitry and evaluation of generic high-current serial powering ASIC	P,R	M24
8.2.3	Full-scale super-module with custom serial powering circuitry	D	M36

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Overview of activities in a nut shell

*DC-DC **buck converters** and **charge-pumps***
On-(read-out) chip** and dedicated **stand-alone converters

Serial powering regulators implemented in
(read-out) chip** and dedicated **stand-alone generic chip

Studies so far were largely limited to bulky commercial devices

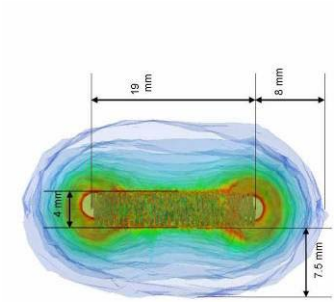
Program requires development of these devices for one:

-good electrical performance
-radiation hardness
-low mass/ small size
-high reliability
-high current capability
-magnetic field tolerance
-low EMI

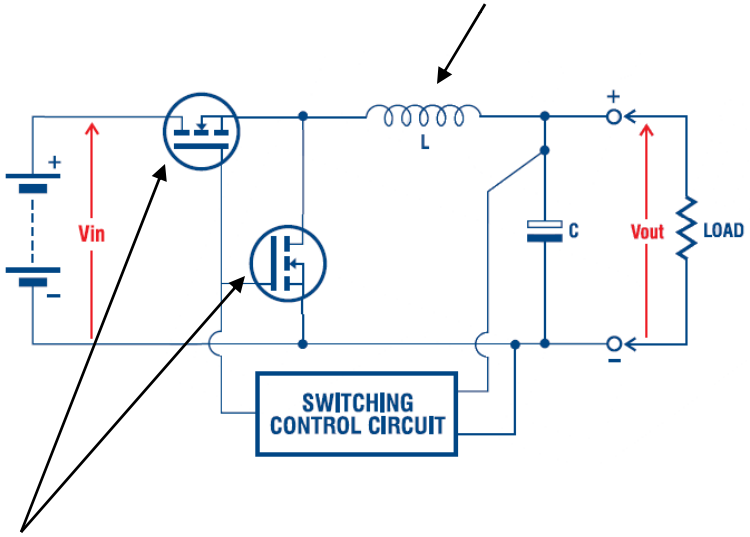
Development of these devices also requires their validation with detector modules or chains of detector modules

DC-DC step-down converters at SLHC: challenges

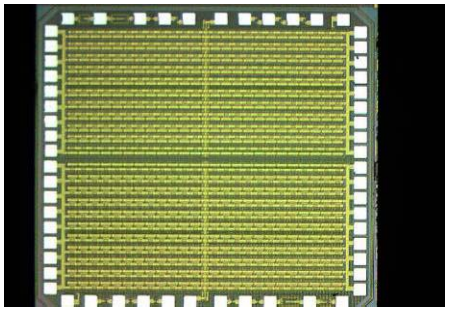
Inductor has to operate in a 4T magnetic field => cannot make use of ferromagnetic materials (coreless inductor). This implies a limit in the size of the inductance and the emission of magnetic field around the component.



Example: simplest topology for a Buck Converter



Transistors need to stand "high" voltage (12V) and to work in the SLHC radiation environment. High-voltage technologies developed for automotive applications are being surveyed, and techniques to tolerate radiation developed.



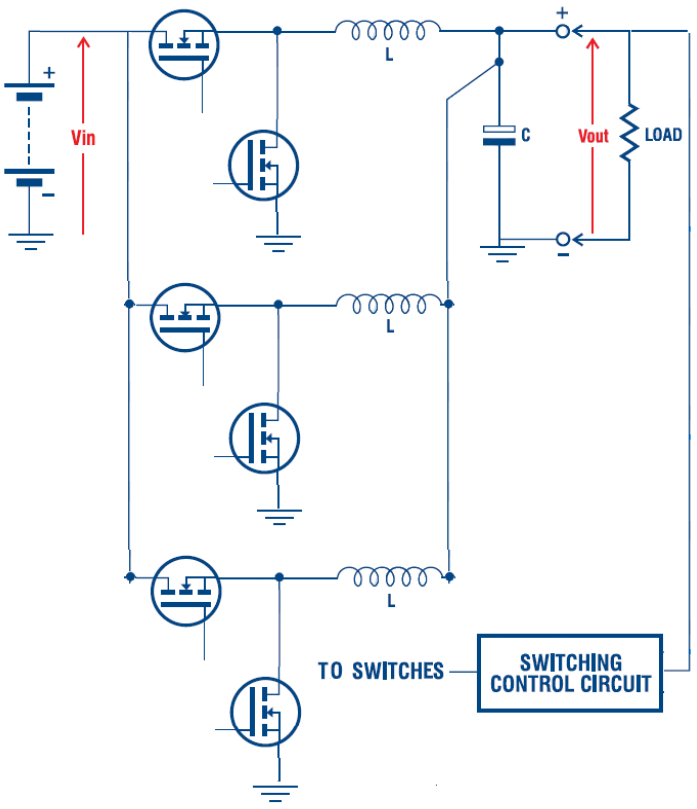
Select system architecture and DC-DC buck converter topology

System architecture must fit to SLHC tracker requirements:
Choice between e.g. 1 or 2 stage conversion

Converter topology must be optimized for the architecture:

-High efficiency (resonant topology)
-Cancellation of output voltage ripple
(interleaved topology)
-Small volume required (high frequency switching to minimize the inductor size)

Example: Buck interleaved converter

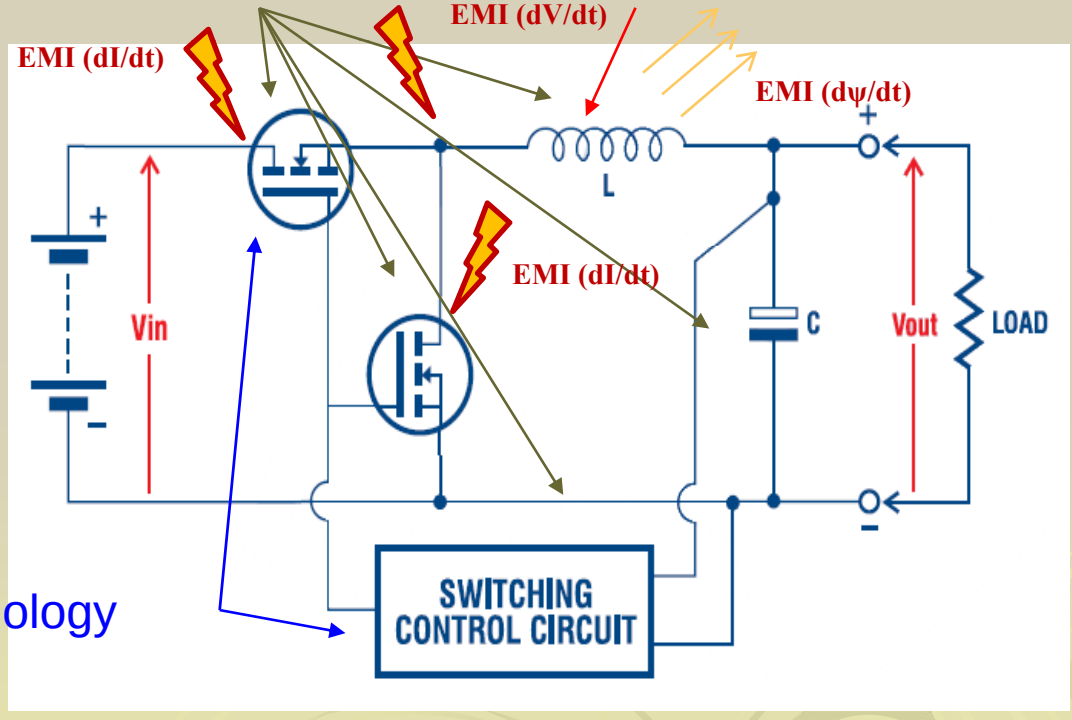


EMC issues

- Have to understand and quantify accurately the noise properties of the converters.

Power dissipation

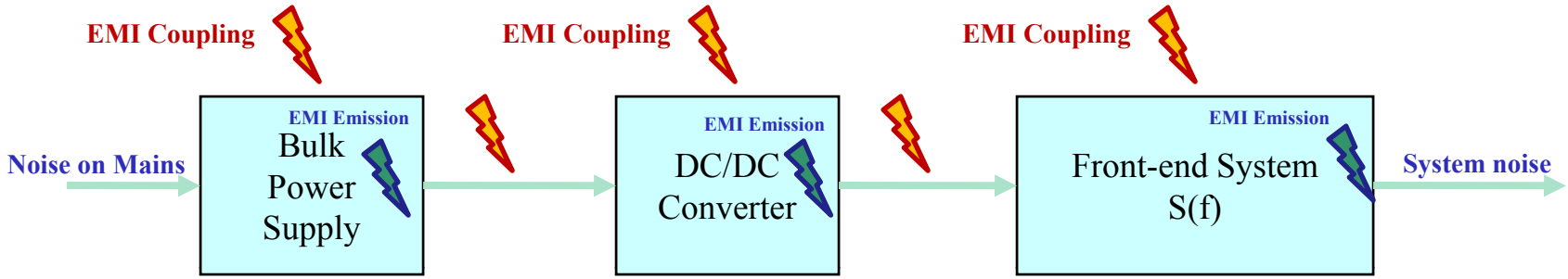
Inductor



Vin=12-24 V
Vout=1.5-3V
Iout=1-2A

Rad-hard technology

A typical SLHC system



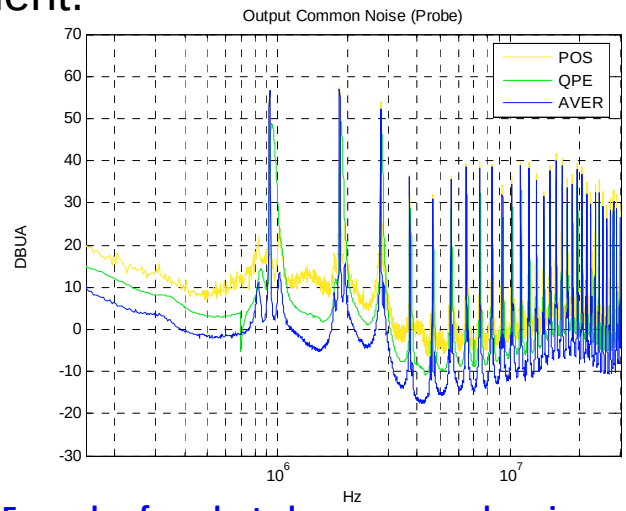
Contributors to overall system (detector) noise:

- The system itself: thermal noise, cross talk and internal couplings within the system.
- EMI couplings from other sources onto the cables and boards.
- EMI emissions of the DC-DC converter on the cables.
- EMI emissions of the bulk power system and ancillary systems.
- Conducted noise from the mains.

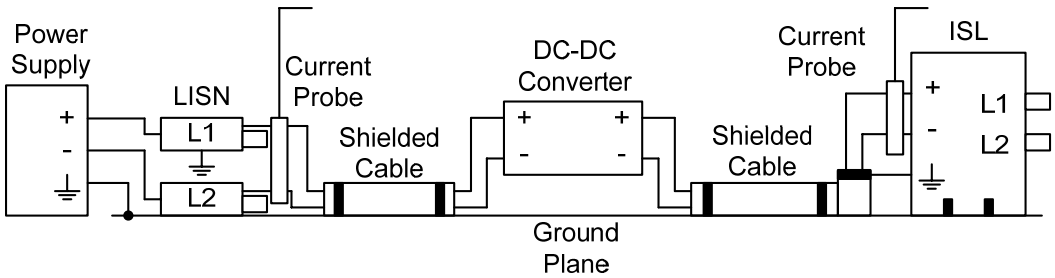
EMC reference test bench

The presence of a switching converter inside the detector system implies that Electro-Magnetic Compatibility has to be very seriously addressed at the system level since the beginning of the development.

CERN have developed a reference test-bench to characterize the conducted and emitted noise from a converter. This test bench will be used to understand and master the noise injected in the system.



Example of conducted common-mode noise over a wide frequency range



On Chip DC – DC Converters

• PSI group has designed CMS Pixel ROC with *On-Chip linear regulators* for typical power loads of 20-30mA. Was very successful in reducing material budget of LV cabling of CMS Barrel Pixel detector.

• Investigate possibilities for moderate *On-Chip DC-DC step down converter* using commercial CMOS technology with radiation hard layout technique.

• Try to benefit from incredible reduction in size and weight of ceramic capacitors over the last few years. e.g. 100 nF in 0201 size

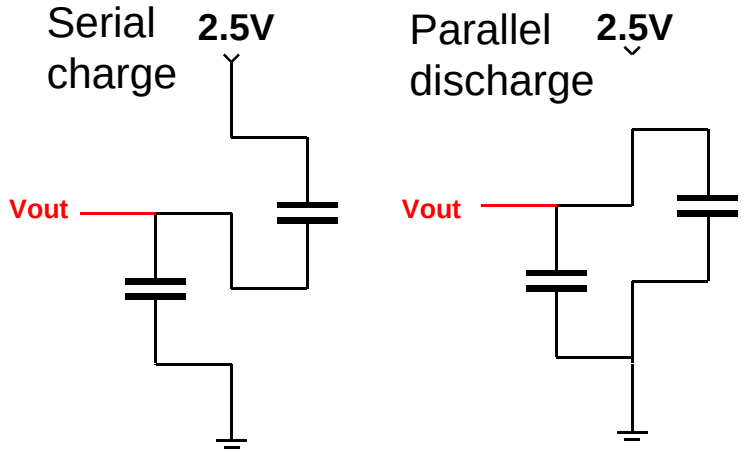
• Focus on Switched Capacitor Step-down converters for moderate voltages. e.g. 3.3 V to 1.1 volt

First exercise in 0.25um CMOS

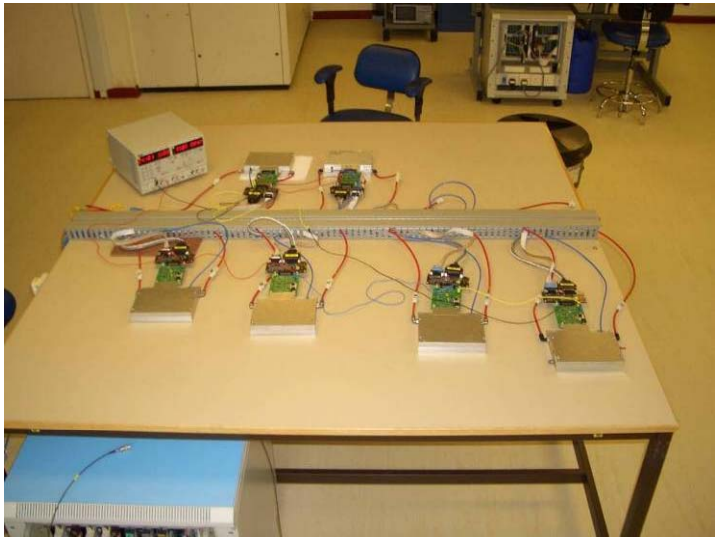
→ 2 to 1 step down at 40 MHz

→ submitted in MPW 0.25 IBM (04/2008)

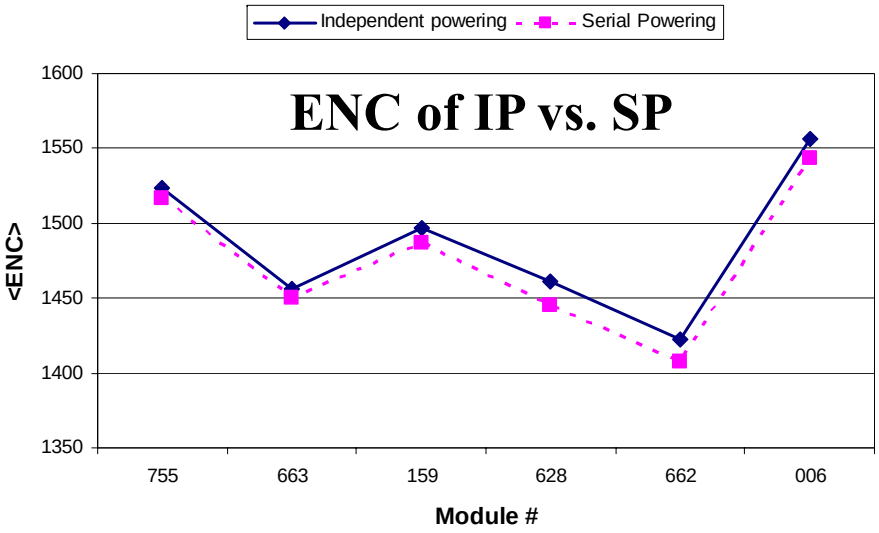
→ 83% efficiency at 25 mA load current (simu)

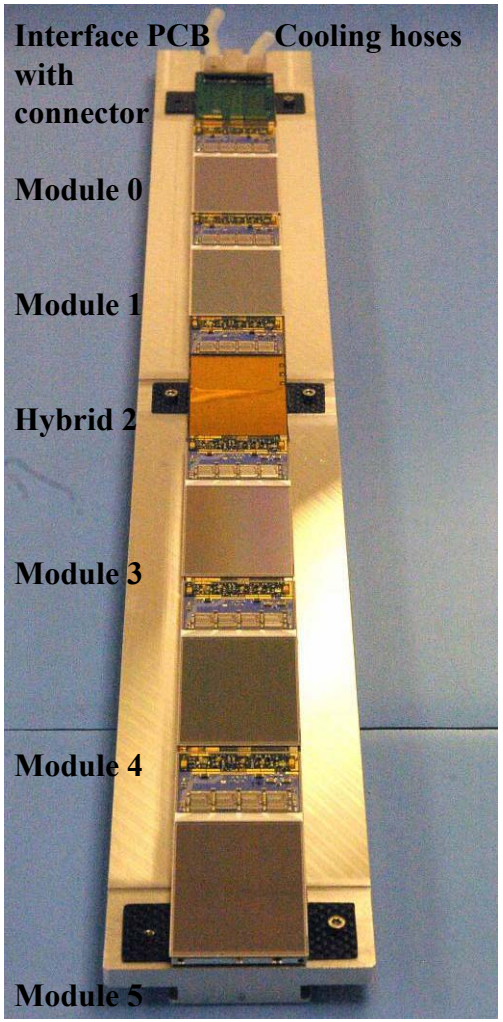


Performance of serial powering systems for strips



ATLAS SCT module tests

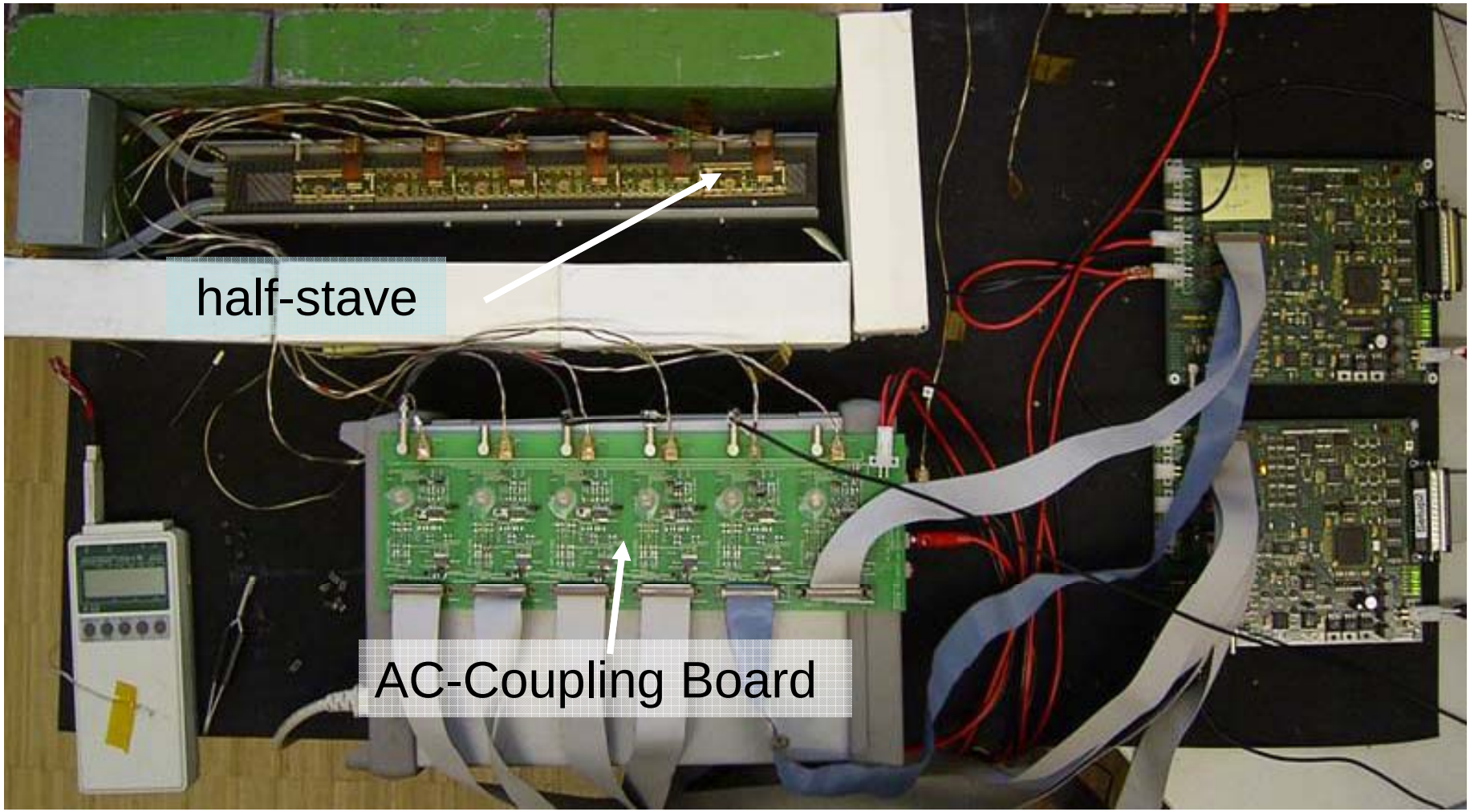




6-module serial powering stave

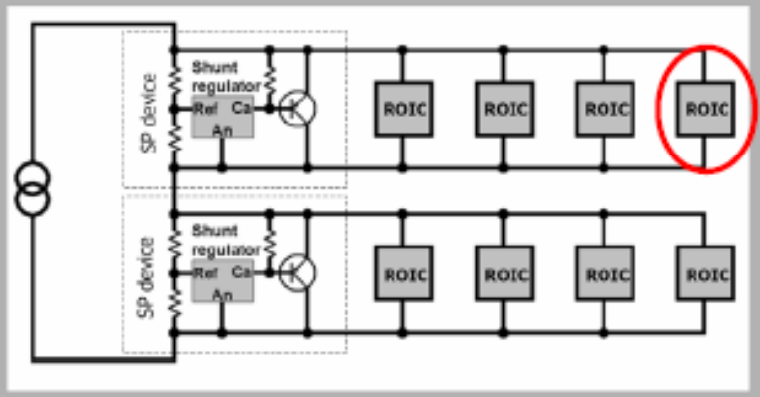
Half-stave setup

Six serially powered ATLAS pixel modules



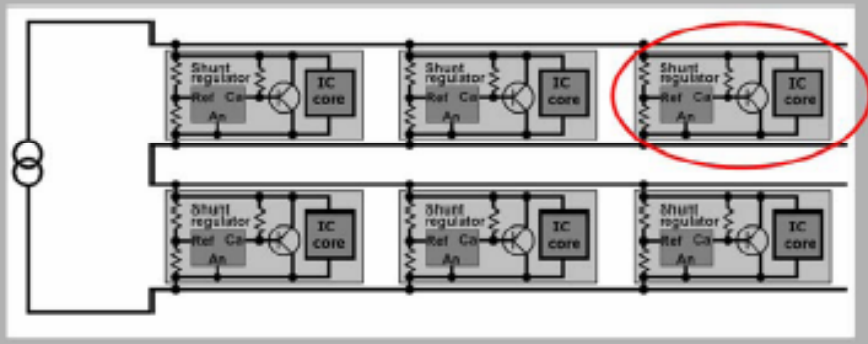
Serial Powering Schemes - Motivation

1) External shunt regulator + transistor



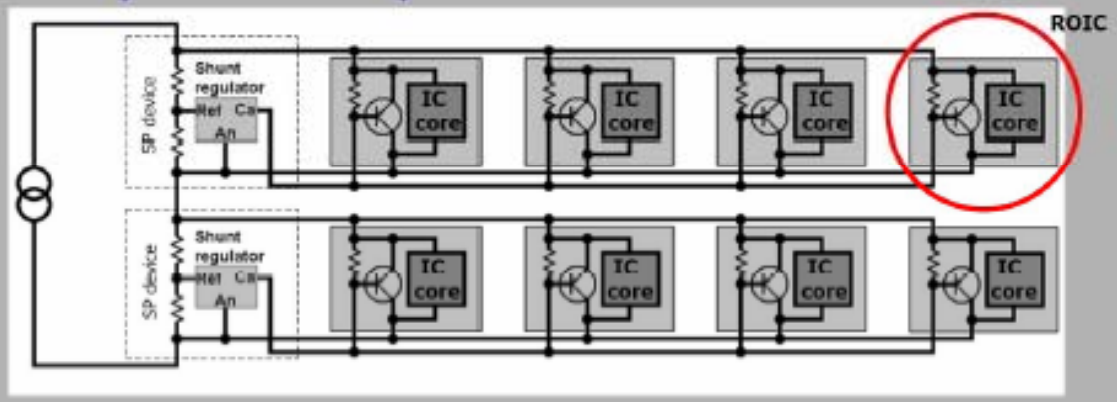
Good approach, but implies a **high current shunt**
-> limited experience in HEP-IC community
SP device enables to operate non SP-ROIC in SP mode

2) Internal shunt regulator + transistor in each ROIC



Disadvantage: many power supplies in parallel
Matching issue can cause hot spots and potentially kill chips

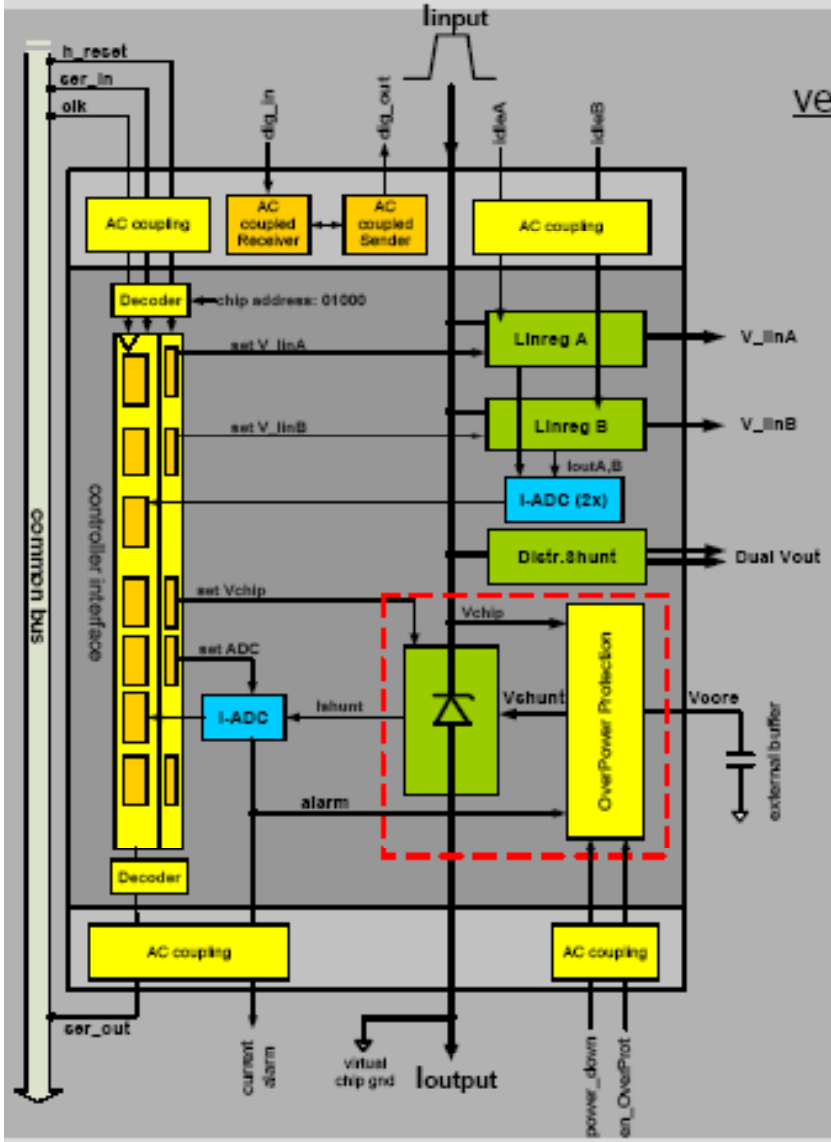
3) External SR + parallel shunt transistor in ROIC



feedback however **more challenging** and depends on implementation

- choice of architecture **not obvious**, detailed studies anticipated by RAL/LBNL (M.Weber, C.Haber)
- **SPI chip should cover scheme (1) and (3)**
- scheme (2) can be realized by any ROIC standalone

SPI - Architecture Overview



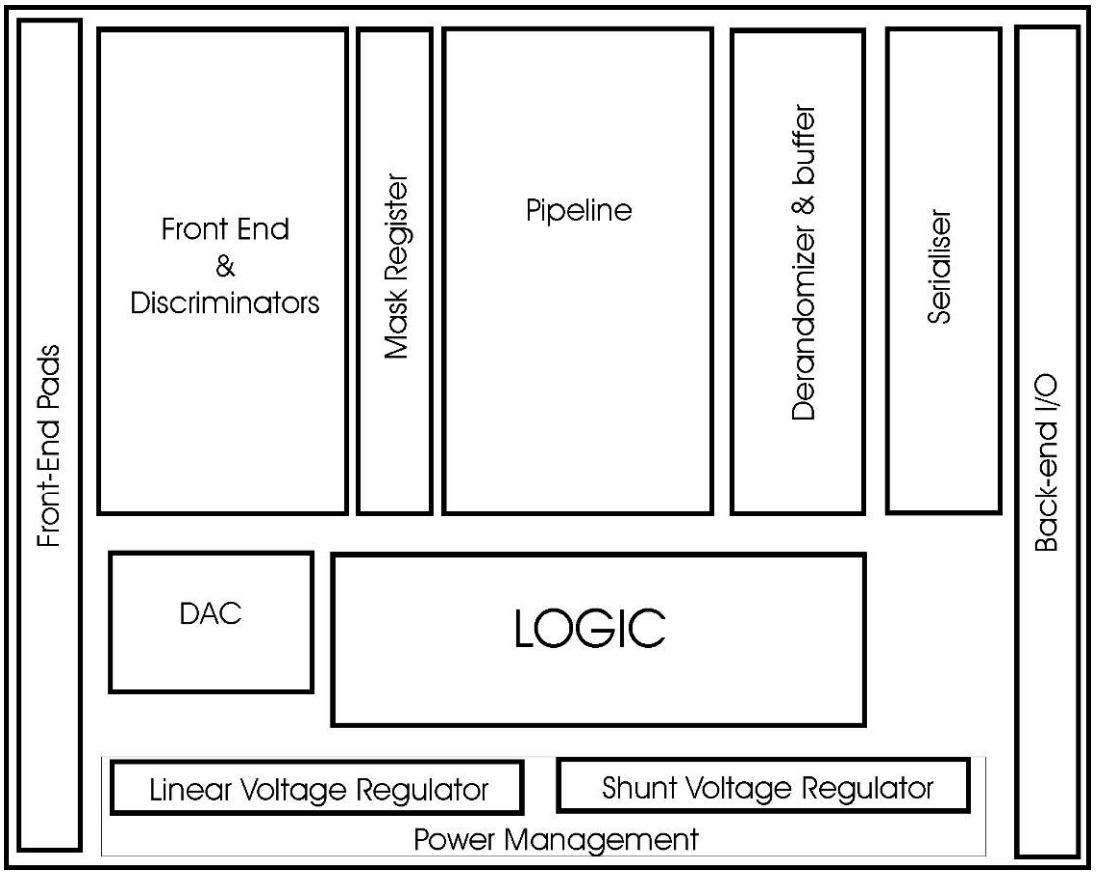
versatile SP chip - list of basic features:

- **shunt** creates Vchip (scheme1) , distr. shunt (scheme3)
- communication via **multi drop** bus (each SPI chip has 5bit address)
- spare AC coupled interfaces (**comports**)
- **ADC**s to monitor shunt and LR current
- **2x LinReg**: separate analog / digital supply to hook up some chips (1-3) for tests Not proposed as a scaleable solution for a whole module (linregs should be in the ROIC, as e.g. in the ABCn)
- on-chip **OverPower** protection (avoids detector hot spots)
- **radtol. design** techniques, TSMC 025MM process

ABC-Next

Prototype chip for Si strip readout in Upgrade Inner Tracker

- **Binary readout**
- **Front-end optimised for short strips**
- **Positive or negative input charge**
- **Readout clock up to 160 Mbits/sec**
- **250 nm CMOS (IBM) technology**
- **2.5 V digital power supply (100 mA)**
- **2.2 V analogue power supply (30 mA)**
- **Compatible with serial powering scheme**



Full shunt regulator on chip - design concept

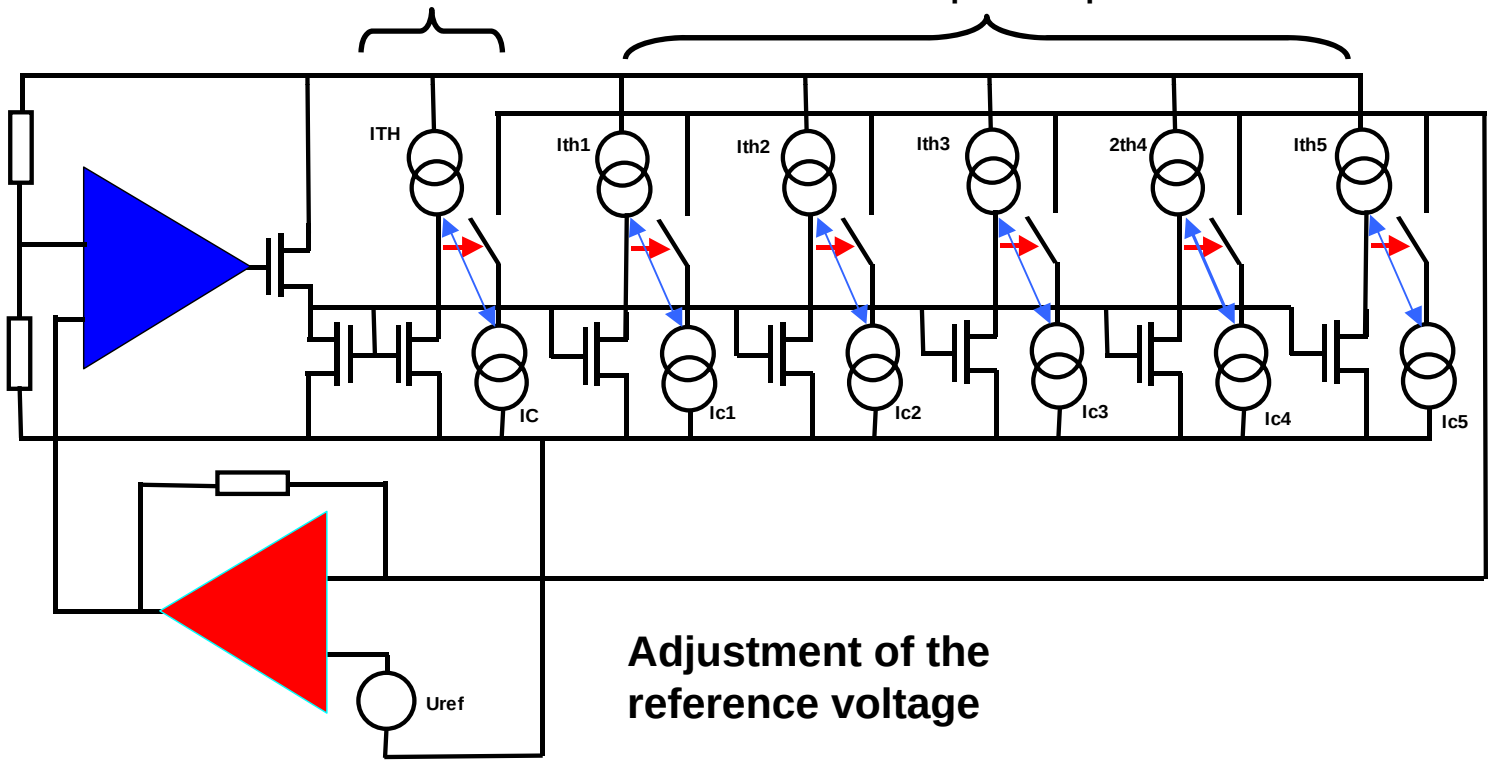
Need democratic distribution of shunt current, not winner takes it all.

Shunt current limiter

Current limit set by an internal resistor and selected by bonding

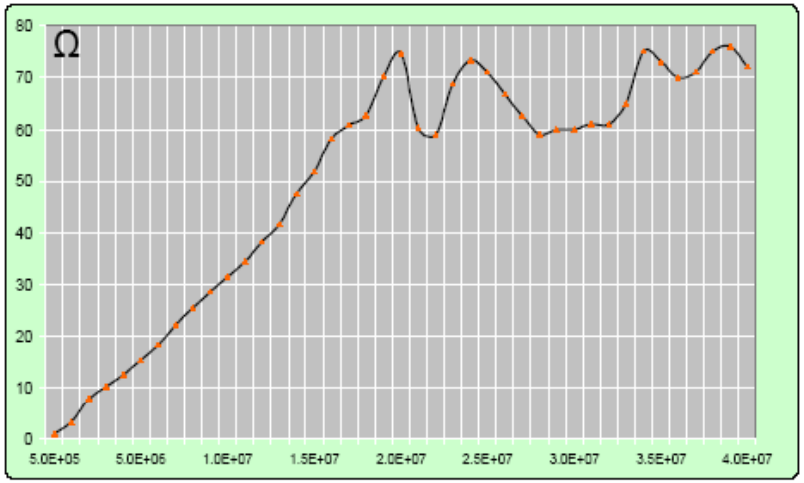
Re-adjustment and redistribution of the shunt current

Number of stages depends on the assumed spread of parameters

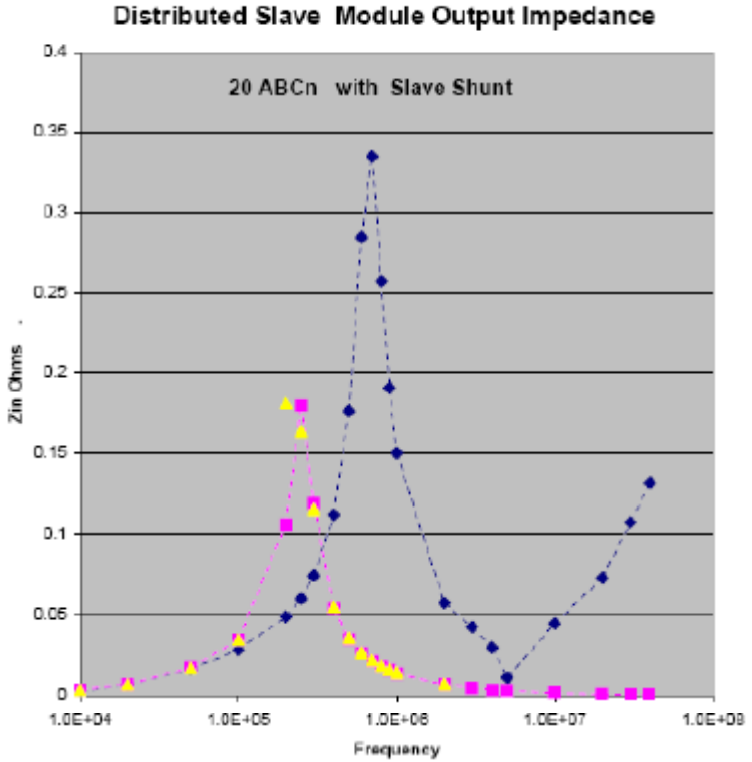


Adjustment of the reference voltage

Expected performance benefit of custom SP circuitry



Measurement (RAL): Prototype with commercial components



Simulation (Mitch Newcomer): External Shunt Regulator and Integrated Shunt Transistors

Dynamic impedance: reduced by one or two orders of magnitude!

Summary

Solving power distribution for SLHC trackers is crucial, extremely challenging and urgent.

Powering of new trackers will be very different from now, if we like it or not. If we are successful, we will need (considerably) less cables for LHC than for SLHC

Challenge has been recognized and international collaboration is growing. Despite encouraging R&D activities, we are still at the very beginning and on a steep learning curve.

Let's try to go these steps together, exploit synergies between experiments, use joint infrastructure effectively, exchange information and prototype chips…

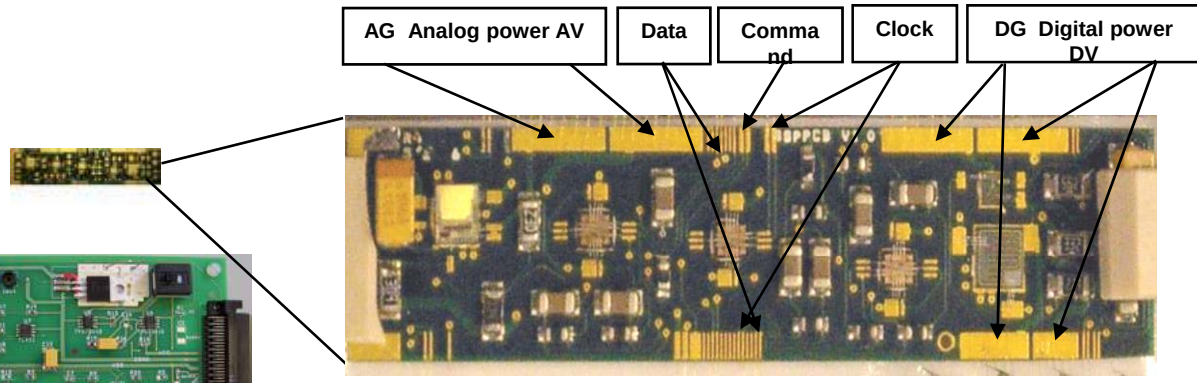
Appendix

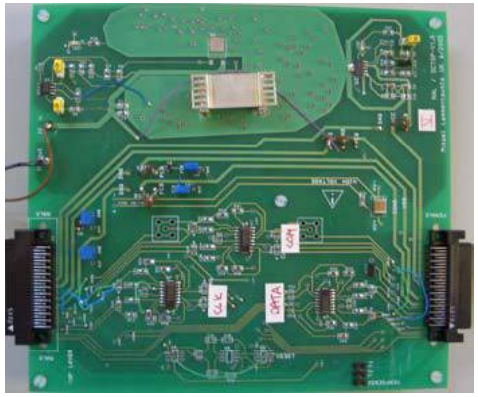
Serial powering circuitry evolution

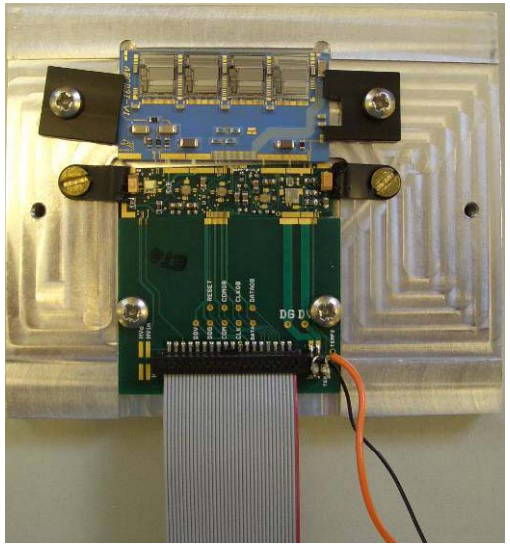
SSPPCB - 2006/7 -
38 mm x 9 mm

SPPCB - 2006 -
111 mm x 83 mm

SPPCB - 2006 -
150mm x 150mm





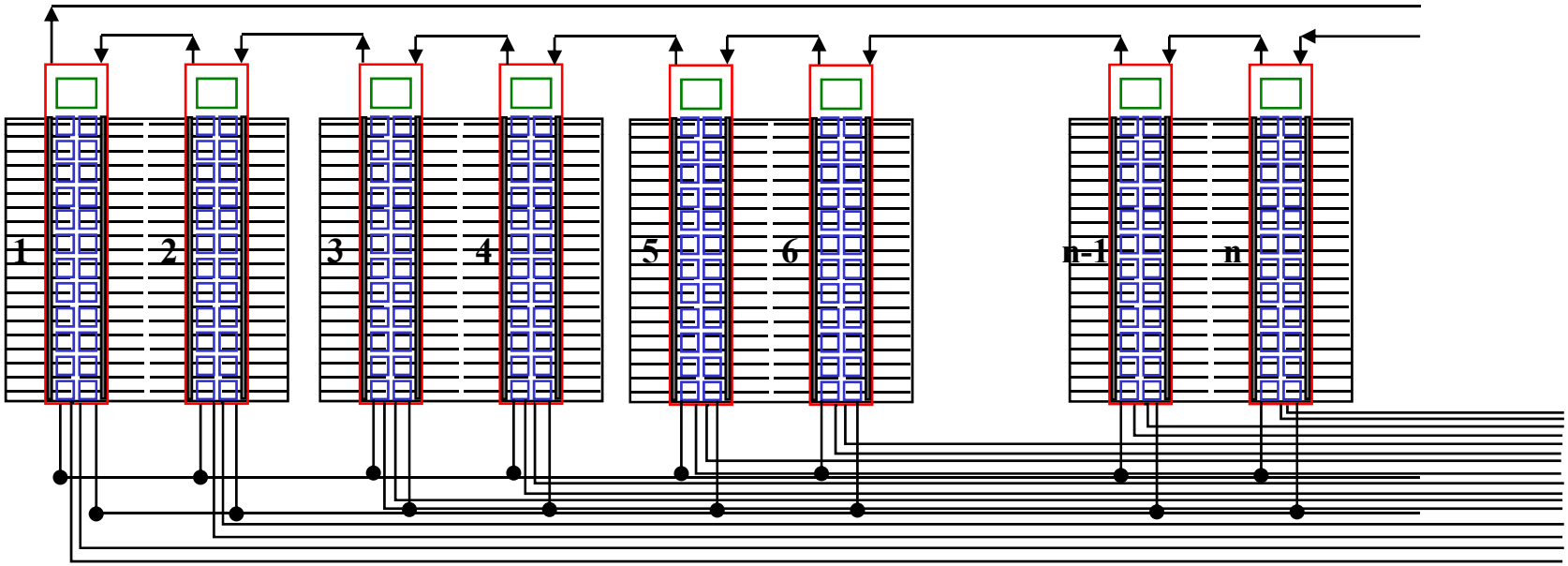


Let's work out a powering example

here V_{ROIC} = 2.5 V; I_H = 2.4 A; 20 hybrids; DC-DC gain = 20

SP: n=20; $I_H = I_{PS} = 2.4$ A; $V_{PS} = nV_{ROIC} = 50$ V

Features: saves factor ~8 in power cables/length over ATLAS SCT



DC-DC PP: n=20; g = 20; $I_{PS} = n/g\ I_H = 2.4$ A; $V_{PS} = gV_{ROIC} = 50$ V

Features: saves factor ~8 in power cables as SP, watch IR drops ⇔ $R_{cable} \sim 0.1\text{-}1\ \Omega$

DC-DC IP: n=1; g = 20; $I_{PS} = I_H/g = 0.12$ A; $V_{PS} = gV_{ROIC} = 50$ V

Features: 2x more cables than SCT ⇔ problematic for strips

Features of IP and alternative schemes

	IP	SP	DC-DC	Comment
Power efficiency	10-20%	60-80%	60-80%	Varies with I, **n** (SP); gain (DC-DC)
Local regulator inefficiency	0%	~10%	<20%	This is without linear regulator for analog
number of power cables	4 per hybrid	Reduction by factor 2n	Reduction by factor 2n	**n** = number of hybrids
Voltage control over ind. hybrids	Yes On/Off; fine-adjustment	Stand-by mode: 2.5V/1.5V -> 0.7 V; Limited fine-adjustment	Yes On/Off; limited fine-adjustment	New schemes have regulators; no fine adjustment needed
Hybrid current info	Yes	Yes (sensing current through power device)	Yes	Some power penalty for DC-DC
Hybrid voltage info	Yes (need sense wires)	Yes	Yes	Not strictly needed, since regulators
Floating hybrid power supplies	Yes	No, voltage chain	No	
Protection features	Separate set of cables for each hybrid	Local over-current protection; redundant regulators	Don't know yet	Protect against open (SP) and short (DC-DC)

Let's preserve the good features of IP ⇔ **have voltage control, current monitoring, and protection features**

Power distribution at LHC

Depending on experiment (ATLAS and CMS) and detector type (pixels or strips) we have:

- 6 – 80 million of channels
- 4 – 15 thousand detector modules
- 7-70 thousand watts of rack power for readout electronics
- 50 m to 110 m long power cables (one way)
- 20-50% power efficiency only

Constraints: limited space to feed through cables; requirement of minimum mass; need to minimize thermal losses in cables; packaging constraints on detector

SLHC trackers will have 5 to 10 times more channels than LHC ⇔

Power distribution concept must change radically

The quest for specifications…

	Required range	Desirable range
Output voltage	1.2 V – 1.8 V	1.2 – 2.8 V
Output current	> 2 A	> 4 A
Dynamic output impedance	10 Ω at < 10 MHz	0.1 Ω at < 100 kHz 0.5 Ω at < 10 MHz
Magnetic field operation	> 4 T	> 4 T
Radiation-tolerance	10^{15} n/cm^2 100 MRad	10^{16} n/cm^2 500 MRad
Size		100-250 mm^2
Inefficiency	<20%	~5%
Minimum EMI	EMI susceptibility is detector specific. Limits for radiative EMI (e.g. from inductor coils) are not yet understood. For conducted EMI, 40 dbμA of common-mode should not be exceeded in the frequency range of 100 kHz to 30 MHz.	
High reliability	System dependent. Targeted module power failure rate: < 1% per module over 5 years of operation	

Table 2: Specification for SLHC power regulators, converters or transformers. See the text for explanations.