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Wireless data transfer with mm-waves for future tracking detectors

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Wireless data transfer has revolutionized the consumer market for the last decade giving products equipped with transmitters and receiver for wireless data transfer. Wireless technology has features attractive for data transfer in future tracking detectors. The removal of wires and connectors for data links is certainly beneficial both for the material budget and the reliability of the system. Other advantages is the freedom of routing signals which today is particularly complicated when bringing the data the first 50 cm outside the tracker. With wireless links intelligence can be built into a tracker by introducing communication between tracking layers within a Region Of Interest which would allow the construction of track primitives in real time.

The wireless signal is transmitted by a passive antenna structure which is clearly a much less complex and radiation hard object than an optical transmitter. The technology used in consumer goods are however not suitable for trackers. The first limitation is the low data transfer capacity with current 5 GHz transceivers but also the relatively large feature sizes of the components.

Due to the requirement of high data rates in detectors a high bandwidth is required. The frequency band around 60 GHz turns out to be a very promising candidate. The frequency is a strong candidate for future WLAN use hence components are available on the market.
The high baseband frequency allow for data transfer of the order of several Gbit , and due to the small wave length in the mm range, only small structures are needed. The challenge is to bring the signal around or trough boundaries that are not transparent to the mm-waves like silicon detector modules or support structure. Further more low power operation and strong focusing antennas is required for massive parallelization of data transfer inside the tracker.

We will present patch antennas produced on flexible Printed Circuit Board substrate that can be used in future trackers. The antennas can be connected to transceivers for data transmission/reception or be connected by wave-guides to structures capable of bringing the signal pass boundaries.
This presentation aims to present results on simulation, modelling, fabrication and characterisation of such antennas. Studies of a 60 GHz data link for radial transmission of mm-waves through a ATLAS detector model will be shown.

1

A Parallel FPGA Implementation for Real-Time 2D Pixel Clustering for the ATLAS Fast TracKer (FTK) Processor

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The parallel 2D pixel clustering FPGA implementation used for the input system of the ATLAS Fast TracKer (FTK) processor is presented. The input system for the FTK processor will receive data from the Pixel and micro-strip detectors from inner ATLAS read out drivers (RODs) at full rate, for total of 760Gbs, as sent by the RODs after level1 triggers. Clustering serves two purposes, the first is to reduce the high rate of the received data before further processing, the second is to determine the cluster centroid to obtain the best spatial measurement. For the pixel detectors the clustering is implemented by using a 2D-clustering algorithm that takes advantage of a moving window technique to minimize the logic required for cluster identification. The cluster detection window size can be adjusted for optimizing the cluster identification process. Additionally, the implementation can be parallelized by instantiating multiple cores to identify different clusters independently thus exploiting more FPGA resources. This flexibility makes the implementation suitable for a variety of demanding image processing applications. The implementation is robust against bit errors in the input data stream and drops all data that cannot be identified. In the unlikely event of missing control words, the implementation will ensure stable data processing by inserting the missing control words in the data stream.
The 2D pixel clustering implementation is developed and tested in both single flow and parallel versions. The first parallel version with 16 parallel cluster identification engines is presented. The input data from the RODs are received through S-Links and the processing units that follow the clustering implementation also require a single data stream, therefore data parallelizing (demultiplexing) and serializing (multiplexing) modules are introduced in order to accommodate the parallelized version and restore the data stream afterwards. The results of the first hardware tests of the single flow implementation on the custom FTK input mezzanine (IM) board are presented. We report on the integration of 16 parallel engines in the same FPGA and the resulting performances. The parallel 2D-clustering implementation has sufficient processing power to meet the specification for the Pixel layers of ATLAS, for up to 80 overlapping pp collisions that correspond to the maximum LHC luminosity planned until 2022.

Summary:

The ATLAS Fast TracKer (FTK) processor is a custom electronics system that will rapidly reconstruct tracks in the inner-detector Pixel and micro-strip layers from every event that passes the level-1 trigger. The input system for the FTK processor will receive data from the ATLAS inner track detectors read out drivers (RODs) at full rate, for total of 760Gbs. This massive amount of data throughput requires a data reduction technique with as little loss of useful data as possible.

A 2D-clustering FPGA implementation was developed to achieve this for the input of the Pixel detector. The role of the 2D-clustering implementation is combined: a) reduce the high rate of the received data, b) determine the cluster centroid to obtain the best spatial measurement.
The 2D-clustering implementation consists of three modules: a) the hit decoder module, b) the grid clustering module and c) the centroid calculation module. The hit decoder trafsorms the pixel hit data in a format useful for the clustering identification. It is the module that ensures that all the data are properly identified and even in the unlikely event of missing control words, it will ensure stable data processing inserting the missing control words in the data stream. It's main operation however is to realign the pixel hits in order to be in the proper sequence for the clustering identification. The ATLAS Pixel modules [1] have 344x128 pixels which are read out by 16 front end chips (FEs). The FEs however are read out in an anticlockwise sequence which leads to half of the pixels being read out in the opposite direction than the other half. The hit decoder restores the proper pixel read out sequence by storing the reversed half of the hits in a LIFO and propagating out the hits in an increasing column number order.

The grid clustering module is the most computationally intensive part of the implementation and the one that performs the actual cluster identification. A moving window technique is used to identify the clusters. The first hit that arrives serves as a reference hit and is placed in the middle row and leftmost column of the window. The hits are read from the input until a hit with a column number outside the detection window arrives. The hits whose coordinates are not part of the detection window are stored in a circular buffer. To identify the cluster the reference hit then serves as a "seed"which propagates a "select"signal to change the state of all hits neighboring it. The "selected"hits are part of a cluster and are read out one by one and the hits which are in the detection window but don't belong to the cluster are stored in the circular buffer. In the next run the leftmost hit stored in the circular buffer is chosen as a reference hit, the detection window is filled first by hits from the circular buffer and then the input and the process is repeated until the pixel module is all read out and the circular buffer is empty. The detection window size is generic and can be adapted for different applications. For the ATLAS Pixel module a size of 8 columns x 21 rows was chosen.

The centroid calculation module is where each cluster is replaced by a set of coordinates, the centroid coordinates then corrected by a variable calculated by taking into account the absolute pixel position as well as the charge imbalance (using the measured Time-Over- Threshold for each pixel hit).

One fundamental characteristic of the 2D-clustering implementation is that different clustering engines can work independently and in parallel to identify different clusters, therefore increasing performance while exploiting more FPGA resources. However, the pixel data are received through S-Links [2] and the processing units that follow the clustering implementation also require a single data stream, therefore data parallelizing (demultiplexing) and serializing (multiplexing) modules are introduced in order to accommodate the parallelized version and restore the data stream afterwards. Each engine processes the data from one Pixel module. A parallel distributor module was developed that splits the data stream into the different engines by choosing the less busy one to propagate the next module into. The LVL1ids of the processed events are stored in a FIFO so that the same sequence of events can be recovered when the data stream is serialized again. A data merger module is used to serialize the data output in the same data sequence.

The single flow 2D-clustering will be tested on the custom FTK input mezzanine (IM) board using an 80MHz clock. Post place and route simulations with 80 overlapping pp collisions files have demonstrated a worst case estimate of 10 cycles / data word processing time. The x16 implementation has achieved a 65MHz maximum clock frequency and occupies 40% of a Spartan 6 lx150T FPGA device. Pixel data is received at a maximum 40MHz word rate. By using a x16 parallelization the 2D-clustering implementation will significantly exceed the processing power required for the Pixel detector. The 2D-clustering operation has been overlapping pp collisions that correspond to the maximum LHC luminosity planned until 2022.

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2

Event building and reconstruction at 30 MHz using a CPU farm

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The upgrade of the LHCb detector relies on the ability to perform a full detector readout and event building at the LHC inelastic collision rate of 30 MHz, corresponding to a data rate of approximately 2.4 TB/s. We describe a novel uniform event builder architecture, based around a farm of commercial PCs linked by a bidirectional network, which fulfils this requirement in a cost effective way. We furthermore demonstrate that the event building itself can be performed while taking up only a small fraction of the computing power of this farm, while the rest is available to perform the earliest stages of event reconstruction
and classification. We discuss the kinds of reconstructions which can be deployed in this farm and their uses in classifying the LHCb upgrade events with reference to several key physics benchmarks of the LHCb upgrade.

3

The upgrade of the LHCb trigger system

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The current LHCb trigger system consists of a hardware level, which reduces the LHC inelastic collision rate of 30 MHz to 1 MHz, at which the entire detector is read out. In a second level, implemented in a farm of 20k parallel-processing CPUs, the event rate is reduced to about 5 kHz. The major bottleneck in LHCb's trigger efficiencies for hadronic heavy flavour decays is the hardware trigger. The LHCb experiment plans a major upgrade of the detector and DAQ system in the LHC shutdown of 2018. In this upgrade, a purely software based trigger system is being developed, which will have to process the full 30 MHz of inelastic collisions delivered by the LHC. We demonstrate that the planned architecture will be able to meet this challenge, particularly in the context of running stability and long term reproducibility of the trigger decisions. We discuss the use of disk space in the trigger farm to buffer events while performing run-by-run detector calibrations, and the way this real time calibration and subsequent full event reconstruction will allow LHCb to deploy offline quality multivariate selections from the earliest stages of the trigger system. We discuss the cost-effectiveness of such a software-based approach with respect to alternatives relying on custom electronics. We discuss the particular importance of multivariate selections in the context of a signal-dominated production environment, and report the expected efficiencies and signal yields per unit luminosity in several key physics benchmarks the LHCb upgrade.

4

Fiber-optic links based on silicon photonics for high-speed read-out of trackers

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We propose to use silicon photonics technology to build radiation-hard fiber-optic links to readout tracking detectors at 40 MHz. The CMOS integrated silicon photonics was developed by Luxtera and commercialized by Molex. The commercial off-the-shelf fiber-optic links feature moderate radiation tolerance insufficient for trackers. A transceiver contains four RX and four TX channels operating at 10 Gbps each. The next generation will likely operate at 25 Gbps per channel. The approach uses a standard CMOS process and single-mode fibers, providing low power consumption and good scalability and reliability.

5

Towards a Level-1 tracking trigger for the ATLAS experiment at the High Luminosity LHC

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The future plans for the LHC accelerator allow, through a schedule of phased upgrades, an increase in the average instantaneous luminosity by a factor 5 with respect to the original design luminosity. The ATLAS experiment at the LHC will be able to maximise the physics potential from this higher luminosity only if the detector, trigger and DAQ infrastructure are adapted to handle the sustained increase in particle production rates.

In this paper the changes expected to be required to the ATLAS detectors and trigger system to fulfill the demands of such a high luminosity scenario are described. The increased number of interactions per bunch crossing will result in higher occupancy in the detectors and increased rates at each level of the trigger system. The trigger selection will improve the selectivity, partly from increased granularity for the sub detectors and the consequent higher resolutions achievable. One of the largest challenges will be the provision of tracking information at the first trigger level, which should allow a large increase in the rejection power at this stage of the selection and yet still allow the full physics potential of the experiment to be fulfilled. In particular, reconstructing objects at the electroweak scale will still require that the thresholds on the transverse momenta of particles be kept as low as possible. Tracking provides essential information of this kind for individual particles so it is desirable to attempt to reconstruct tracks as early in the trigger chain as possible.

The ability to apply fast processing that can take account of the properties of the tracks that are being reconstructed will enhance the rejection, while retaining high efficiency for events with desired signatures, such as high momentum leptons or multiple jets. Studies to understand the feasibility of such a system have begun, and proceed in two directions: a fast readout for high granularity silicon detectors, and a fast pattern recognition algorithm to be applied just after the Front-End readout for specific sub detectors. Both existing, and novel technologies can offer solutions. The aim of these studies is to determine the parameter space to which this system must be adapted. The status of ongoing tests on specific hardware components crucial for this system, both to increase the ATLAS physics potential and fully satisfy the trigger requirements at very high luminosities are discussed.

Summary:

A luminosity upgrade for the LHC[1] is foreseen for 2024 in order to allow increased phase space coverage both for searches and precision Higgs physics. For this high luminosity LHC (HL-LHC), instantaneous luminosities around $7\times10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ are expected, delivering around $300\mathrm{fb}^{-1}$ per year. At these high luminosities, mean numbers of separate pp interactions in the range of 160-200 are expected for every bunch crossing. Event rates for single lepton candidates passing the Level 1 (L1) triggers in the ATLAS[2][3] detector using the current trigger strategy are expected to be of the order of 200-400 kHz for each lepton species individually, with jet and other physics signatures providing some significant rate in addition. The current ATLAS trigger strategy uses only coarse granularity Calorimeter and Muon Spectrometer information at Level 1, with full granularity data including tracking information from the Inner Detector used in the

High Level Trigger (HLT). Processing this rate of output from L1 is not possible in the HLT.

For the HL-LHC upgrade ATLAS will be equipped with an all-new Silicon Inner Tracker (ITK). Studies have been performed to evaluate the performance benefits of reconstructing tracks in the ITK at Level 1, and matching them to either calorimeter clusters or muon candidates. To enable the processing of the high rates from the HL-LHC, ATLAS has therefore proposed a Level 1 Track Trigger to work within a scenario where the current Level 1 processing is split into consecutive harware stages, denoted Level 0 (L0) and Level 1. Limitations from the front-end pipelines for no-longer accessible sub-detector components mean that any upgraded ATLAS trigger system will have only 20μs from the time of the bunch crossing until the L1 decision must arrive back at the detector front ends. The maximum L1 output rate that can be supported by these sub-detectors is 200 kHz. To operate within these constraints, in the split L0-L1 scenario the detector front end electronics for some sub-detectors will make use of a double buffer. In the L0 system the Calorimeter and Muon systems will process events using course granularity data to identify regions of interest (RoI) as in the current Level 1 trigger. The L0 decision will be distributed back to the detector front ends at the rate of 500 kHz to arrive 6μs after each bunch crossing. On a L0 accept the data from the primary buffers will be read into a secondary buffer where it will remain until the L1 decision arrives. Within the remaining 14μs both the transfer of the ITK data to the L1 track processor and the track reconstruction must be performed.

The readout latency is critical: if the data can be read out within 6μs then 8μs will remain for the tracking algorithm. Upon receipt of a Regional Readout Request (R3), identifying a particular RoI, each detector element within the RoI will read out a sub-sample of the data from the secondary buffer to the L1 processing systems. For each L0 accept it is expected that the average number, and size of all the RoIs in each event will comprise only about 10% of the total data volume within the event. In this way, only 10% of the detector need be read out, such that the total event rate to be read out to the L1 system will be 50kHz only 10% of the 500 kHz L0 accept rate. The readout of the ITK strip tracker is arranged by module: each module reading out the strips using several daisy-chained identical front end ASIC (ABC130), which use 130 nm CMOS technology. Studies using a discrete event simulation of the complete readout chain from the distribution of the R3 and L1 accept requests, to readout through the Hybrid Chip Controller (HCC) to the off-detector electronics have been performed using simulated ITK hit occupancies expected from 200 pileup interactions per bunch crossing. These studies suggest that the R3-95% latency – the time taken to read out all packets from a hybrid for 95% of all R3 – for all modules in the inner most barrel layer of the ITK strip tracker, is safely within 6μs for the standard 200 kHz L1A rate. To help in this, the readout chip can contains logic to prioritise the read out of R3 data over that of data from a L1 accept. An additional FIFO can be added to buffer the input on the HCC from each daisy chain. The latencies both with and without R3 data prioritisation and different FIFO depths on the HCC were measured for different regions of the tracker detector.

The tracking algorithm must complete execution in the remaining 8μs in this scenario. This is feasible with current technologies which make use of CAM (Content-addressable memory) to perform fast pattern-matching in the first stage of the selection, and fast fitting procedures in a

second step, after the combinatorics have been reduced. The pattern-matching algorithm performance will move in a large parameter space, based on the number of coincidence layers of silicon, the system segmentation and the pattern resolution, with constraints provided by both hardware limitations, such as the input/output bandwidths and size of the pre-registered pattern content per processor, and physics requirements, such as the minimum track momentum to be selected. Studies are ongoing using detailed simulations of the ITK geometry and detector response in high pile-up environments in order to understand the connections between these parameters.

In this paper the results of studies that will drive the design of the L1 track system of ATLAS, together with the results of intermediate stage tests on prototype hardware that will extend the potential of this system are discussed.

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6

The Serial Link Processor for the Fast TracKer (FTK) processor at ATLAS

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The Associative Memory (AM) system of the FTK processor has been designed to perform pattern matching using the hit information of the ATLAS silicon tracker. The AM is the heart of the FTK and it finds track candidates at low resolution that are seeds for a full resolution track fitting. To

solve the very challenging data traffic problems inside the FTK, multiple designs and tests have been performed. The currently proposed solution is named the "Serial Link Processor"and is based on an extremely powerful network of 2 Gbit/s serial links.
This paper reports on the design of the Serial Link Processor consisting of the AM chip, an ASIC designed and optimized to perform pattern matching, and two types of boards, the Local Associative Memory Board (LAMB), a mezzanine where the AM chips are mounted, and the Associative Memory Board (AMB), a 9U VME board which holds and exercises four LAMBs. Special relevance will be given to the AMchip design that includes two custom cells optimized for low consumption.
We report also on the performance of a first prototype based on the use of a min@sic AM chip, a small but complete version of the final AM chip, built to test the new and fully serialized I/O. A dedicated LAMB prototype, named miniLAMB, with reduced functionalities, has been produced to test the mini@sic. The serialization of the AM chip I/O significantly simplified the LAMB design. We report on the characterization of the min@sic chip, the tests and performance of the integrated system mini@sic, miniLAMB and AMB.

Summary:

The Associative Memory \1 (AM) system of the FTK processor \2 has been designed to perform pattern matching using the hit information of the ATLAS silicon tracker. The AM is the heart of the FTK. It finds track candidates at low resolution that are seeds for a full resolution track fitting. An array of 128 AM boards will provide 1 billion AM patterns that will perform pattern recognition for the FTK system. In order to achieve the pattern density of 8M patterns / AM board and stay within the power consumption limits significant R&D has been performed for both the AM chip and AM board. The recent developments for AM chip, LAMB and AM board are reported.

This contribution will focus on the design of the new Associative Memory chip (AMchip05) that is the last planned prototype for the Fast Tracker (FTK) system. The AMchip05 is a 12 mm2 ASIC using 65nm technology with I/O based on 11 serial links at 2 Gbit/s. We will report on the design choices and simulation results of the AMchip05. The design of the AMchip05 is based on the characterization of the previous mini@sic AM chip (see fig. 1) that uses for the first time the 2Gbps serial links for I/O. With respect to the mini@sic the AMchip05 further improves the power consumption per pattern and includes all features required for use in FTK and some improvements among which the possibility to have separate speeds for input and output channels in order to allow better performance for the same power consumption.

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Fig. 1: test setup for the mini@sic AM chip

After test and characterization, four of the first mini@sic AM chips have been installed on the mini-LAMB (see fig. 2) in order to test them in conditions close to those of their final use in FTK. We report the results of the mini-LAMB tests and of the new AMBSLP (see fig. 3).

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Fig. 2: test setup for the mini-LAMB

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Fig. 3: new AM board (AMBSLP) prototype

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7

Analysis of data compresssion efficiency in silicon detector read-out

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On-detector intelligence permits a reduction of the information to be sent off detector. In the best case this permits the scrutiny of every event before any trigger decision. This work investigates what is the minimum number of bits needed to send a given amount of information off detector. This permits a systematic analysis of the readout efficiency relative to this
theoretical minimum number of bits. The greater the readout efficiency the lower the burden on the processing needed to reduce information. Different level efficiencies are defined to include context information and engineering properties needed for reliable transmission, such as DC-balance. A commonly used encoding method is analyzed as an example and found to have an efficiency only of order 50\%. A new encoding method called Pattern Overlay Compression is introduced to illustrate how the systematic analysis can guide the construction of more efficient readout methods. Pattern Overlay Compression significantly outperforms the above example in the occupancy range relevant of strip detector readout. These results are documented in a paper submitted to JIST that can be found here: http://arxiv.org/abs/1309.1869. The analysis of pixel detector readout introduces added complications. On-going work on pixel readout will be presented along with results on strip detector readout.

Summary:

see http://arxiv.org/abs/1309.1869

8

Level-1 track triggering at CMS for the HL-LHC

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The High Luminosity LHC (HL-LHC) is expected to deliver luminosities of 5x10ˆ34 cmˆ2/s, with an average of about 140 overlapping proton-proton collisions per bunch crossing. These extreme pileup conditions place stringent requirements on the trigger system to be able to cope with the resulting event rates. A key component of the CMS upgrade for HL-LHC is a track trigger system which would identify tracks with transverse momentum above 2 GeV already at the first-level trigger. This talk presents a proposal for implementing the L1 tracking using tracklets for seeding. The expected performance and the use of L1 tracks for triggering is discussed.

9

Hardware Implementation of FPGA based Level-1 Tracking

Author: Jorge Chaves[1]

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This presentation describes a new approach for track reconstruction to be used in the Level 1 trigger. This is intended for the upgraded CMS all-silicon tracker, which is to be installed for the High Luminosity era of the LHC (HL-LHC). The track finding is seeded with pairs of hits from adjacent layers in the tracker that are combined to form 'tracklets'. The tracklets are projected to other layers (both outside-in and inside-out), where hits consistent with the trajectory of a high-pT track are added. The pT threshold for the tracks to be considered is 2 GeV. A linearized track fit provides the final 3-D track parameters. The strict timing requirements of the L1-trigger at CMS require that the fit is done within 5 us, which is within the estimates for the algorithm. The algorithm is such that allows for an integer implementation to be used on an FPGA. Currently we are working on a demonstrator hardware implementation using a Xilinx Virtex 6 FPGA.

10

L1 track triggering with associative memories for the CMS HL-LHC tracker

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One of the proposed solutions currently under study in CMS to reconstruct tracks at the first level trigger (L1) for the HL-LHC is based on the usage of Associative Memory (AM) chips. The tracker information is first reduced to suppress low pT tracks and sent to boards equipped with AM chips. Each AM compares the tracker information with pre-calculated expectations (pattern matching) in a very short time (order or a μs), therefore providing a solution to the challenging computational problem of pattern recognition in a very busy environment. Associated to fast track fit methods, like the Hough transform, the AM approach should be able to fulfill the very demanding requirements of L1 tracking. The proposed architecture for the AM-based L1 track reconstruction system will be presented, together with the latest results obtained using a complete software emulation of this system.

11

System Architecture and Vertical Slice Demonstration for CMS L1 Silicon-based Tracking Trigger

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The development of a silicon-based L1 tracking trigger system is of utmost importance for CMS for the HL-LHC, in order to maintain physics acceptances for the important trigger objects (such as leptons). A silicon-based L1 tracking trigger has never been realized at this scale and thus it is imperative that its feasibility be demonstrated before the design of the Phase-II Tracker can be finalized. The higher occupancies anticipated at the HL-LHC and the low latencies required at L1 present us with a formidable set of challenges that we need to attack with a well organized R&D campaign. For the off-detector part of tracking trigger, the main challenges are the complex data dispatching

and the pattern recognition and track fitting. Data dispatching is where the stubs from many thousands silicon modules must be organized and delivered to the appropriate eta-phi trigger towers. Due to the finite size of the beam's luminous region in z and the finite curvature of charged particles in the magnetic field, some stubs must be duplicated and sent to multiple towers in an intelligent way. Since all this must be done within a very short time (of the order of a micro-second), communication between processing elements in different towers requires very high bandwidth and very low latency. In addition, extremely fast and effective pattern recognition and track fitting is also required. Extensive R&D and experimentation of innovative ideas is needed in this area. Therefore, it is desirable that the design of the overall architecture can address the need for efficient dispatching of the data for time and regional multiplexing and the capability of providing a common flexible framework to test different possible solutions for track finding and fitting. For this purpose, a custom full mesh enabled ATCA board called Pulsar II has been designed at Fermilab with the goal of creating a scalable architecture abundant in flexible, non-blocking, high bandwidth board-to-board communication channels. In addition, pattern recognition mezzanine cards can be designed for Pulsar II, and this will be the pattern recognition engine and can host FPGA with the new associative memory chips being developed. In this talk, we will present a status report of the off-detector L1 silicon-based tracking trigger R&D program, from system level architecture considerations to the concept of a Vertical Slice Demonstration, with board and chip level prototype results designed for such a demonstration. This R&D is being pursued in collaboration with a few CMS institutions, and some of the R&D activities will be presented in other talks at this workshop.

12

60 GHz Wireless Data Transfer for Tracker Readout Systems - First Studies and Results

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To allow highly granular trackers to contribute to first level trigger decisions or event filtering a fast readout system with very high bandwidth is required. Space, power and material constraints however pose severe limitations on the maximum available bandwidth of electrical or optical data transfers.

A new approach for the implementation of a fast readout system is the application of a wireless data transfer at a carrier frequency of 60 GHz. The available bandwidth of several GHz allows for data rates of multiple Gbps per link. Transceiver chips can be produced with a small form factor and a high integration level. A prototype transceiver currently under development at the University of Heidelberg is presented in this talk. Furthermore, results of bit error rate measurements with a commercially available wireless 60 GHz transceiver are shown.

Crosstalk might be a big issue for a wireless readout system in a tracking detector. Direct crosstalk can be avoided by using directive antennas, linearly polarised waves and frequency channelling. Reflections from tracking modules can be reduced by applying an absorbing material like graphite foam. Properties of different materials typically used in tracking detectors and graphite foam have been measured in the 60 GHz frequency range. Moreover, directive horn antennas made from aluminised thin Kapton foil have been tested successfully to focus the radio signal. In addition, linear polarisation of the wireless signal and parallel communication through different frequency channels have been analysed with respect to their benefit to reduce crosstalk.

13

A New Track Reconstruction Algorithm for the Mu3e Experiment based on a fast Multiple Scattering Fit

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A new track reconstruction algorithm developed for the high track multiplicity environment of the *Mu3e* experiment, where track uncertainties are dominated by multiple scattering, is presented.

The goal of the *Mu3e* experiment is to search for the lepton flavor violating decay $\mu^+ \to e^+e^-e^+$. To reach a sensitivity of 10^{-16} the experiment will be performed at a future high intensity beam line (*HiMB*) at the Paul-Scherrer Institute (Switzerland) providing more than 10^9 muons per second. Muons with a momentum of $\approx$ 28 MeV are stopped on a target. Their decay at rest, in which mainly low momentum positrons with energies below 53 MeV are produced, is analyzed by the *Mu3e* tracking detector consisting of four cylindrical layers of thin silicon pixel sensors. The high granularity of the pixel detector with a pixel size of 80×80 μm^2 allows for a precise track reconstruction in the high occupancy environment of the *Mu3e* experiment reaching 100 tracks per readout frame of 50 ns. These tracks will be reconstructed online using a triggerless readout scheme. The implementation of a fast 3-dimensional multiple scattering fit based on hit triplets, where spatial uncertainties are ignored, is described and performance results in the context of *Mu3e* experiment are presented. Also the implementation on Graphics Processor Units (GPUs) for fast online reconstruction is discussed.

14

Three-Dimensional Triplet Tracking for LHC and Future High Rate Experiments

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The hit combinatorial problem is one of the main challenges for track reconstruction and track triggering at high rate experiments.
At hadron colliders the dominant fraction (99%) of hits is due to low momentum tracks for which multiple scattering effects dominate hit resolution effects. Multiple scattering is also the dominating source for track uncertainties in low energy precision experiments.
In such environments, track reconstruction and fitting can be largely simplified using three-dimensional (3D) hit-triplets, where the track uncertainties are solely determined by multiple scattering effects at the middle hit layer.

Fitting of hit-triplets is particularly simple in experiments exploiting a solenoidal magnetic field.

In contrast to track reconstruction methods based on the linking of single hits or hit pairs (vector tracking) a triplet method provides full track parameters and does not suffer from fake combinations as the 3D-triplet fit is over-constrained.
Full tracks are step-wise reconstructed by connecting already fitted hit triplets, thus heavily reducing the combinatorial problem and enabling a fast track reconstruction.

The triplet method is ideally suited for pixel detectors, which allow to treat hits as space-points.
With the advent of relatively cheap and industrially available CMOS-sensors the construction higly granular full scale pixel tracking detectors is possible.
Tracking performance studies for full-scale pixel detectors, including the optimisation for 3D-triplet tracking are presented and compared to standard tracker designs and reconstruction methods.
The potential of reducing the number of tracking layers and - along with that- the material budget using this new tracking concept is discussed.
The possibility of using
3D-triplet tracking for track triggering or fast online tracking is also mentioned.

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Test of a Fast Cluster Finding Self-Seeded Trigger System for the ATLAS Upgrade

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The ABCN 130 chip developed for the high luminosity LHC upgrade of the ATLAS silicon strip tracker implements a Fast Cluster Finder (FCF). The FCF is capable of reading out certain track cluster information serially with a clock rate up to 640 MHz, sufficient to output the location within the 40 MHz collision frequency. An external correlator circuit can be used to find the position coincidence of clusters at two adjacent layers of silicon sensor. The coincidence offset is related to the transverse momentum of the track, and therefore it provides information which may contribute to a Level-1 trigger decision. These circuit elements have been implemented in sensor doublet configuration coupled to an FPGA which executes the correlator algorithm. Design and test results of this system will be presented.

17

Macro Pixel ASIC (MPA): The Readout ASIC for the Pixel-Strip (PS) module of the CMS Inner Tracker at HL-LHC

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The CMS tracker at HL-LHC is required to provide prompt information on high transverse momentum to the central level one trigger. The innermost part of the tracker is based on a combination of a pixelated sensor with a short strip sensor, the so-called Pixel-Strip module (PS). The readout of the sensors is carried out by two ASICs, the Strip Sensor ASIC (SSA) for the strip layer and the Macro Pixel ASIC (MPA) for the pixel layer. The processing of the data directly on the front-end module represents a design challenge due to the large data size (30720 pixels and 1920 strips per module) and the limited power budget. This is the reason why several studies have been carried out to find the best compromise between stub finding efficiency and power consumption.

This talk describes the current status of the ASIC development, focusing on the MPA chip development where the logic for the stub generation is implemented. An overview of the readout ASIC is presented with particular attention on the cluster reduction, position encoding and momentum discrimination logic. Concerning the testing, a software test bench capable of reading Monte-Carlo generated events has been developed and used to validate the MPA design and to evaluate the MPA performance. The obtained results will be reported and compared with the standard analysis software. In addition the first prototype of the MPA ASIC, namely the MPA-Light, will also be presented in the talk. The MPA-Light is scheduled for this year and will include the full analog functions and a part of the digital logic of the final version in order to qualify the chosen VLSI technology for the analog front-end, the module assembly and the low voltage digital supply.

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3-D Pixel Imagers with Exploitation of Delta-rays in Precision Tracking and Identification of Relativistic Particles

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no abstract summary only

Summary:

The scenario for long-term development at the Large Hadron Collider LHC is a further increase in luminosity, which might be beyond the current limits of the trigger capabilities of the experiments based primarily on emerging muons and large particle energy deposits in the calorimeters. The community must investigate new approaches for detectors and their signals that would allow recognizing specific features of particles that emerge from a collision with high potential for new physics. When such features could be identified locally within the tracker, or closeby, a more effective trigger could be constructed and higher intensities may become acceptable. One possibility under discussion is the recognition of a “stiff-track”, high momentum particles such as muons, by correlating signals in closely spaced inner pixel detector layers. Here we like to describe an even more ambitious possibility: exploitation of high-frequency delta-ray emission by relativistic charged particles when these traverse a 3-dimensionally arranged layer of pixel cells (see Fig. 1). Such a high-granularity active detector at the same time allows an order-of-magnitude improvement of precision on the spatial position of the particles that traverse this device, comparable to a passive nuclear emulsion. Several experiments have studied ‘glancing-angle’ incidence of minimum-ionizing particles in pixel detectors. In this case, delta-electrons are clearly recognizable via tracks as one or several off-trail pixels, or as a pixel with excess-signal, as visible in Fig. 1. Different generation processes compete, where some may provoke discontinuities. For example interaction of hadrons, emerging from the vertex, with silicon nuclei represents such a track discontinuity. For

the tracking a relatively thick silicon layer could bring near real-time information about 'energy-flow', and providing a 'pre-shower' identification potential.
-> Here is an essential and nice figure; how can I put this in ?????
Fig. 1. Selected tracks produced by energetic particles in the pixel detector Timepix onboard the ESA Proba-V satellite in LEO orbit at 820 km altitude. The particle identification can be done not only based on ionizing losses but also on energy distribution and density of observed delta electrons associated to the track. The track shape is influenced by dE/dx and by charge sharing in the process of charge collection across the silicon sensor depth (z-coordinate). a) High energy transfer heavy particle (high Z and high A), b) High energy transfer heavy particle (high Z and high A) accompanied by energetic light particles, c) high energy transfer light particle, d) MIPs.

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Beam test performance of the 2S prototype module for the High Luminosity Upgrade of the CMS Strip Tracker.

Author: Davide Braga[1]

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The 2S module for the High Luminosity upgrade of the CMS Tracker has recently passed an important milestone, with the first beam test of two versions of the prototype mini 2S modules equipped with both n-on-p and p-on-n strips sensors and read out by two CBC2 ASICs. The first test of the stacked strip sensors concept in beam also provided the opportunity to evaluate the CBC2 readout ASIC in beam and the integration with the bespoke uTCA-based DAQ. The CBC2 correlation logic appears to be working well, and the analysis of the Pt selection cut and of the performance of the system as a function of the particle incident angle is presented. Other recent activities such as the TID irradiation of the CBC2 ASIC are also presented.

Summary:

The mini 2S (strip-strip) module for the High Luminosity upgrade of the CMS Outer Tracker consists of a stack of two 5cm Si strip sensors read out by two CBC2 (CMS Binary Chip 2) ASICs. The module is assembled on a high-density hybrid and it is intended to prove the viability and the performance of the stacked sensor concept for selecting high Pt-tracks, as well as a demonstrator for the assembly and component developments.
In November 2013 the 2S prototype module passed an important milestone with the first beam test with 4GeV positrons at DESY. Such test was a first in many ways: the first beam test of the stacked silicon sensors concept, but also the opportunity to test the bespoke, Phase-II oriented uTCA DAQ, the first test of the performance of the CBC2 in beam and the first test with both p-on-n and n-on-p sensors, one of which not tested before.
During one week more than 120M events were recorded and this allowed extensive tuning of the commissioning steps, with trigger and stub latency scans and offset tuning, but also importantly to study the performance of the module with angular and threshold scans. The results from the analysis of these data will be presented: among these turn-on curves for the Pt selection cut, efficiency plots and cluster-width distribution as function of the particle incident angle.
Other recent activities such as the TID irradiation of the CBC2 ASIC are also presented.

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A Time-Multiplexed Track-Trigger architecture for CMS

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The CMS Tracker under development for the HL-LHC includes an outer tracker based on "PT-modules"which will provide track stubs based on coincident clusters in two closely spaced sensor layers, allowing the rejection of low transverse momentum hits before data transmission to the Level-1 trigger. The tracker data will be used to reconstruct track-segments in dedicated processors before onward transmission to other trigger processors which will combine tracker information with that originating from the calorimeter and muon detectors, to make the final L1 trigger decision.

The architecture for processing the tracker data is still an open question. One attractive option is to explore a Time Multiplexed design similar to the one which is currently being implemented in the CMS calorimeter trigger as part of the Phase I trigger upgrade.

The Time Multiplexed Trigger concept will be explained and the potential benefits of applying it for processing future tracker data using a possible design based on currently existing hardware will be described.

Summary:

There is now a well established baseline design for the future CMS Tracker to be used after 2025 at the HL-LHC. The upgrade requires complete replacement of the present tracker with a higher granularity detector which must contribute information to the Level 1 trigger. The working design contains a pixel detector at small radii and an outer tracker (30cm< r <120cm and end-caps) instrumented as two regions. The outermost region (60cm < r < 120cm, and outer end-cap disks) will be populated by so-called 2S-PT modules with two closely spaced microstrip sensor layers, providing L1 triggering information by correlating hits in the two layers to reject low transverse momentum track hits, and reduce the L1 data volume. The 2S designation refers to the two microstrip-sensor layers. A similar approach is adopted for the inner region of the outer tracker with increased segmentation in z, where one of the sensor layers is coarsely pixelated, hence known as PS modules.

A novel, highly flexible processing architecture for the calorimeter trigger has been adopted by CMS for the Phase I upgrade. In a traditional trigger system, each module processes data from a small part of the detector using pipelined logic. Seamless coverage of the detector requires many cross-links between modules, and the dataflow architecture is fixed in the system design, for instance by the routing on crate backplanes. In the Time-Multiplexed Trigger (TMT), the system instead transfers all data corresponding to a given bunch-crossing into a single hardware module, with many identical modules working in parallel on different bunch-crossings. This approach is similar to that used by the CMS event builder.

The new calorimeter TMT trigger is designed with two layers. The first transfers data rapidly to the Layer 2 processing nodes where trigger algorithms run, but the system can be constructed with identical boards in both layers with advantages for maintenance, operation and overall cost. The current μTCA FPGA processor board is called the MP7, based on a Xilinx Virtex-7 FPGA and Avago MiniPOD optics, which provides a powerful flexible processor core with 72 input and 72 output serial optical links, all running at 10 Gbps. The new system has been successfully demonstrated in a series of tests and will be commissioned in CMS during 2015 data taking, in parallel with the existing trigger, so that it can be deployed during 2016 operations.

The TMT architecture can be deployed in a future tracking system. A conceptual design for such a system, based on MP7s, has been devised which allows to estimate the requirements to build such a system. The first layer of MP7s would perform the function of the Front End Drivers in the present CMS silicon tracker but also transmit the tracker data to a second layer of MP7s which would carry out the track finding which is envisaged to take place in the Layer 2 FPGAs. One reason to investigate this approach is to establish whether this method of track finding can be proven to work with an acceptable efficiency and latency, which must be a few μs.

Progress with the TMT in the Phase I calorimeter trigger will be summarised. The Phase II track-trigger system design will be explained including the motivations for the parameters adopted. A demonstrator

system can be constructed using available hardware and is planned to take place during 2014. The plans to do this will be described.

21

R&D on detector components using 3D IC for LHC upgrades and other future detectors

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Three dimensional integrated circuit technologies offer the possibility of fabricating large area arrays of sensors integrated with complex electronics with minimal dead area, which makes them ideally suited for applications at the LHC upgraded detectors and other future detectors. We describe the ongoing R&D efforts to demonstrate functionality of components of such detectors. This includes testing of TSV technology, fabrication and testing of silicon or glass interposer structures to assemble arrays that integrate and match the pitch of large area sensors with arrays of readout integrated circuits, as well as the study of integrated 3D electronics with active edge sensors to produce "active tiles" which can be tested and assembled in to arrays of arbitrary size with high yield. The latter includes studies of possible post-processing to achieve active edges without the complexity of silicon-on-insulator sensor assemblies.

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Sensors with several different pixel geometries assembled into modules with common pixel ASIC

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ATLAS is proposing to replace the entire tracking system for operation at the HL-LHC. The baseline pixel geometry at higher radii is 50x250um, based on the FE-I4 readout chip and is optimized for the central barrel region. The tracking performance in the end-cap pixel disks can benefit from enhanced resolution in the R-direction to improve the Z-resolution of the track vertex reconstruction, which is critical in the high pile-up environment of the HL-LHC. So called strixel geometries, with long narrow pixels, are proposed at higher z in the barrel where tracks pass through at large angles. Larger

pixels can also be considered for an additional pixel layer if this could reduce the requirements, and therefore cost, for the outer part of the tracker.

This presentation will report on the development and testing of pixel sensors with different geometries assembled into modules with the FE-I4 readout chip: 50μm x250μm (the size that matches the front end), 25μm x500μm , 100μm x 125μm, 125 μm x167 μm, 50μm x2000μm and 25 μmx2000μm "strixels" for the outer regions of the barrel pixel system. The sensors with geometries 50μm x250μm, 25μm x500μm, 100μm x 125μm were irradiated and tested at the DESY testbeam. These and other testbeam results as well as results from characterization of these sensors in the laboratory will be presented.

Summary:

The approach demonstrated here allows much greater flexibility in optimizing the detector in different eta ranges without the need for multiple ASIC designs. This offers significant potential advantages in development of a variety of pixel modules or paired pixel assemblies which can all be based on a common format ASIC design. Given the design effort and fabrication costs of advanced pixel ASICs, the approach can represent a significant saving in cost and time for achieving a detector which is better matched for the full coverage and not just for the regions where tracks are near orthogonal to the sensor surface.

24

Simulation and performance of an artificial retina algorithm for 40 MHz track reconstruction

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We present the results of a detailed C++ simulation of the artificial retina pattern-recognition algorithm, designed to reconstruct events with hundreds of charged-particle tracks in pixel detectors at 40 MHz. The detailed geometry and charged-particle's activity of a large tracking detector are simulated and used to assess the performance of the artificial retina algorithm. We find that offline-like quality tracking is possible with sub microsecond latencies.

25

Multi-Gigabit Low-Power Radiation-Tolerant Data Links for High Energy Physics Experiments

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This work presents data link technologies that are capable of multi-gigabit data-transmission rates in the harsh environments typical of High Energy Physics (HEP) experiments. The presented modules are IP cores – designs that can be incorporated into HEP ASICs to enable fast data transfer. We developed two data link versions in a 130nm CMOS process. A low-power 1Gbps serializer and deserializer that work at ˜1mW each, a pair of transmit and receive differential 3GHz I/O drivers that consume 6mW and 22mW respectively. An additional 5Gbps data link has been developed. The data link is based on a 8mW serializer integrated with a 35 mW for transmitter and a 5mW deserializer integrated with a 5 mW receive amplifier. The 5Gbps link uses a unique pseudo-synchronous encoding, allowing it to operate asynchronously for short bursts, 4 bits at a time in our implementation. This operating mode does not require a high-speed clock in either transmit or receive devices. Projections for behavior at the 65 nm node are also presented.

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Thin pixel assembly fabrication development with backside compensation layer

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ATLAS is proposing to replace the entire tracking system for operation at the HL-LHC. This will include a significantly larger pixel detector. It is critical to reduce the mass of the pixel modules and this requires thinning both the sensor and readout to 150 micrometers. The bump yield in module assembly using solder based bump bonding can be problematic due to wafer bowing during processing at high temperatures. A new bump-bonding process using backside compensation to address the issue of low yield will be presented. Results from characterisation of thinned readout wafers and the effect of applying backside compensation will be presented.
This work is presented on behalf of the UK ATLAS Pixel collaboration.

Summary:

The ATLAS FE-I4 ROIC is almost 20 mm x 20 mm in size with order 10 micrometers of metal and dielectrics above the CMOS implants. When the die is thinned to a few hundred micrometers it tends to bow due to the stress in the dielectric/metal layers no longer being resisted by a thick silicon substrate. This bowing is increased further at elevated temperatures due to the different coefficient of thermal expansions of the dielectric/metal layers and silicon substrate. Solder based bump-bonding takes place typically at 260C and will increase the bow of the die significantly to several hundred micrometers. The size of the solder bumps are only 25 micrometers in diameter. Therefore, bowing of the ROIC will cause issues with the yield of the solder connections as they will not make electrical connection with the sensor and ROIC.
The work will show that the bow of the die can be affected with the use of a post-processed dielectric layer deposited on the backside of the wafer. The bow of the FE-I4 die as a function of die temperature for different backside dielectric deposition is shown. The details of the fabrication process and the characterisation techniques are described, as well as the final result. The processing technologies have been chosen to be compatible with both the existing CMOS ROIC but also with the through-silion-via, TSV, technology of the foundry.

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The artificial retina processor for track reconstruction at the LHC crossing rate

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We present the results of an R&D study for a specialized processor capable of precisely reconstructing events with hundreds of charged-particle tracks in pixel detectors
at 40 MHz, thus suitable for processing LHC events at the full crossing frequency. We design a massively parallel pattern-recognition algorithm, inspired by studies of the processing of visual images by the brain as it happens in nature, and propose an efficient hardware implementation in modern, high-speed, high-bandwidth FPGA devices.

28

Design and Assembly Studies for Track Trigger Modules

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High luminosity upgrade of the LHC will require that tracking detectors participate in the lowest levels of trigger decisions. The implementation of such track-trigger logic systems will necessitate local processing of information and sparsification of data transmitted to global processors. Further, such a system will require dense interconnections between various sensors, readout electronics and local trigger logic. We will describe R&D efforts aimed at optimizing module concepts and mechanical designs that realize this functionality. We will also describe interconnect technologies that will be employed in such assemblies. Progress in prototyping of modules will be presented.

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Introduction

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Welcome from Department Chair

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Bio-inspired vision sensors and processing systems

Biology provides us with a fascinating example of an intelligent, low-power, and highly efficient sensory system. With the advances in CMOS technology, it has become feasible to build microelectronic systems that mimic some of the key features found in biology. The presentation describes our work on neuromorphic vision sensors that include on-chip processing modeled after the biological system. This will include a retina-like imager, a focal-plane multi-mode imager and a polarizer imager. If time permits we will give a brief overview of a wireless Brain-Machine-Brain Interface

(BMBI) system whose purpose is to effectively link the brain to external hardware to create new sensory and motor pathways for persons suffering from neurological disorders.

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Discussion

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Discussion

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Close-out