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Multi-Gigabit Low-Power Radiation-Tolerant Data Links for High Energy Physics Experiments

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This work presents data link technologies that are capable of multi-gigabit data-transmission rates in the harsh environments typical of High Energy Physics (HEP) experiments. The presented modules are IP cores – designs that can be incorporated into HEP ASICs to enable fast data transfer. We developed two data link versions in a 130nm CMOS process. A low-power 1Gbps serializer and deserializer that work at $\sim 1\text{mW}$ each, a pair of transmit and receive differential 3GHz I/O drivers that consume 6mW and 22mW respectively. An additional 5Gbps data link has been developed. The data link is based on a 8mW serializer integrated with a 35 mW for transmitter and a 5mW deserializer integrated with a 5 mW receive amplifier. The 5Gbps link uses a unique pseudo-synchronous encoding, allowing it to operate asynchronously for short bursts, 4 bits at a time in our implementation. This operating mode does not require a high-speed clock in either transmit or receive devices. Projections for behavior at the 65 nm node are also presented.

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