Contribution ID: **26** Type: **Oral presentation**

Thin pixel assembly fabrication development with backside compensation layer

Friday, 16 May 2014 09:30 (30 minutes)

ATLAS is proposing to replace the entire tracking system for operation at the HL-LHC. This will include a significantly larger pixel detector. It is critical to reduce the mass of the pixel modules and this requires thinning both the sensor and readout to 150 micrometers. The bump yield in module assembly using solder based bump bonding can be problematic due to wafer bowing during processing at high temperatures. A new bump-bonding process using backside compensation to address the issue of low yield will be presented. Results from characterisation of thinned readout wafers and the effect of applying backside compensation will be presented.
This work is presented on behalf of the UK ATLAS Pixel collaboration.

Summary

The ATLAS FE-I4 ROIC is almost 20 mm x 20 mm in size with order 10 micrometers of metal and dielectrics above the CMOS implants. When the die is thinned to a few hundred micrometers it tends to bow due to the stress in the dielectric/metal layers no longer being resisted by a thick silicon substrate. This bowing is increased further at elevated temperatures due to the different coefficient of thermal expansions of the dielectric/metal layers and silicon substrate. Solder based bump-bonding takes place typically at 260C and will increase the bow of the die significantly to several hundred micrometers. The size of the solder bumps are only 25 micrometers in diameter. Therefore, bowing of the ROIC will cause issues with the yield of the solder connections as they will not make electrical connection with the sensor and ROIC.
The work will show that the bow of the die can be affected with the use of a post-processed dielectric layer deposited on the backside of the wafer. The bow of the FE-I4 die as a function of die temperature for different backside dielectric deposition is shown. The details of the fabrication process and the characterisation techniques are described, as well as the final result. The processing technologies have been chosen to be compatible with both the existing CMOS ROIC but also with the through-silion-via, TSV, technology of the foundry.

Primary author: BATES, Richard (University of Glasgow (GB))

Presenter: BATES, Richard (University of Glasgow (GB))