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Sensors with several different pixel geometries assembled into modules with common pixel ASIC

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ATLAS is proposing to replace the entire tracking system for operation at the HL-LHC. The baseline pixel geometry at higher radii is $50 \times 250 \mu\text{m}$, based on the FE-I4 readout chip and is optimized for the central barrel region. The tracking performance in the end-cap pixel disks can benefit from enhanced resolution in the R-direction to improve the Z-resolution of the track vertex reconstruction, which is critical in the high pile-up environment of the HL-LHC. So called strixel geometries, with long narrow pixels, are proposed at higher z in the barrel where tracks pass through at large angles. Larger pixels can also be considered for an additional pixel layer if this could reduce the requirements, and therefore cost, for the outer part of the tracker.

This presentation will report on the development and testing of pixel sensors with different geometries assembled into modules with the FE-I4 readout chip: $50 \mu\text{m} \times 250 \mu\text{m}$ (the size that matches the front end), $25 \mu\text{m} \times 500 \mu\text{m}$, $100 \mu\text{m} \times 125 \mu\text{m}$, $125 \mu\text{m} \times 167 \mu\text{m}$, $50 \mu\text{m} \times 2000 \mu\text{m}$ and $25 \mu\text{m} \times 2000 \mu\text{m}$ “strixels” for the outer regions of the barrel pixel system. The sensors with geometries $50 \mu\text{m} \times 250 \mu\text{m}$, $25 \mu\text{m} \times 500 \mu\text{m}$, $100 \mu\text{m} \times 125 \mu\text{m}$ were irradiated and tested at the DESY testbeam. These and other testbeam results as well as results from characterization of these sensors in the laboratory will be presented.

Summary

The approach demonstrated here allows much greater flexibility in optimizing the detector in different eta ranges without the need for multiple ASIC designs. This offers significant potential advantages in development of a variety of pixel modules or paired pixel assemblies which can all be based on a common format ASIC design. Given the design effort and fabrication costs of advanced pixel ASICs, the approach can represent a significant saving in cost and time for achieving a detector which is better matched for the full coverage and not just for the regions where tracks are near orthogonal to the sensor surface.

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