Contribution ID: **5** Type: **Oral presentation**

Towards a Level-1 tracking trigger for the ATLAS experiment at the High Luminosity LHC

Wednesday, May 14, 2014 10:30 AM (30 minutes)

The future plans for the LHC accelerator allow, through a schedule of phased upgrades, an increase in the average instantaneous luminosity by a factor 5 with respect to the original design luminosity. The ATLAS experiment at the LHC will be able to maximise the physics potential from this higher luminosity only if the detector, trigger and DAQ infrastructure are adapted to handle the sustained increase in particle production rates.

In this paper the changes expected to be required to the ATLAS detectors and trigger system to fulfill the demands of such a high luminosity scenario are described. The increased number of interactions per bunch crossing will result in higher occupancy in the detectors and increased rates at each level of the trigger system. The trigger selection will improve the selectivity, partly from increased granularity for the sub detectors and the consequent higher resolutions achievable. One of the largest challenges will be the provision of tracking information at the first trigger level, which should allow a large increase in the rejection power at this stage of the selection and yet still allow the full physics potential of the experiment to be fulfilled. In particular, reconstructing objects at the electroweak scale will still require that the thresholds on the transverse momenta of particles be kept as low as possible. Tracking provides essential information of this kind for individual particles so it is desirable to attempt to reconstruct tracks as early in the trigger chain as possible.

The ability to apply fast processing that can take account of the properties of the tracks that are being reconstructed will enhance the rejection, while retaining high efficiency for events with desired signatures, such as high momentum leptons or multiple jets. Studies to understand the feasibility of such a system have begun, and proceed in two directions: a fast readout for high granularity silicon detectors, and a fast pattern recognition algorithm to be applied just after the Front-End readout for specific sub detectors. Both existing, and novel technologies can offer solutions. The aim of these studies is to determine the parameter space to which this system must be adapted. The status of ongoing tests on specific hardware components crucial for this system, both to increase the ATLAS physics potential and fully satisfy the trigger requirements at very high luminosities are discussed.

Summary

A luminosity upgrade for the LHC[1] is foreseen for 2024 in order to allow increased phase space coverage both for searches and precision Higgs physics. For this high luminosity LHC (HL-LHC), instantaneous luminosities around $7\times10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ are expected, delivering around $300\mathrm{fb}^{-1}$ per year. At these high luminosities, mean numbers of separate pp interactions in the range of 160-200 are expected for every bunch crossing. Event rates for single lepton candidates passing the Level 1 (L1) triggers in the ATLAS[2][3] detector using the current trigger strategy are expected to be of the order of 200-400 kHz for each lepton species individually, with jet and other physics signatures providing some significant rate in addition. The current ATLAS trigger strategy uses only coarse granularity Calorimeter and Muon Spectrometer information at Level 1, with full granularity data including tracking information from the Inner Detector used in the High Level Trigger (HLT). Processing this rate of output from L1 is not possible in the HLT.

For the HL-LHC upgrade ATLAS will be equipped with an all-new Silicon Inner Tracker (ITK). Studies have been performed to evaluate the performance benefits of reconstructing tracks in the ITK at Level 1, and matching them to either calorimeter clusters or muon candidates. To enable the processing of the high rates from the HL-LHC, ATLAS has therefore proposed a Level 1 Track Trigger to work within a scenario where the current Level 1 processing is split into consecutive harware stages, denoted Level 0 (L0) and Level 1. Limitations from the front-end pipelines for no-longer accessible sub-detector components mean that any upgraded ATLAS trigger system will have only 20μs from the time of the bunch crossing until the L1 decision must arrive back at the detector front ends. The maximum L1 output rate that can be supported by these sub-detectors is 200 kHz. To operate within these constraints, in the split L0-L1 scenario the detector front end electronics for some sub-detectors will make use of a double buffer. In the L0 system the Calorimeter and Muon systems will process events using course granularity data to identify regions of interest (RoI) as in the current Level 1 trigger. The L0 decision will be distributed back to the detector front ends at the rate of 500 kHz to arrive 6μs after each bunch crossing. On a L0 accept the data from the primary buffers will be read into a secondary buffer where it will remain until the L1 decision arrives. Within the remaining 14μs both the transfer of the ITK data to the L1 track processor and the track reconstruction must be performed.

The readout latency is critical: if the data can be read out within 6μs then 8μs will remain for the tracking algorithm. Upon receipt of a Regional Readout Request (R3), identifying a particular RoI, each detector element within the RoI will read out a sub-sample of the data from the secondary buffer to the L1 processing systems. For each L0 accept it is expected that the average number, and size of all the RoIs in each event will comprise only about 10% of the total data volume within the event. In this way, only 10% of the detector need be read out, such that the total event rate to be read out to the L1 system will be 50kHz only 10% of the 500 kHz L0 accept rate. The readout of the ITK strip tracker is arranged by module: each module reading out the strips using several daisy-chained identical front end ASIC (ABC130), which use 130 nm CMOS technology. Studies using a discrete event simulation of the complete readout chain from the distribution of the R3 and L1 accept requests, to readout through the Hybrid Chip Controller (HCC) to the off-detector electronics have been performed using simulated ITK hit occupancies expected from 200 pileup interactions per bunch crossing. These studies suggest that the R3-95% latency – the time taken to read out all packets from a hybrid for 95% of all R3 – for all modules in the inner most barrel layer of the ITK strip tracker, is safely within 6μs for the standard 200 kHz L1A rate. To help in this, the readout chip can contains logic to prioritise the read out of R3 data over that of data from a L1 accept. An additional

FIFO can be added to buffer the input on the HCC from each daisy chain. The latencies both with and without R3 data prioritisation and different FIFO depths on the HCC were measured for different regions of the tracker detector.

The tracking algorithm must complete execution in the remaining 8μs in this scenario. This is feasible with current technologies which make use of CAM (Content-addressable memory) to perform fast pattern-matching in the first stage of the selection, and fast fitting procedures in a second step, after the combinatorics have been reduced. The pattern-matching algorithm performance will move in a large parameter space, based on the number of coincidence layers of silicon, the system segmentation and the pattern resolution, with constraints provided by both hardware limitations, such as the input/output bandwidths and size of the pre-registered pattern content per processor, and physics requirements, such as the minimum track momentum to be selected. Studies are ongoing using detailed simulations of the ITK geometry and detector response in high pile-up environments in order to understand the connections between these parameters.

In this paper the results of studies that will drive the design of the L1 track system of ATLAS, together with the results of intermediate stage tests on prototype hardware that will extend the potential of this system are discussed.

[1]
L. Evans and P. Bryant, LHC Machine, Tech. Rep. JINST 3 (2008) S08001, CERN, Geneva, 2008.

[2] The ATLAS Collaboration; The ATLAS Experiment at the CERN Large Hadron Collided, JINST 3 (2008) no. 08, S08003, . http://stacks.iop.org/1748-0221/3/i=08/a=S08003.

[3]
The ATLAS Collaboration, Performance of the ATLAS Trigger System in 2010, Eur. Phys. J. C72 (2012) 1849.

Primary author: Dr MARTIN, Tim (University of Warwick)

Presenter: Dr MARTIN, Tim (University of Warwick)