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The Serial Link Processor for the Fast TracKer (FTK) processor at ATLAS

Wednesday, 14 May 2014 10:00 (30 minutes)

The Associative Memory (AM) system of the FTK processor has been designed to perform pattern matching using the hit information of the ATLAS silicon tracker. The AM is the heart of the FTK and it finds track candidates at low resolution that are seeds for a full resolution track fitting. To solve the very challenging data traffic problems inside the FTK, multiple designs and tests have been performed. The currently proposed solution is named the "Serial Link Processor"and is based on an extremely powerful network of 2 Gbit/s serial links.
This paper reports on the design of the Serial Link Processor consisting of the AM chip, an ASIC designed and optimized to perform pattern matching, and two types of boards, the Local Associative Memory Board (LAMB), a mezzanine where the AM chips are mounted, and the Associative Memory Board (AMB), a 9U VME board which holds and exercises four LAMBs. Special relevance will be given to the AMchip design that includes two custom cells optimized for low consumption.
We report also on the performance of a first prototype based on the use of a min@sic AM chip, a small but complete version of the final AM chip, built to test the new and fully serialized I/O. A dedicated LAMB prototype, named miniLAMB, with reduced functionalities, has been produced to test the mini@sic. The serialization of the AM chip I/O significantly simplified the LAMB design. We report on the characterization of the min@sic chip, the tests and performance of the integrated system mini@sic, miniLAMB and AMB.

Summary

The Associative Memory \1 (AM) system of the FTK processor \2 has been designed to perform pattern matching using the hit information of the ATLAS silicon tracker. The AM is the heart of the FTK. It finds track candidates at low resolution that are seeds for a full resolution track fitting. An array of 128 AM boards will provide 1 billion AM patterns that will perform pattern recognition for the FTK system. In order to achieve the pattern density of 8M patterns / AM board and stay within the power consumption limits significant R&D has been performed for both the AM chip and AM board. The recent developments for AM chip, LAMB and AM board are reported.

This contribution will focus on the design of the new Associative Memory chip (AMchip05) that is the last planned prototype for the Fast Tracker (FTK) system. The AMchip05 is a 12 mm2 ASIC using 65nm technology with I/O based on 11 serial links at 2 Gbit/s. We will report on the design choices and simulation results of the AMchip05. The design of the AMchip05 is based on the characterization of the previous mini@sic AM chip (see fig. 1) that uses for the first time the 2Gbps serial links for I/O. With respect to the mini@sic the AMchip05 further improves the power consumption per pattern and includes all features required for use in FTK and some improvements among which the possibility to have separate speeds for input and output channels in order to allow better performance for the same power consumption.

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Fig. 1: test setup for the mini@sic AM chip

After test and characterization, four of the first mini@sic AM chips have been installed on the mini-LAMB (see fig. 2) in order to test them in conditions close to those of their final use in FTK. We report the results of the mini-LAMB tests and of the new AMBSLP (see fig. 3).

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Fig. 2: test setup for the mini-LAMB

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Fig. 3: new AM board (AMBSLP) prototype

References:

\1 A. Andreani et al., "The AMchip04 and the processing unit prototype for the FastTracker", IOP J. Instr. 7, C08007 (2012).

\2 Andreani et al., The FastTracker Real Time Processor and Its Impact on Muon Isolation, Tau and b-Jet Online Selections at ATLAS, 2012 TNS Vol.: 59 , Issue:2, pp, 348 –357

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