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Hardware Implementation of FPGA based Level-1 Tracking

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This presentation describes a new approach for track reconstruction to be used in the Level 1 trigger. This is intended for the upgraded CMS all-silicon tracker, which is to be installed for the High Luminosity era of the LHC (HL-LHC). The track finding is seeded with pairs of hits from adjacent layers in the tracker that are combined to form 'tracklets'. The tracklets are projected to other layers (both outside-in and inside-out), where hits consistent with the trajectory of a high-pT track are added. The pT threshold for the tracks to be considered is 2 GeV. A linearized track fit provides the final 3-D track parameters. The strict timing requirements of the L1-trigger at CMS require that the fit is done within 5 us, which is within the estimates for the algorithm. The algorithm is such that allows for an integer implementation to be used on an FPGA. Currently we are working on a demonstrator hardware implementation using a Xilinx Virtex 6 FPGA.

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