	TID limit	Configuration Tolerant to SEUs	SEUs in functional blocks	Notes
MicroSemi ProAsic Flash	20-40 krad (very dependent on dose rate & refresh conditions/annealing)	Yes	Use TMR, embedded blocks should be tests (eg PLLs)	Already tested
MicroSemi SmartFusion2 Flash	?	Yes	Use TMR, embedded blocks should be tested (eg PLLs)	Very new and not tested much
AntiFuse	? (but higher than Flash. PINT was tested good to 150 krad)	Yes	Use TMR, embedded blocks should be tested (eg PLLs)	One shot only!
SRAM FPGA	100s krad	No: needs scrubbing	Use TMR, embedded blocks should be tested (eg PLLs)	Needs careful testing & scrubbing implementation

- Scrubbing is used in ALICE (flash device stores reference)
- Some new FPGAs have automatic procedure for correction (Kintex7, with external flash).
- Scrubbing has to be tested against expected SEU rate
- Vendors sell ‘rad-tol’ FPGAs, but they are expensive

  ‘rad-tol’ = sample-tested, MIL grade package

  ie the chip is the same as non-rad-tol
- How can we program the FPGAs in situ?