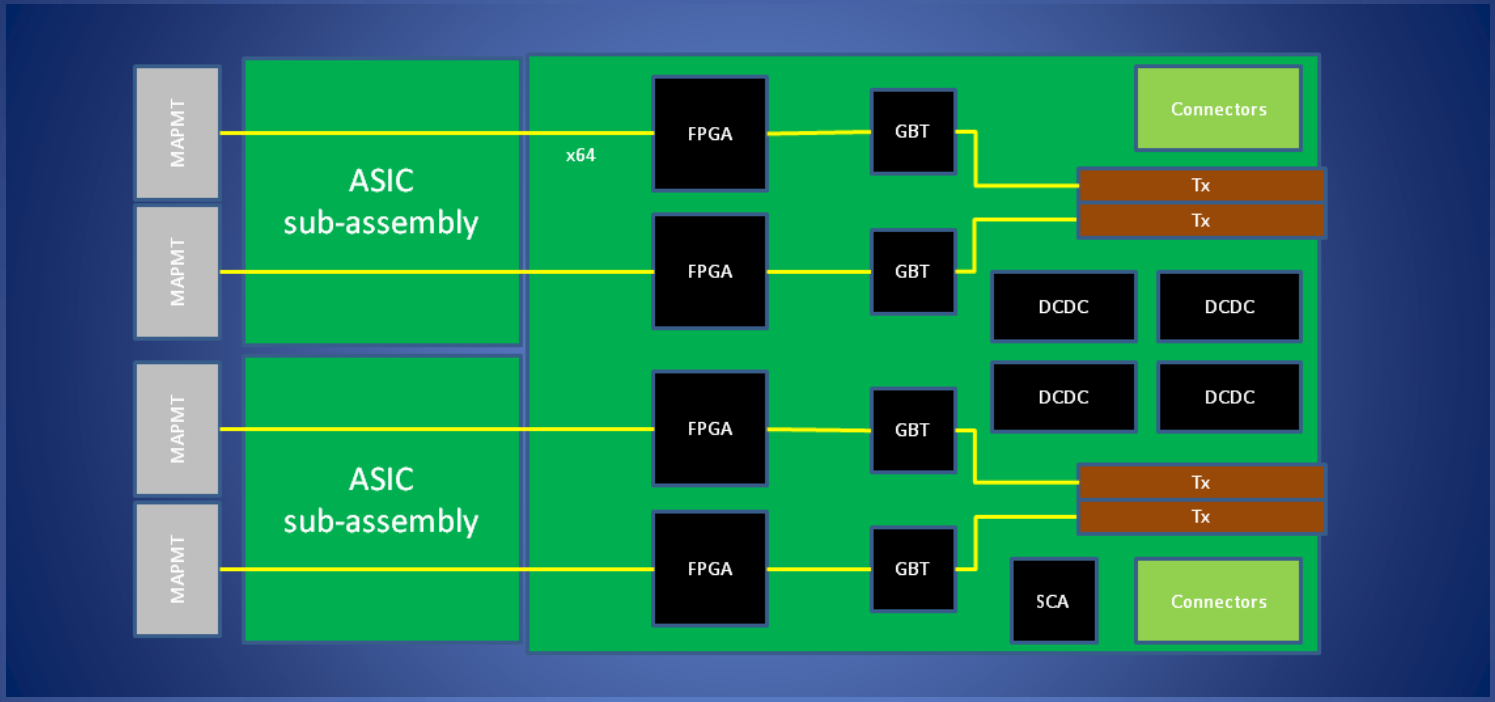
RICH FE FPGA Usage

RICH FE module



- RICH upgrade uses 64-channel photon-detectors (MAPMTs)
- Basic modularity is 4 MAPMTs per FE module
- CLARO ASIC does analogue to binary conversion
- Binary signals transmitted using up to four GBT links

- FPGA functions
  - Latch the binary signals
  - Do zero suppression (low occupancy region only)
  - Format GBT frames
  - Transmit to GBTX
  - Housekeeping and configuration etc.
- Too complex /risky to do in ASIC or anti-fuse

FPGA

Radiation tolerance

- Maximum annual dose 23krad
- ASIC or anti-fuse to risky
  - complex logic
  - long development cycle
  - risk of errors that only become apparent at a late stage
  - impossible to adapt to change in DAQ protocol
- Anti-fuse
  - PINT tested up to 150 krad
- MicroSemi ProASIC Flash
  - 20-40 krad
- MicroSemi SmartFusion
  - New, no data
- SRAM FPGA
  - 100 krad

Summary

- Little option other than SRAM FPGA
- Still need to select a device family
- Choice of FPGA has some knock-on consequences
  - Choice of DCDC converters (voltages)
  - Power dissipation
- Need to choose a family with a reasonable product lifetime
- RICH group would be interested to participate in FPGA radiation studies
- Current design requires large number of FPGAs
  - 2000 relatively small FPGAs for non-zero-suppressing modules
  - 400 larger ones for ZS modules.
- Need to keep costs under control
  - Avoid expensive FPGAs with features we don't require
  - Even Spartan-6 would probably satisfy our logic, IO and performance requirements
  - Only reason to choose a more expensive part would be if savings could then be made elsewhere (e.g. use built-in transceivers instead of GBTX)