SciFi detector FPGA's in radiation environment

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On behalf of the SciFi group

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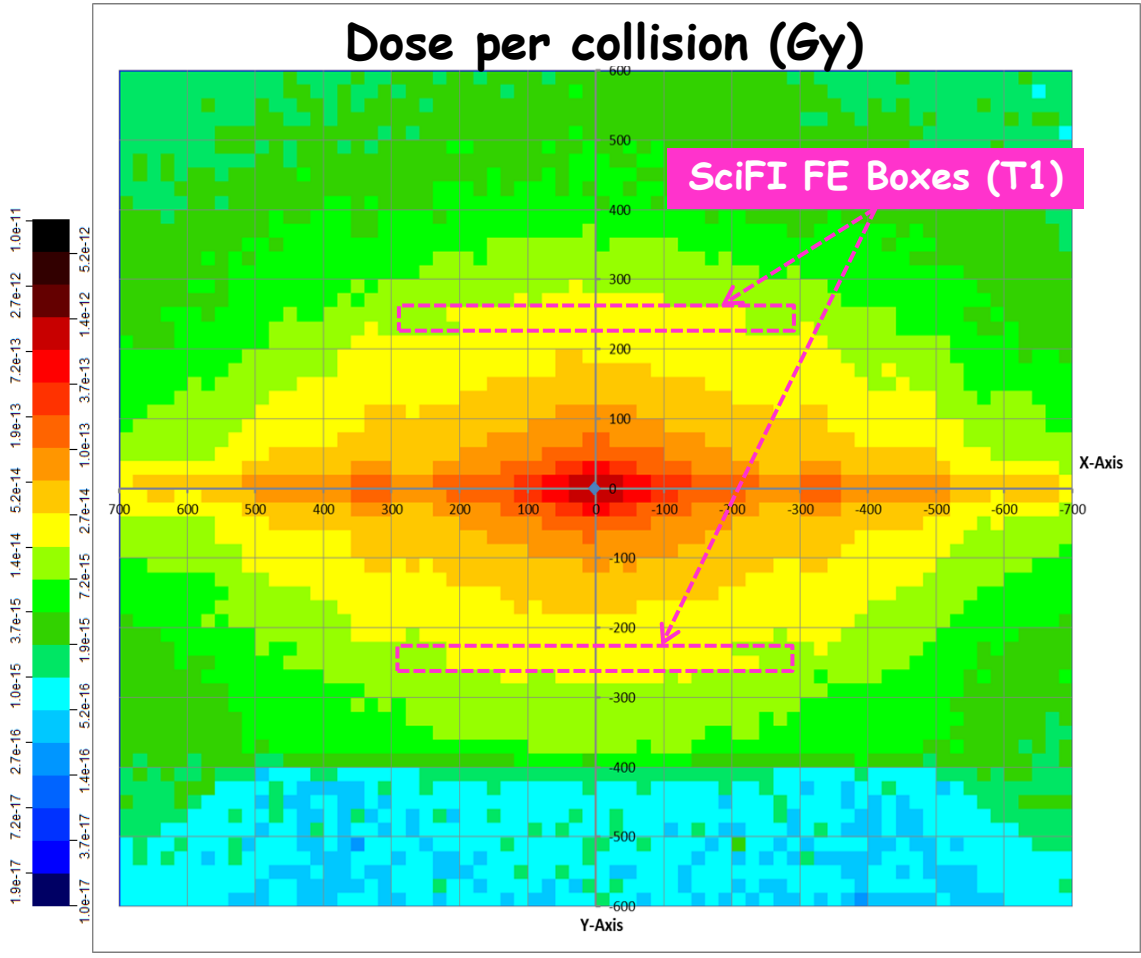
Radiation levels at the SciFi detector Front-end electronics

At FE location of T3 : ~1.44 Gray (0.144 krad) per fb^{-1}
e.g. ~7.2 krad for 50 fb^{-1}

Adopting a factor 2 safety for the simulation uncertainty and another factor 2 safety for the FE irradiation tests

a good figure to remember as radiation-hardness specification is ~30 krad



(see M. Karacson talk at 14 Feb 2013 Electronics meeting)

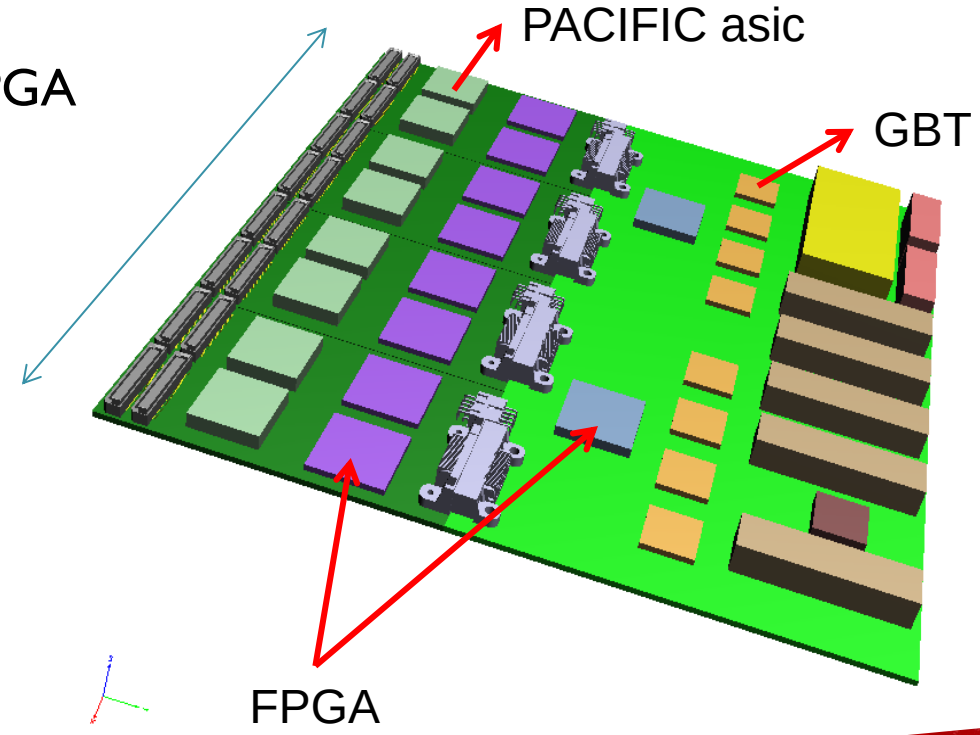
Straw tubes → SciFi

- Upgrade Outer Tracker
  - Replace the digital frond-end electronics by FPGA based TDC's
    - Advanced developments with Actel Proasic3E based TDC
    - Radiation test performed by Syracuse group
      - Unable to re-program after ~18 krad
      - TID limit ~30 krad

- SciFi detector
  - More logic resources needed for data compression algorithm
  - Microsemi Smartfusion2(SF2) / Igloo2, 65 nm flash based family
    - SF2 Silicon base for space qualified devices, probably the same
    - Option to use internal serializers / GBT protocol

SciFi Front end electronics

- Input data rate: 128 channels * 6 bit ADC at 40 MHz from PACIFIC asic
  - Needs data compression → channel clusterization
- 288 frond end boxes with each
  - 16 clusterization FPGA's
  - 4 concentrator / TFC Fan-out FPGA
- Total 5760 Microsemi FPGA's
- Specific FPGA cores
  - PLL
  - EPCS Serializer for GBT
  - Used SF2 because of availability,
    - design for Igloo2



Summary & Conclusions

- SciFi data compression algorithm
  - Unable to fit in Actel Proasic3E
  - SF2 limited resources (mid-range FPGA)
  - Fall-back: Xilinx Kintex-7 ☹
- No SF2 Irradiation results available yet
  - Waiting for Microsemi tests results, expected soon
- Nikhef didn't plan irradiation tests.
  - But offers to collaborate !

Spare slides

Actel ProAsic3E radiation tests

Tests of 3APE1500(-2) in 2010-2012 with 200Mev protons at Boston hospital
(Syracuse University, M. Artuso, E. Cowan, Bin Gui, D. Hsu, R. Mountain, JC Wang)

- see talk by R. Mountain in LHCb Electronis Upgrade Meeting 14/Oct/2010
- see talk by R. Mountain in LHCb Electronis Upgrade Meeting 21/Jul/2011
  - roughly reproduce results from SPECS test
  - RAM: few SEU every 3min run (few krad per run)
  - similarly for Flash ROM

- see talk by JC Wang in LHCb Electronics Upgrade Meeting 14/Feb/2012
  - dedicated test of PLL and Nikhef TDC firmware (see next slides)

Irradiation results Actel PLL & TDC

talk by JC Wang in LHCb Electronics Upgrade Meeting 14/Feb/2012

Verification	failed
Reconfiguration	failed x3
Power-cycle reconfiguration	failed

Results for FPGA 2 (received 45.6 krad)

Verification	OK
Reconfiguration	OK
Verification	OK

PLL lock error.
(run was with high intensity)

Change comparator value to 11: large error count is seen. Change back to 10.

Near station Computer crashed

LED indicates TDC = 12