

Matthias Saimpert D. Breton, E. Delagnes, J. Maalmi, C. Royon

CEA Saclay - Irfu/SEDI,SPP ; CNRS Orsay - IN2P3/LAL

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SAMpler for **PIC**osecond time pick-off : A read-out chip for the AFP timing detectors

- Application-Specific Integrated Circuit (ASIC) for picosecond timing measurement
- New patented concept based on Analog memory
 + Discriminator + Counter + Delay Locked Loops
 (DLL) + Analog to Digital Converter (ADC)
- 16 short Switch Capacitor Array (SCA), single-ended channels with embedded ADC and independent deadtime. Each is self-triggerable

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Timing measurement

- TimeStamp Gray counter (~ 6 ns step) sampling the external reference clock
- DLL (\simeq 150 ps step) defining a region of interest
- Waveform shape (few ps RMS after interpolation) acquired on a 64-step analog memory

Design status

Two working prototype available now

- 2 Mezzanine boards integrating SAMPIC with 16 acquisition channels available (MXC connectors)
- USB, Ethernet and Fiber Optic read-out
- 5V-1A supply required
- First tests gave satisfactory results (3-4 ps RMS reached) (see H. Grabas talk on http://qcdworkshop.ifj.edu.pl/)

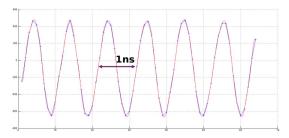


Test status (1/2)

(see H. Grabas talk on http://qcdworkshop.ifj.edu.pl/)

Chip usable now to perform timing measurement

- Sample speed from 1 to 8.2 Gigasample/s (GSPS) on all the channels
- Up to 10 GSPS on 8 channels
- Read-out error in a few cases and central trigger to correct
- Already very good sampling quality example of sampling of a sinus without any correction at 10 GSPS showed below



Test status (2/2)

2013: Early tests see H. Grabas talk on http://qcdworkshop.ifj.edu.pl/



- 25-28 Feb. 2014: Test-stand setup with TOTEM people at CERN. SAMPIC test with a pulser generator
- July 2014 (to be confirmed): Beam tests at the Paul Scherrer Institute (Switzerland) with low energy beams
- October-December 2014 (to be confirmed): Beam tests at CERN with the SPS (TOTEM beam test zone)
- Manpower: Yura, master student as of March to work on the SAMPIC software (9 months), money for 1 extra post-doc

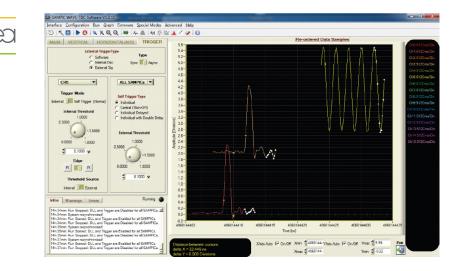
SAMPIC Acquisition software



- **Developped at LAL (Orsay, France)** by D.Breton and J.Maalmi
 - Windows software
 - Sets up SAMPIC and acquires signals. ASCII (tested) or binary (not tested) file outputs
 - Allows an **online vizualization** of the signals
 - Can perform different calibrations
 - Can perform online time measurements

Already usable for beam tests data acquisition

SAMPIC Acquisition software





Pedestals : residual signals due to component defaults (5 mV RMS)

acquisition with no signal on each channel for calibration

 Analog to Digital Converter (ADC) : non linearity of the transfer function, independent of the channel (1% RMS)

acquisition of different static ramps for calibration

 Timing Non Uniformity : Jitter on the sampling time (3% RMS)

acquisition of a sinusoid for calibration

Any other calibration can be implemented

SAMPIC Fast Analysis software

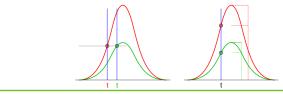
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- SPP/SEDI (Saclay, France) code in C++ interfaced with ROOT for data analysis (developped by myself)
 - Very light and adaptable code in order to test easily several time measurement methods
 - Convert ASCII data (offline) into a ROOT tree
 - Robustness to test by confronting it to different data
- **Purpose**: make it usable for beam tests data analysis

Time measurement algorithms implemented in the software (1/2)

Constant Fraction Discriminator (CFD)

- Pulse maximum determined directly from datapoints (default) or with a spline interpolation
- Fraction can be easily change, default is 50% of the maximum
- Crossing time determined by linear or spline interpolation
- CFD can theoritically be performed online by AFP
- Sensible to baseline shifts and linearity of the pulse slope



Time measurement algorithms implemented in the software (2/2)

Cross-correlation (CC)

- Possibility to add points to the original waveforms by spline interpolations before the CC computation
- Maximum of the correlation function determined by spline interpolation
- Less sensible to baseline shifts and linearity of the pulse slope
- Signal must show a very good reproductibility

Further SAMPIC developments required for AFP

Prototypes are not radiation-hard

not completely needed if SAMPIC is in the alcove

- if inside the tunnel, full radiation-hardness required
- Ping-pong mode (= 2 channels connected to a single detector cell) required to handle LHC rates

Checks/tests to perform to fully understand the chip

Minor bugs corrections

Signal attenuation and Delay tests with a pulse generator **at 6.4 GSPS**

Time measurement between two shifted pulses

Delay test

- SAMPIC Self-triggered
- I pulse split into 2 pulses (simple T-junction) of the same amplitude
- variable delays with different cables

Signal attenuation test

- SAMPIC Self-triggered
- 1 pulse split into 2 pulses (simple T-junction)
- varying amplitudes of the pulse with attenuators before splitting
- little timing offset between the two pulses with cables to mimic real conditions

Characteristics of the circuit



- Pulse generator (Lecroy)
 - Amplitude: 5V (before splitting and attenuation)
 - Width: 0.90 ns
 - Frequency: 1 kHz

Reducers

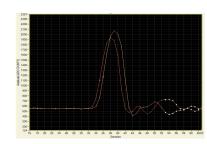
- High bandwidth attenuator (Wavetek, 3GHz) from 6 to 33 dB
- or Low bandwidth reducer (Ferisol, 500MHz) from 6 to 33 dB

Delayer

Use of cables of different lengths

Delay tests (\simeq 1.2 V pulse amplitude)

Visualization of the split pulses with the acquisition software



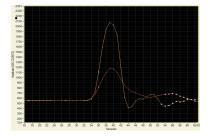
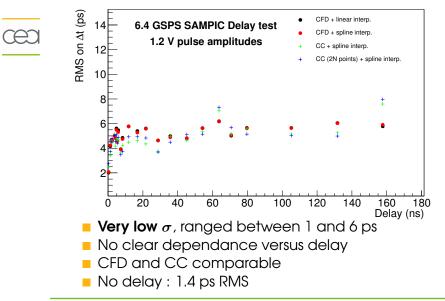


Figure : $\gamma\gamma$ production via γ exchanges

Figure : $\gamma\gamma$ production via gluon exchanges

 Signal distorsion and attenuation at high delay due to the increasing length of cables (skin effect and limited bandwidth)

Delay test results (\simeq 1.2 V pulse amplitude)



Signal attenuation tests with a 3 GHz bandwidth reducer (4.73 ns delay)

Visualization of the split pulses with the acquisition software

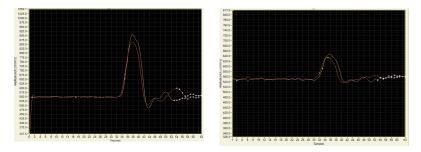
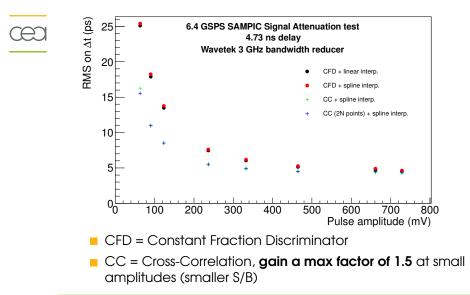


Figure : 12dB

Figure : 24dB

- Rising edge of the slope : 1 ns
- Good signal reproductibility

Signal attenuation tests with a 3 GHz bandwidth reducer (4.73 ns delay)



Signal attenuation tests with a 500 MHz bandwidth reducer (4.73 ns delay)

Visualization of the split pulses with the acquisition software

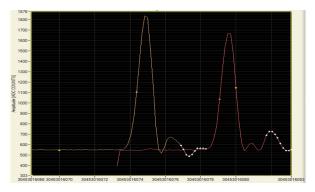
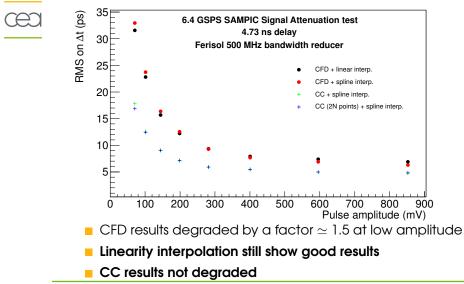


Figure : 0dB

Rising edge of the slope lasts 1.5 ns (+50%)

Signal attenuation tests with a 500 MHz bandwidth reducer (4.73 ns delay)



The SAMPIC chip for timing detectors

Elegant way to measure the jitter noise

the RMS on the time measurement of 1 pulse is the quadratic sum of the jitter noise σ_t and a term proportional to the rising edge of the pulse

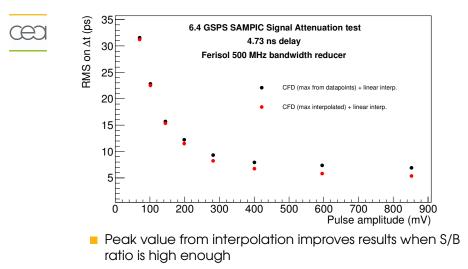
 Rising edge of the pulse inversely proportional to the amplitude (constant width pulses)

RMS (2 pulses) =
$$\sqrt{2}$$
 RMS(1 pulse) = $\sqrt{\sigma_t^2 + (\frac{K}{A})^2}$

- Jitter noise expected to be a few ps if the design is correct
- Results of the fit for the two attenuators with CC 2N points + spline interp. method
 - 3 GHz bandwidth: σ_t = 3.0 ps, K = 657 s.mV, χ^2 = 0.03
 - 500 MHz bandwidth: σ_t = 3.3 ps, K= 807 s.mV, χ^2 =0.04

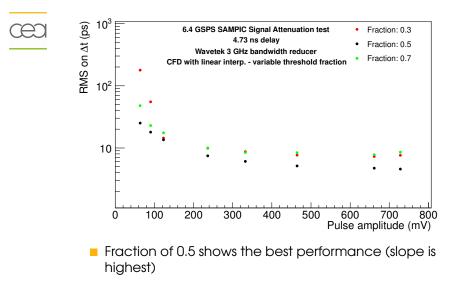
First validation of the SAMPIC design

Extra : CFD with fraction from interpolated maximum



Makes almost no difference at low S/B ratio

Extra : CFD algorithm performance against fraction



Conclusion

Good performance of SAMPIC confirmed

- 2 to 4 ps resolution achieved with a pulse generator and a basic CFD method
- Jitter noise measurement (3 ps) validates SAMPIC design
- Calibrations can still be improved
- Data acquisition can still be optimized (a few outliers were detected)

Conclusion

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- 2 to 4 ps resolution achieved with a pulse generator and a basic CFD method
- Jitter noise measurement (3 ps) validates SAMPIC design
- Calibrations can still be improved
- Data acquisition can still be optimized (a few outliers were detected)
- First test of the fast analysis C++/ROOT code and different time measurement algorithms
 - A simple CFD with maximum value picked from datapoints + linear interpolation is enough to give very good results
 - CFD ratio of 0.5 shows the best performance
 - CC improves the results but it might not be the case for real signals (reproductibility issue)

Plans for the SAMPIC fast analysis code

- Pre-treatment algorithm to isolate the main peak of the pulse to be coded
- **Signal template** to be built from data
- Use of binary data instead of ASCII data (faster acquisition time)
- **Cross-talk** effect to be studied
- Outliers to be looked at



The SAMPIC chip for timing detectors Back-up

Matthias Saimpert D. Breton, E. Delagnes, J. Maalmi, C. Royon

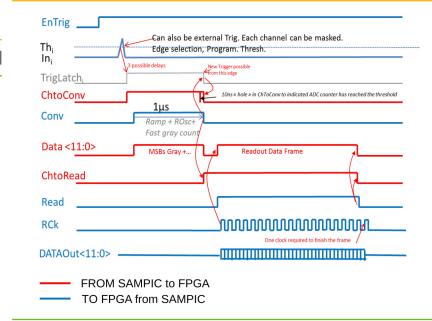
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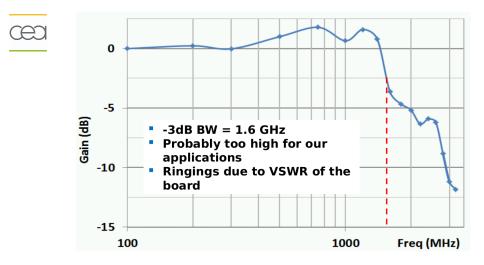
Austria Micro System 0.18 μm CMOS kit

- Based on IBM0.18m : IBM quality & documentation
- Good Standard Cells Library
- Good lifetime foreseen (HV module, automotive)
- 1.8V power supply: nice for analog design/ high dynamic range
- Reasonable leakages
- Good noise properties (already checked with IdefX chips for CdTe)
- Reasonable radiation hardness
- Less complex (and less expensive) than IBM 0.13m
- AMS high quality Design Kit
- Easy access (CMP, Europractice, AMS)

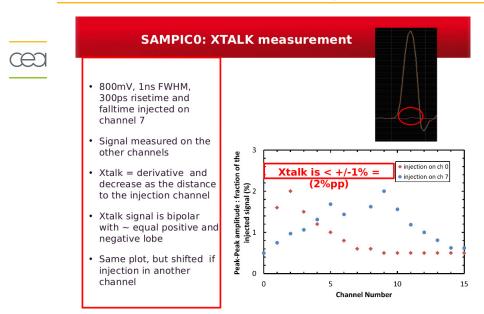
Operation



Bandwidth

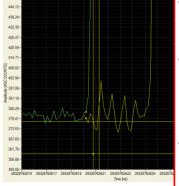


Cross-talk (E. Delagnes)



Cross-talk (E. Delagnes)

SAMPICO: Is it really derivative XTALK ?



450.00

- Instead of a short pulse, we send a longer pulse. Then we see that the Xtalk is not really derivative:
- The edge (green) triggers a damped oscillation with ~ 1.2 GHz frequency (yellow). With a short input pulse, we only see the first period of the sinewave
- This resonance frequency is the same for all the channels and unchanged if we change the sampling frequency

Consistent with the resonance

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Cross-talk (E. Delagnes)

SAMPICO: XTALK in the frequency domain

