Analysis and Calibration of a High Precision AD Converter

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Abstract

The accuracy of AD converters can be improved by error correction. The presented ADC analyzer and calibrator, based on a histogram test with small triangular input signals, determines the static errors like gain, offset and linearity. The advantages of the principle are fast results with a high level of confidence and small experimental burden.

I. Introduction

At the Paul Scherrer Institute PSI [1], a large number of fully digitally controlled magnet power supplies are in operation [2]. Current transducer and the following AD conversion of the measured current are the key elements of a high precision power supply. The accuracy achieved by commercially available current transducers is within the range of 1 ppm. It is essential to keep any degradation of these excellent properties by the succeeding stages as small as possible. Therefore, a very precise AD conversion is needed. A mere increase of the ADC resolution will not yield the expected results. The level of accuracy can only be achieved by measuring and correcting the miscellaneous errors of the ADC and all involved components like voltage reference, antialiasing filter and input amplifier.
The presented AD analyzer and calibrator acquires the static ADC errors like gain, offset and linearity. Corrections based on these parameters can be computed. The converted analog signals are corrected with the help of a lookup table (LUT) into very accurate digital equivalents. It should be noted that a successful correction is based on stable error conditions of the conversion circuitry.

II. ADC Performance Characteristics

The ADC converts an analogue quantity – normally a voltage – into a discrete digital value. Ideally, the transfer function (TF) or the relationship between input voltage and corresponding digital code describes a straight line. Because of limited ADC resolution, the transfer function represents a more or less coarse staircase green curve in Fig. 1.
Many parameters have been defined for a comprehensive description of the performance characteristics of an ADC. A first classification was arranged by standards committees into static (DC) and dynamic (AC) characteristics.
The DC characteristics (Fig. 1) like offset, gain, integral nonlinearity INL and differential nonlinearity DNL describe the static behavior. Temperature, aging and the tolerance of components are responsible for this class of non-idealities.

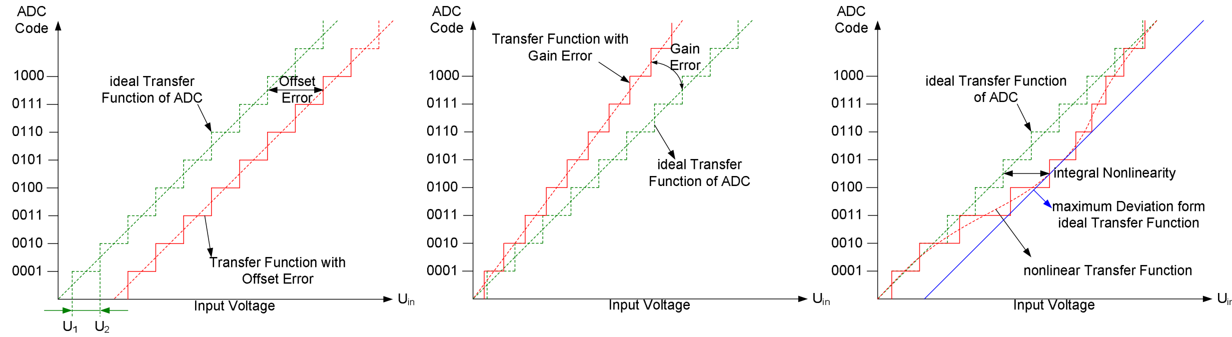

Fig. 1: Left: offset error; middle: gain error; right: DNL/INL error

The AC characteristics like - Signal-to-Noise SNR, Dynamic Range, Spurious-Free-Dynamic Range SFDR, Total Harmonic Distortion THD, Signal-to-(Noise + Distortion) S/[N+D] – describe the dynamic ADC behavior. The demands on very high precise magnet currents are needed at low frequencies primarily. Therefore, the focus of this paper will be the analysis and calibration of the DC characteristics. Modern highly integrated ADC architectures contain internal error correction circuits. But these internal characteristics are degraded by necessary external circuits like anti-aliasing filter, external voltage reference and more.

The presented method is not based on a dedicated ADC technology. For power electronic applications we prefer successive approximation register (SAR) types. This class of ADC is the best choice among high accuracy and small group delay.

III. Acquiring of the Static ADC Characteristics Gain, Offset and Linearity

The static ADC transfer functions as well as the static ADC characteristics are fully defined by the transitions voltages T[k]. They are defined as the voltage where both corresponding adjacent output codes obtain the same number of occurrences

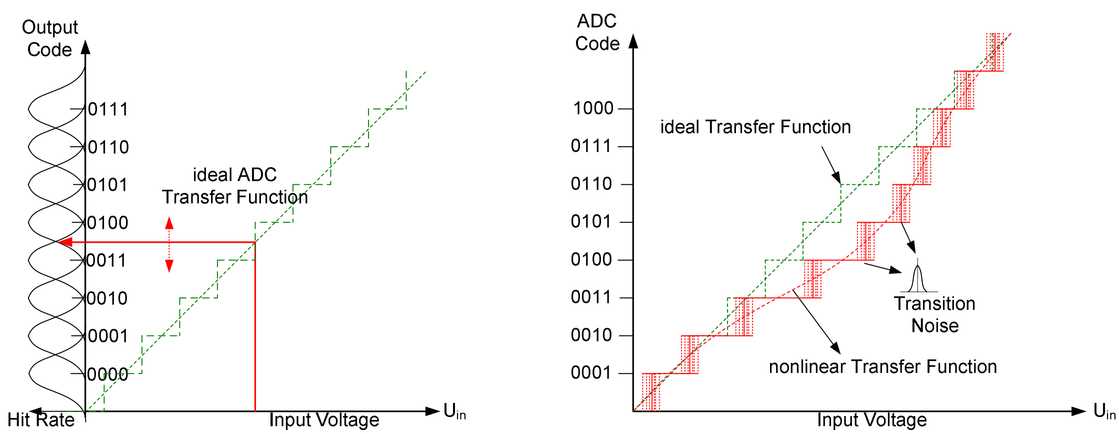

Fig. 2: Left: definition of transition level; right: transition noise

With an increasing number of ADC bits the number of transitions increases at the same degree and the transition levels come closer. Mainly induced by the noise of the voltage reference, the position of the transition varies with time, which is called transition noise (Fig. 2: right). Obviously, we cannot find the exact position of the transition levels by individual measurements. But we can determine the mean position of the transition levels with statistical methods.

The principle of the histogram method

The stimulus is generated by a precise function generator. The converted codes are accumulated in a histogram. A sine wave is commonly used as stimulus. It enables us to sweep the interesting frequency range and to determine the AC performance of the involved ADC. Nevertheless, the triangle or ramp function has several advantages if only the static characteristics have to be determined. The resulting histogram is uniform, which means that all codes have basically the same hit rate (Fig. 3).

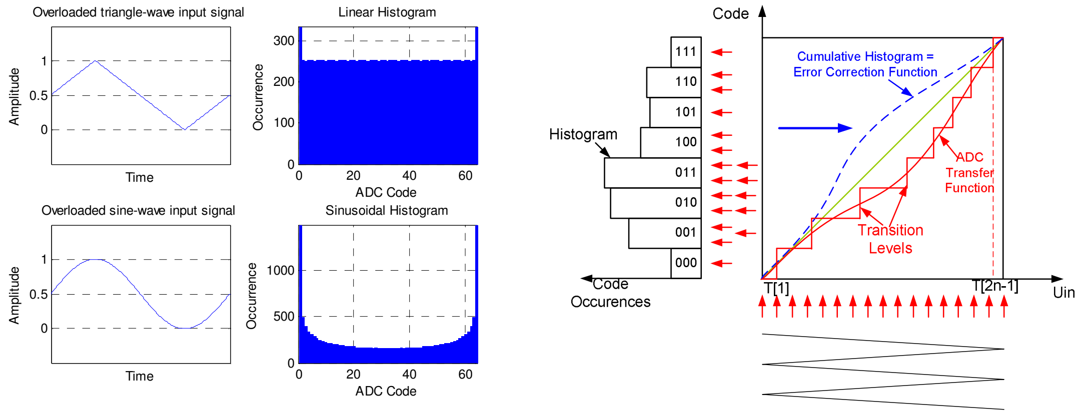

Fig. 3: Left: histograms of an ideal ADC with different stimulus; right: histogram with full scale triangle

As the DC performances are very important in our application, we will focus on the triangular method. As mentioned above the occurrences of all codes should be equal as long as the transfer function is a straight line. But the resulting histogram is very sensitive to nonlinearities in the real transfer function.
Starting with a single triangular stimulus sweeping over the full ADC range, isochronous conversions are performed. To show the principle the nonlinear transfer function is overdrawn. In flat areas of the transfer function, the steps are wider than in sharp rising areas. Therefore, in these areas the probability of a hit of the corresponding codes is higher, as shown in the resulting histogram. A cumulative histogram is built by adding up the different histogram values. Fortunately, the resulting function (blue line) is equal to the mirrored transfer function (around ideal TF) and can be used excellently as an error correction function (ECF).

The histogram method with small triangular waves

For a good reproducibility the resolution and precision of the stimulus should be considerably higher than the ADC itself. For instance, for an 18 bit ADC the requirements to the stimulus generator are 21 bit. High precision DC-calibrators are available on the market but their settling time is far too long (about 1 second) for the huge number of required measurements. A full calibration cycle would take days.
A new method, based on small triangular stimulus signals as depicted in Fig. 4: left, mitigates the requirements for the settling time of the DC calibrator and the accuracy of the triangular function generator (DAC). The basic idea is described in publication [3]. The test uses small triangular stimulus signals superimposed on a DC offset value produced by a precise and stable DC-calibrator. The particular histograms are finally merged into a single one.
The requirements on the linearity of the stimulus generator can be reduced by increasing the number of triangular waves. The loss of time for the setting of the different operating points is only short.

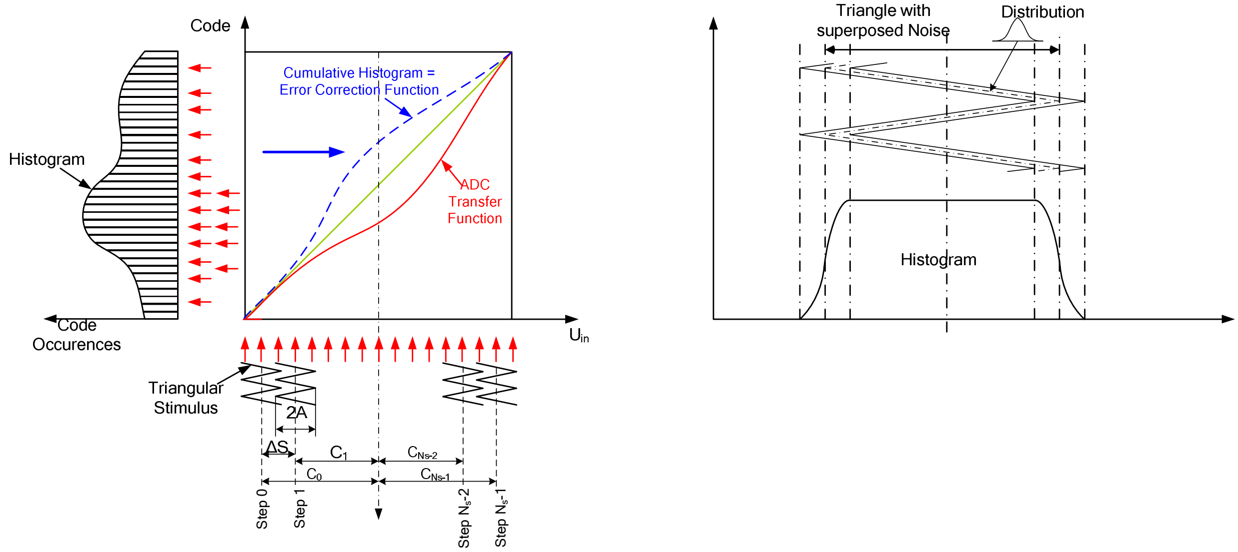

Fig. 4: Left: histogram with small triangular waves; right: shape of a single sub-histogram

As depicted in Fig. 4: right the triangular stimulus yields a uniform histogram with smooth transitions due to superimposed noise. For this reason the triangles are overlapped and - for the histograms merge - the unusable boundaries will be cut away (Fig. 5).

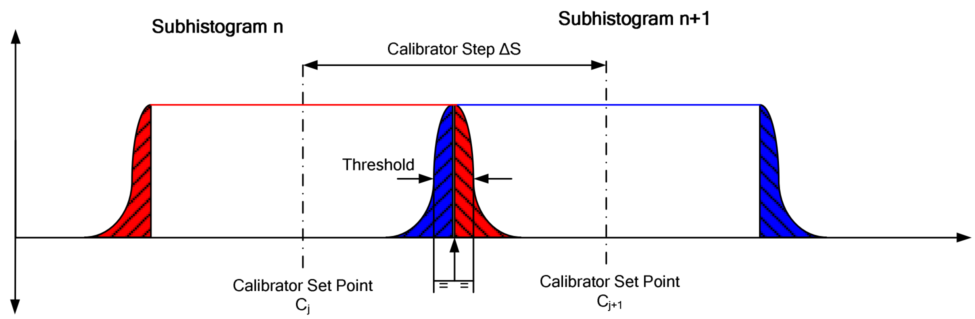

Fig. 5: Merging of sub-histograms

Algorithm:

1. Set the threshold value to 0.5 of mean occurrences.
2. Determine the beginning and end of each particular histogram.
3. Calculate the middle between the end of sub-histogram n and the beginning of sub-histogram n+1.
4. The histogram values farthest away from the calibrator set point C_j (red and blue areas) will be eliminated while merging the sub-histograms.

IV. Analysis and Calibration of a High Precision AD Converter

A Matlab based control system was designed for the data acquisition and analysis. The time critical parts, like sequencing and function generation, are implemented on a dedicated fast controller card. By successively increasing the DC offset voltage, the full ADC range can be processed. The numbers of occurrences of the converted output codes are accumulated in a histogram on the controller card. From this, a cumulative histogram is derived which contains information of all code transition levels and the differential and integral nonlinearity DNL/INL.

The function generator is operated synchronously to the sampling frequency of the ADC. This guarantees a maximum hit rate in each quantization interval and hence a high level of confidence for the determined

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transition levels. The test duration could be reduced by a factor of about 50 [3] compared to the traditional histogram test. With the exception of the point of reversion of the triangle, the gradient and therefore the dynamic conditions are the same over the full range.

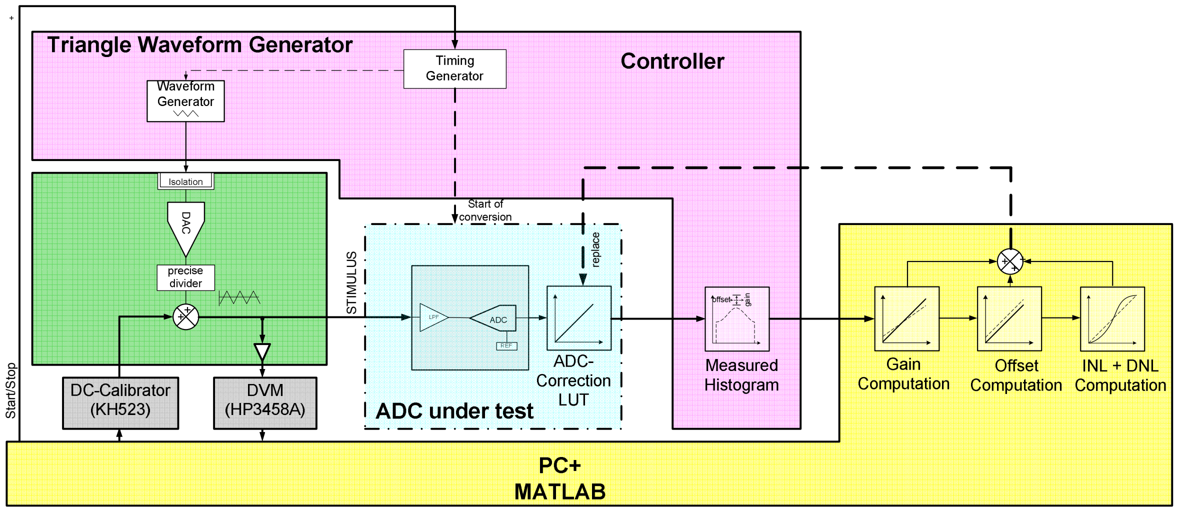

Fig. 6: Topology of AD analyzer and calibrator

The following considerations are based on the ideas of the IEC Standard 62008 [4]. The formalism was adopted as far as possible. Differences arose since the focus of this paper is on high precision and high resolution ADC and some operation could not be solved mathematically but by iterative processes. Minor differences result also through the use of a triangular generator, based on a DAC, which is updated synchronous to the ADC sampling rate.

Performance characteristics of the analysis and calibration system

For a precise and reproducible calibration, the following performance characteristics of the involved equipment have to be known precisely:

- Accuracy of the stimulus operating point
- Linearity of the triangular stimulus
- Noise superimposed on stimulus
- Stability over a single wave (minutes), a full calibration cycle (hours) and several calibration cycles (days)
- Temperature dependency

The most important characteristics of the calibration system are summarized in Table I. The DC-calibrator operating point as well as offset, gain and amplitude of the stimulus generator are aligned to the DVM (HP3458A). Doing so, the accuracy of the DVM is inherited by DC calibrator and stimulus generator. Therefore, the accuracy of the calibration system is mainly determined by the DVM. Unfortunately, the stability of the calibration system is influenced by changes in temperature. To minimize the temperature dependencies and thermoelectric effects, all equipment is placed in a cabinet which is temperature stabilized to +/- 1ºC. Thanks to the method with small triangular waves the requirements for the accuracy of the triangular function generator can be fulfilled by a standard precision DAC. The value for nonlinearity NL is related to one stimulus amplitude (peak-peak). The negative influence on the calibration accuracy decreases with increasing number of small triangular waves.

Table I: Important characteristics of the calibration system

Characteristics	Value
Relative accuracy DVM HP3458A Opt. 002 (24 hours)	0.55 ppm
Temperature coefficient DVM	0.16 ppm/°C
RMS noise DVM (@ integration time DVM = 20 ms)	0.09 ppm
Noise stimulus σ_N	0.75 ppm
Short term stability of stimulus (<2 hours) (Stimulus-board and KH523)	< 2 ppm
Nonlinearity NL and gain error of the triangular generator	70 ppm

Preparation of a calibration cycle

Based on the ADC parameters like number of bits, transfer curve type (unipolar, bipolar with true zero, bipolar with no true zero) and input voltage range, as well as the characteristics of the calibration system (Table I), the settings of the calibration cycle can be derived as follows:

The amplitude of a small triangular wave

The maximum feasible Amplitude A_{max} for the small triangular wave is given by gain error and nonlinearity of the triangular generator and the tolerable deviation from the ideal triangular function.

$$A \leq \frac{B_i \cdot Q}{NL} = A_{\max}; \quad Q = \frac{V_{FSR}}{2^n}; \tag{1}$$

where
n = number of bits of the ADC, B_i = tolerable deviation between actual and ideal triangular function expressed in least significant bit (LSB) (a good proposal is one stimulus increment), NL = nonlinearity of the triangular generator [LSB], Q = quantization interval [V], A_{max} = maximum amplitude [V], V_{FSR} = ADC full scale range [V].

Number of samples and number of stimulus periods

The accuracy of the analysis depends on the existing noise and can be improved by reducing the stimulus increment dS_{STIM} expressed in LSB and by increasing the number of stimulus periods N_{PER}. The number of histogram occurrences per ADC quantization interval (bin) is given by:

$$H_{bin} = \frac{2 \cdot N_{PER}}{dS_{STIM}}; \tag{2}$$

The total considerable noise is the sum of the stimulus noise σ_{SN} and the transition noise σ_{TN} which can be found in the datasheet of the used ADC.

$$\sigma = \sqrt{\left(\sigma_{TN}{}^2 + \sigma_{SN}{}^2\right)}; \tag{3}$$

The required number of samples depends on the tolerable standard deviation σ_T for the transitions:

$$\sigma_T = \frac{\sigma}{\sqrt{2 \cdot H_{bin}}}; \quad H_{bin} = \frac{1}{2} \cdot \frac{\sigma^2}{\sigma_T{}^2}; \tag{4}$$

where
σ = standard deviation of the total noise, in units of ideal code bin widths [LSB], σ_T = standard deviation of the resulting code transition level.

Number of small triangular waves

Distortions which typically occur on the peaks of the triangular waveform and the superimposed noise require a certain overlap of the triangular waveforms. A minimum overlap is also demanded by the merging process which is described later. Starting with the ADC full scale range V_{FSR} and the maximum feasible stimulus amplitude A_{max} from (1) the minimal number of steps N_{Smin} (without overlap) can be calculated as follows:

$$N_{S\min} = \frac{V_{FSR}}{2 \cdot A_{\max}}; \tag{5}$$

Afterwards, the number of waves N_S is increased, which is equivalent to reducing the calibrator step size ΔS (Fig. 4), until the required overlap by the merging process can be achieved.

Analysis

Determination of the offset- and gain-error

The ADC parameters offset and gain, which define the terminal points of the ADC transfer function, can be derived from the first T[1] and last transition levels T[2^n-1] („terminal dependent“) or by linear least-squares estimation techniques („terminal independent“). Basically, the „terminal independent“- method delivers more precise results for offset and gain (all transitions are involved). Nonetheless, the „terminal dependent“- technique was used, because the determined error correction function ECF is also terminal dependent (i.e. the ECF is fixed by T[1] and T[2^n-1]). The following iterative process has been introduced which allows a precise determination of the transitions T[1] and T[2^n-1]:

1. Starting with an input voltage U_{in} slightly above the negative fullscale voltage V_{FS-} a histogram is acquired as depicted in Fig. 7. Some noise must be present on the input voltage to find the precise mean value. Too much noise in contrast leads to an asymmetric histogram.
2. The mean value of this histogram is calculated. Assuming that the ADC has a “True Zero”- curve type the deviation Pos_{diff} to 0.5 is determined.
3. The correction voltage U_{corr} for the next iteration step is calculated from Pos_{diff}. The algorithm is repeated with a new input voltage $U_{in} = U_{in\ last} - U_{corr}$ until the deviation Pos_{diff} is tolerable.

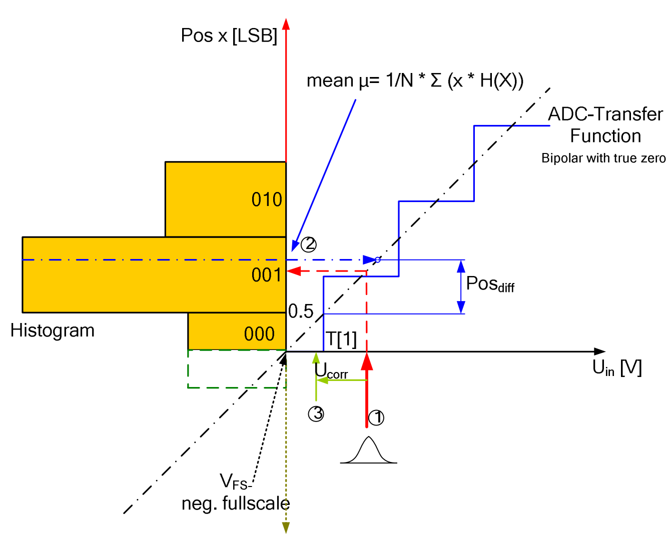

Fig. 7: Determination of the first and last transition (T[1] and T[2^n-1])

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Merging of the sub-histograms

As depicted in Fig. 5, a sub-histogram is produced for each small triangular stimulus. Finally, they are merged into a single histogram. Investigations with a 16 bit ADC have shown that the results of the IEC62008 method differ up to 1 LSB (16 ppm) from run to run. It can be shown that transition- and stimulus-noise are responsible for this effect. With the method described below the reproducibility could be increased from about 16 ppm to less than 4 ppm (Fig. 10):

1. The sub-histograms are merged as described in IEC62008 (Fig. 5).
2. The removed histogram areas per sub-histogram are memorized and the mean value is calculated at the end.
3. The merge process is repeated with the demand that the merging position has to be found where the removed areas are as close as possible to the mean value found under step 2.

Determination of all transitions from histogram

Contrary to [4] the transitions are not expressed in voltages, they are normalized to the ADC range. These transitions can be calculated from the merged histogram by:

$$CH_{Tot} = \sum_{j=1}^{2^n-1} H_j; \quad T_{norm}[k] = \frac{\sum_{j=1}^{k} H_j}{CH_{Tot}} \quad for \quad k = 1,2,...,(2^n - 1); \tag{6}$$

Calculation of the normalized error correction function ECF

The error correction function ECF is calculated by the formulas below:

$$Q_{norm} = \frac{1}{2^n} \quad with \quad n = number \quad of \quad bits; \tag{7}$$

$$T_{ideal\_norm}[k] = \sum_{j=1}^{k} Q_{norm} \quad for \quad k = 1,2,...,(2^n - 1); \tag{8}$$

$$ECF_{norm}[k] = T_{norm}[k] - T_{ideal\_norm}[k]; \tag{9}$$

Calibration

The onboard calibration is performed by a lookup table (LUT) as shown in Fig. 8. The LUT content has been derived by adding the formerly determined offset and gain error to the normalized ECF_{norm}. For each ADC output code, the difference to the ideal transform function is memorized in this LUT. The final correction has been performed by adding this value to the ADC raw data.

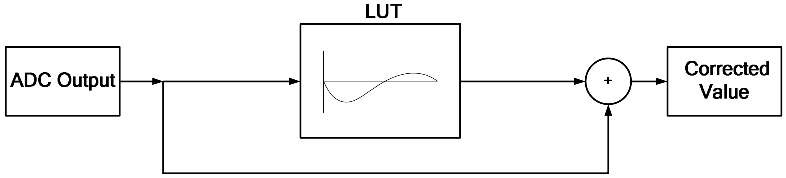

Fig. 8: Diagram of LUT correction

On existing AD-boards, without LUT correction capability, the offset and gain correction can be performed on the associated controller card. Further, a set of polynomial coefficients can be prepared to correct the INL by means of a processor.

V. Measurements and Results

The accurate determination of the static parameters has been confirmed for our widely used 16 bit ADC board (SPA499). The resulting distribution should be uniform because of the triangular stimulus. Deviations are caused by the DNL of the ADC. Some codes stick out but no missing codes, i.e. no zero counts, can be seen. Just like a fingerprint, the histogram patterns are unique and different for each AD converter. The lower part of Fig. 9 depicts the computed corresponding error correction function ECF; it shows a deviation of +/-16 ppm. For this ADC board, the acquisition and analysis of a single histogram takes about 40 minutes.

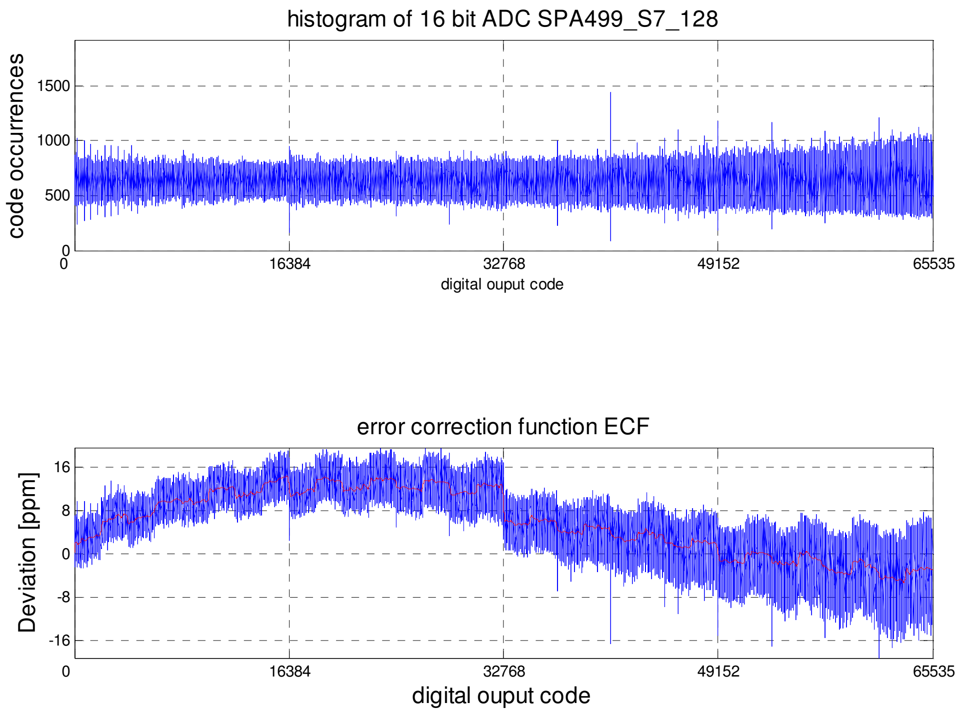

Fig. 9: Upper: histogram of a single calibration cycle; lower: corresponding error correction function ECF

Test series have been performed over 7 hours to show the stability of the equipment and the reproducibility of the results. The upper two pictures of Fig. 10 show the offset- and gain errors. The mean offset amounts to 5 ppm and the variation to about +/- 2 ppm. The mean gain error amounts to 148 ppm the variation is about +/- 1 ppm. Therefore, an improvement by a factor of more than 100 can be expected by calibration. The picture at the bottom shows the determined error correction function ECF which has been filtered to show the deviation over the full test series. The good reproducibility of this ECF allows improving the nonlinearity from +/- 10 ppm to +/- 2 ppm.

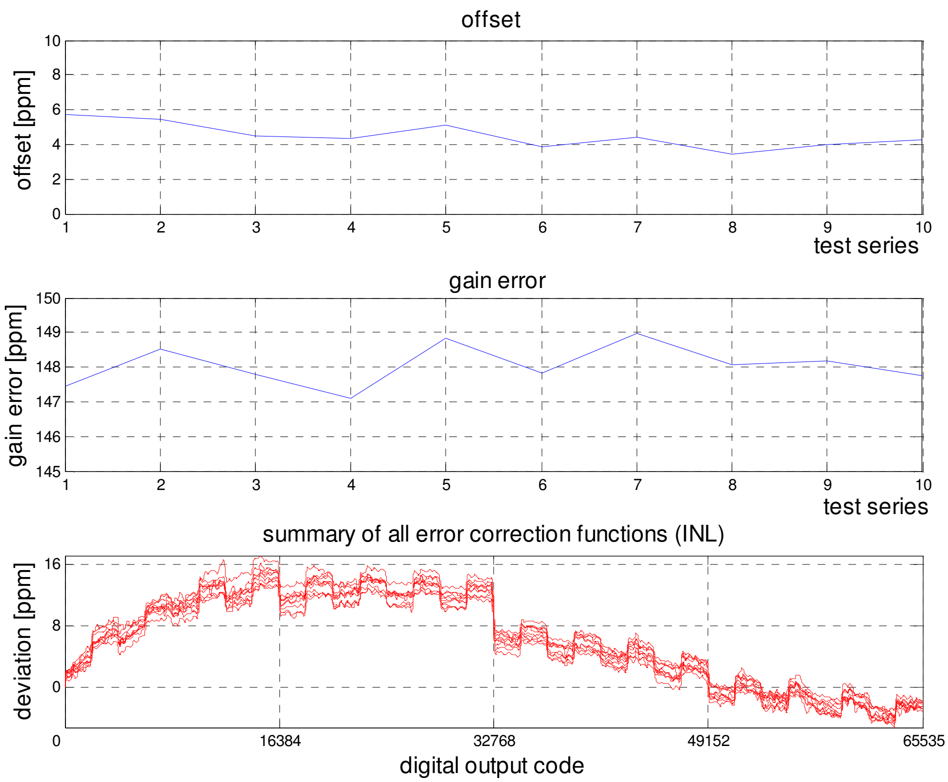

Fig. 10: Stability of the results of an ADC-analysis over 10 test cycles

VI. Conclusion

The presented AD analyzer and calibrator based on histogram technique is a very accurate and efficient method to characterize the static parameters of high resolution ADC. The test duration can be reduced by a factor of 50 and more [3] compared to the IEEE 1057/94 standard static test. It can be used for future AD converters with a resolution of up to 20 bits in spite of a moderate experimental burden. Currently, the equipment will be mainly used for the calibration of a newly designed 18 bit ADC board at PSI.

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