CERN VISIONS

Geneva, 3-4 April, 2014

LEP	→	web
LHC	→	grid-cloud
HL-LHC/FCC	→	??

EXASCALE: 10^{18} Flops

Processors : 10^9 =BILLION!!

Clock frequency: 10^9

Proposal: ***von-Neumann*** → ***NON-Neumann***

BIG-DATA

MASSIVELY PARALLEL

SCALABLE

Not UNIVERSAL

OPTIMIZED for SPECIFIC AIMs

Table 1: Nick Tredennick's Paradigm Classification Scheme

Early Historic Computers:	
	Programming Source
Resources fixed	none
Algorithms fixed	none
von Neumann Computer:	
	Programming Source
Resources fixed	none
Algorithms variable	Software (instruction streams)
Reconfigurable Computing Systems:	
	Programming Source
Resources variable	Configware (configuration)
Algorithms variable	Flowware (data streams)

Call for collaboration in project

E X A M S

(**EXA**scale computing for **M**ulti **S**cience)

Starting team in Budapest Technical University and Roland Eotvos University

Algorithmic and FPGA studies on:

Geant – X (each paricles has its own CPU)
Space-charge simulation in accelerators
Molecular docking, Lattice QCD, Astro-, Plazma-physics…etc

Proposed TIMETABLE

Bilateral communication by e-mail during April 2014 to create proto-collaboration

Proposal for ***kick-off meeting*** at CERN, Geneva 1st week of May 2014

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2013 International Conference on ReConFigurable Computing and FPGAs (ReConFig)

Keynote 1 - **Moore's Law, Programmable Logic and Reconfigurable Systems**

by Steve Trimberger, Xilinx Labs

Abstract

Moore's Law continues, but for how long?

Many are predicting the end, or at least the slowing, of semiconductor scaling even as FinFETs are being introduced. **New technologies**, such as 3D integration, offer new opportunities for silicon vendors and customers.

These technology trends are converging on **Programmable Logic**.

FPGA vendors are changing the way they build their products and those changes are being reflected in the **architecture and tools** that surround those products. These products enable new capabilities for **reconfigurable systems.**

This talk describes the technological pressures and opportunities for programmable logic vendors and highlights recent product trends and what they indicate for the future of programmable logic the future of reconfigurable systems built on it.

HORIZON 2020

FET-Proactive - towards exascale high performance computing
H2020-FETHPC-2014

Publication date *2013-12-11* *Deadline Date* *2014-11-25 17:00:00*

Specific challenge: The challenge is to achieve, by 2020, the full range of technological capabilities needed for delivering a broad spectrum of extreme scale HPC systems.

The designs of these systems need to respond to critical demands of energy efficiency, new delivery models, as well as to the requirements of new types of applications, including extreme-data applications.

New methodologies, environments and tools for extremely-parallel and data-intensive programming are needed to achieve code quality and portability, reduce software development and maintenance costs while maximally exploiting underlying system capabilities (e.g., exploiting millions of cores in an energy-aware way).

New mathematics and new algorithms are needed for ultra-scalable algorithms with predictable performance for existing or visionary applications, including data-intensive and extreme data applications in scientific areas such as physics, chemistry, biology, life sciences, materials, climate, geosciences, etc.

2013 International Conference on ReConFigurable Computing and FPGAs (ReConFig)

Keynote 3 – Extreme Scale Challenges: Can Reconfigurable Computing come to the rescue?

by Maya Gokhale, Lawrence Livermore National Laboratory

Abstract

The international High Performance Computing community has undertaken the challenge of extreme scale computing - breaking the exaflop barrier in the coming decade.

The EU, US, and Japan each have their unique approaches to building machines that can compute the largest scientific and data analysis problems imaginable, from cosmology to climate modeling to personal genomics.

However, these extreme scale aspirations are beset with extreme scale technology challenges which must be mitigated with solutions to power, data movement, concurrency, memory bandwidth, and heterogeneity.

These are familiar hurdles to the reconfigurable computing community, who routinely produce heroic solutions and demonstrate extreme scale performance at extremely low power, high concurrency, high memory bandwidth, and high heterogeneity.

Can reconfigurable computing tools and technology provide the answers HPC is seeking?