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The ABC130 ASIC Design for the ATLAS Silicon Strip Upgrade

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The ABC130 Front End ASIC for the ATLAS Silicon Strip upgrade has been designed and fabricated in IBM 130nm CMOS technology. It uses a binary architecture with fixed trigger latency, similar to that used in the current experiment, but the functionality is extended to support two readout mechanisms: one with low latency to support region of interest track trigger construction, and the other for full event readout. Key results will be shown, including first cross checks of the electronic gain and noise measured with silicon strips and first results from a fully populated detector hybrid

Summary

The 256 channel ABC130 Front-End ASIC has been designed for segmented strip detector readout, according to requirements for the ATLAS Silicon Strip upgrade, driven by the reduction of material. A fixed latency trigger ("L0") is used to tag the hit patterns that are stored internally for a maximum of 6.4us. L0 tagged hit data can subsequently be maintained on-chip in the large Random Access Memory (RAM) blocks for very long time (up to 256us in the present implementation) and then formatted and extracted, by receiving either a "Regional Readout Request (R3)"command, or a global "L1"trigger (which may be based upon the "R3"information). Hit data is formatted into fixed size 60-bit packets with complete stand-alone packet identification. The foreseen system architecture starts with the packets transmitted from chip to chip within the strip detector hybrids and then to the Hybrid Controller Chip (HCC), which interfaces to the GBT high speed link serializer.

The ABC130 circuit is designed to deliver the "R3"packets with priority over the "L1"packets. Other priority mechanisms are used to regulate packet flow and to insert status packets. In simulation, the system works with no loss of information with a L0 trigger rate at 1MHz and combined R3/L1 command rates at 200KHz, and a packet transmission rate of 160Mb/s.

A first batch of chips were affected by a bug regarding the polarity of an internal enable line, which prevented transmission of data by the bidirectional SLVS transceivers. A small number of die were corrected by Focused Ion Beam edit and mounted onto single chip PCBs, enabling the core functionality to be tested. Gain as measured by the internal calibration circuit was found to vary chip to chip between 80 and 100mV/fC with, at the higher end of the scale, noise levels of around 400 electrons with no load (600 electrons with a 2.5cm strip detector). Initial gain measurements from a second batch of fully corrected wafers are consistent with these values. It is expected that studies with external signal sources will confirm this variation to be a property of the calibration circuitry. Results with the first hybrid prototypes will be discussed. The full performance of the ABC130 chip is obtained with power consumption as low as 0.55mW per channel.

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