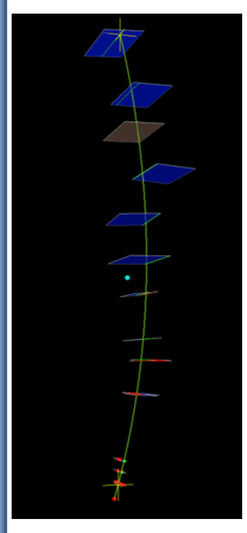
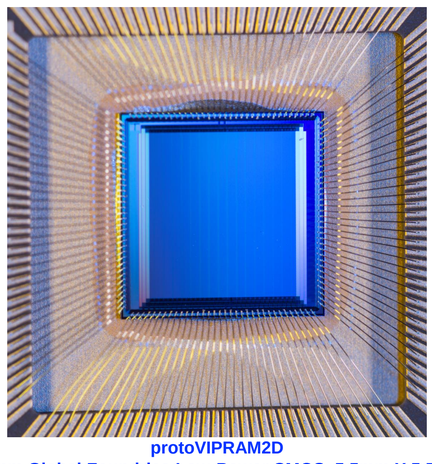
protoVIPRAM2D: Realization and Testing

T. Liu*, G. Deptuch, J. Hoff, S. Jindariani, S. Joshi, J. Olsen, N.Tran, M. Trimpl
Fermi National Accelerator Laboratory, P.O. BOX 500, Batavia, IL, 60510, USA



It has become clear that the development of a L1 tracking trigger will be required for CMS to maintain physics acceptances for basic objects (leptons, photons, jets and MET) in the HL-LHC era. However, a silicon-based L1 tracking trigger has never been realized at this scale and thus it is imperative that its feasibility be demonstrated before the design of the Phase-II Tracker can be finalized. Silicon-based Level-2 tracking trigger systems based on associative memory were successfully implemented in the past and are being actively explored at present. The higher occupancies anticipated at the HL-LHC and the low latencies required at L1 (about several μs for the track finding stage) present us with a formidable set of challenges that must be attacked with a well-organized R&D project.

Introduction



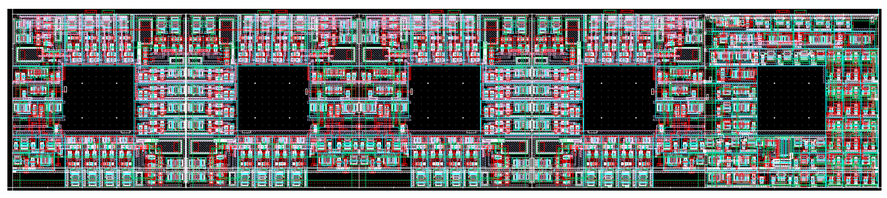
protoVIPRAM2D
130nm Global Foundries Low-Power CMOS 5.5mm X 5.5mm

The rigorous technical requirements of a silicon-based L1 tracking trigger must push the limits of Pattern Recognition Associative Memories (PRAM) in pattern density, speed and power. The VIPRAM (Vertically Integrated PRAM) approach is to divide the PRAM structure among 3D VLSI Tiers to reduce the area consumed by a single road pattern, to reduce the parasitic capacitance of long runs, to increase the effective number of routing layers dramatically and, finally, to increase the readout speed significantly. Since 3D Vertical Integration is an emerging technology and since the requirements of the L1 track trigger have themselves been evolving, the first logical step was to verify the building blocks thoroughly through a simple "2D" prototype run to guarantee their functionality in preparation for the 3D and L1 readout developments in the near future.

This poster presents the design, simulation and preliminary testing results of the first prototype of the Vertically Integrated Pattern Recognition Associative Memory (VIPRAM) concept.

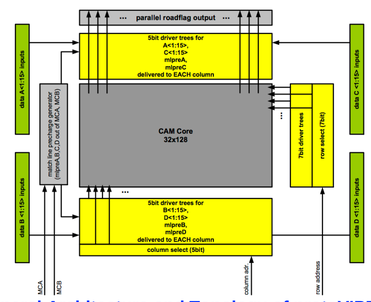
Prototype Design

The prototype chip has 4096 roads (patterns) distributed in 128 rows and 32 columns. Each road has 4 CAM cells and one Majority Logic/Flag Logic cell (Control cell) and performs complete pattern recognition for one 4 layer pattern. Each CAM in each road performs a layer-specific pattern recognition operation on incoming 15-bit data in a single clock cycle. The outputs from the 4 CAMs go the Control cell where threshold conditions are applied to determine the single roadFlag output per road. The 32 roadFlag outputs corresponding to all the columns of a particular, selected row on the chip are sent to the output pads. The eventRearm signal clears the matches when asserted.

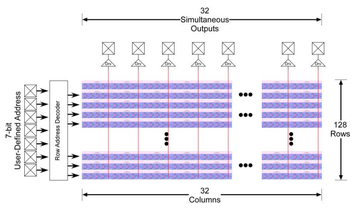


protoLeg layout 25um X 125um

To keep the design compatible with 3D implementation, space is left in the middle for Through Silicon Vias .

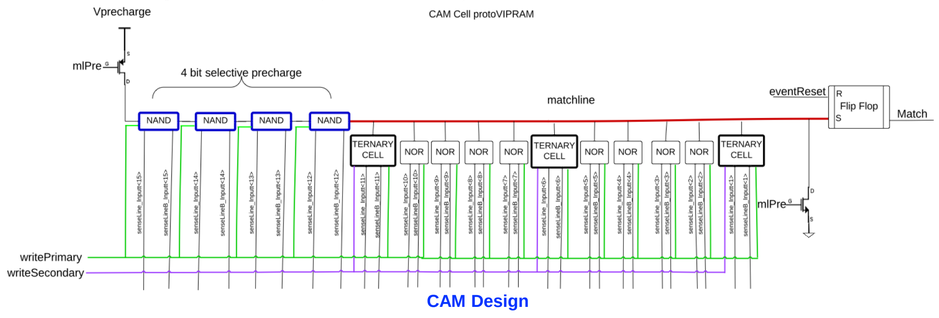


General Architecture and Topology of protoVIPRAM



Readout circuitry is kept simple to allow direct study of CAM and majority logic

The CAMs in the prototype are 15-bit wide including a 4-bit wide NAND-based Bank Selection circuit, 3 Ternary CAM Cells and 8 NOR Cells. The matchLine is pre-discharged each mlPre period, and its state is stored in an SR flipflop until reset by eventReset (eventRearm)



CAM Design

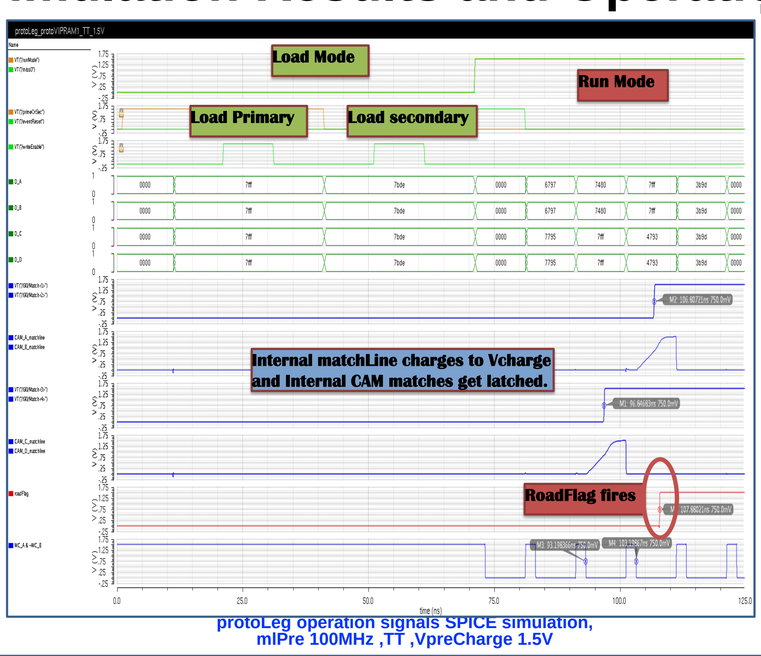
The matchLine connects the different bits in the CAM cell and its parasitic impedance dominates performance. Minimizing the matchLine increases the maximum clock frequency and minimizes power consumption for a given clock frequency. In the prototype the matchLine is shortened considerably by wrapping it in a square.

Simulation Results and Operation

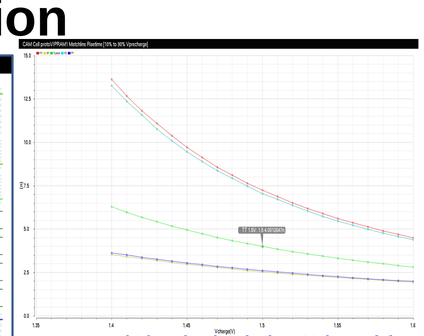
Corner analysis and Monte Carlo(MC) tests were done on all parts of the core and the periphery. Mixed signal simulations were done on the design using a Verilog data generator to test the CAM cells for varying Vcharge values. The AMS (Analog Mixed Signal) simulator was used in Cadence ADE XL to simulate the designs with connection rules for 1.5V logic.

The Chip works in two modes:
Load Mode: Patterns are stored in the CAMs with address [row:col].
Run Mode: Incoming data is compared to the stored patterns and roadFlag outputs are generated based on matches found and threshold conditions asserted.

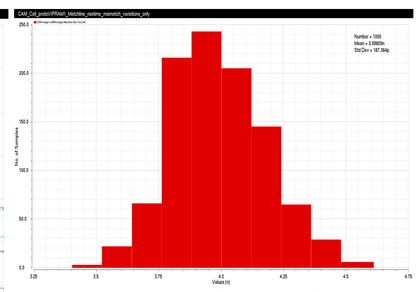
Critical delays measured:
1. Propagation delay(PD) from mlpre release to rising edge of stored match signal, 50% to 50% VDD.
2. Rise time(RT) of matchLine from 10% to 90% Vcharge.
3. PD of last CAM match signal and roadFlag output of control logic.



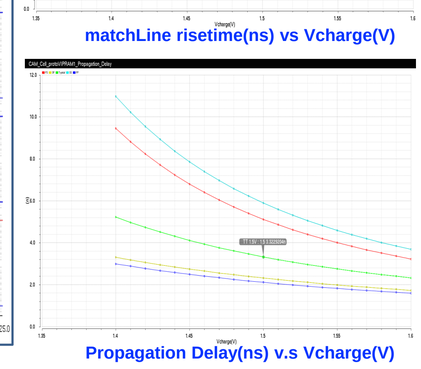
protoLeg operation signals SPICE simulation, mlPre 100MHz ,TT ,VpreCharge 1.5V



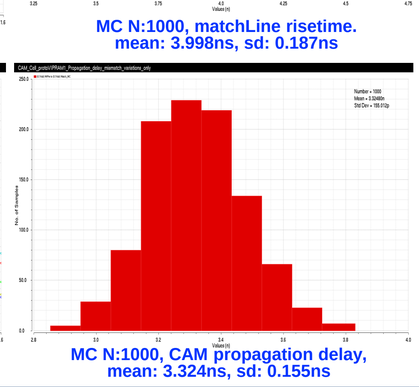
matchLine risetime(ns) vs Vcharge(V)



MC N:1000, matchLine risetime.
mean: 3.998ns, sd: 0.187ns



Propagation Delay(ns) v.s Vcharge(V)



MC N:1000, CAM propagation delay,
mean: 3.324ns, sd: 0.155ns

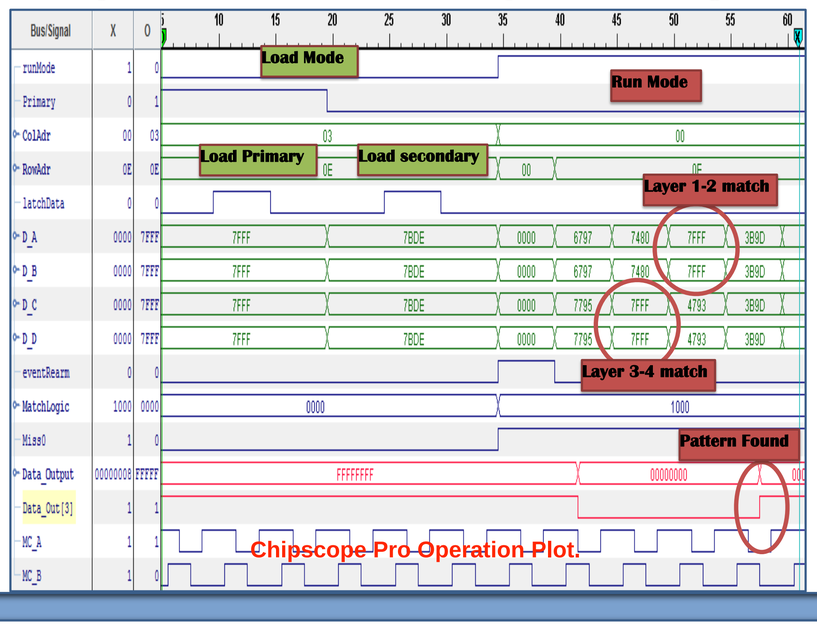
Testing setup and Preliminary Testing Results

"Pseudo-realistic" HL-LHC Test Conditions

The data was taken from the CMS Associative Memory simulation package. The input data contains hits (or Pt stubs) associated with tracks from hard scattering overlaid with 140 pileup interactions, with realistic hit occupancy for each tracker layer. Efficiency of pattern finding has been measured at different operating frequencies ranging from 50MHz to 143MHz.

Efficiency

It is observed that the chip operates with 100% efficiency (i.e. correctly finding all the patterns) up to a frequency of approximately 100MHz with decreased efficiency at higher speeds. This is consistent with the original 100MHz design goal.



Chipscope Pro Operation Plot.

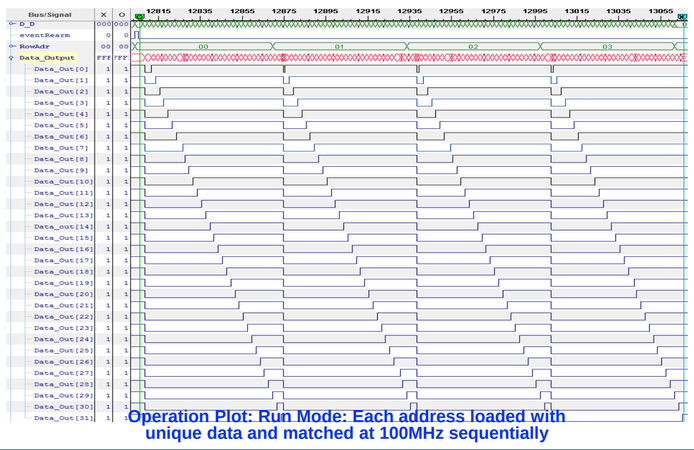
Power Consumption

The power consumption of the chip is being studied by probing current in the power supply lines.

- Line Drivers consume most of the power.
- Typical power consumption at 100MHz for pseudo-realistic patterns is 200-300mW
- Since this chip only contains 4K patterns, it is not easy to measure the power consumption directly related to the pattern matching operation. More detailed study is on going and the results will be reported in the future.
- Initial power and thermal analysis has been done for the design, and the details are described in another poster ("Thermal Analysis of the Proto-VIPRAM2D Chip" by Tao Zhang, Second Poster Session)

Search/ Run Mode

Rows 0-4, 100MHz, Vcharge 1.5V



Operation Plot: Run Mode: Each address loaded with unique data and matched at 100MHz sequentially

Summary

In summary, the first protoVIPRAM chip was designed and fabricated in a 130nm Low Power CMOS process. The layout was deliberately implemented such that the basic associative memory building blocks can be directly re-used for 3D stacking. The design has been thoroughly simulated at all levels and the prototype has been successfully tested both for functionality and performance using a custom test setup, with special test patterns as well as input hit patterns in "pseudo-realistic" HL-LHC conditions. The testing results show that the basic associative memory building blocks that comprise protoVIPRAM2D are ready for 3D vertical integration for proof-of-principle demonstration of the VIPRAM concept. In addition, the protoVIPRAM design can be used as a solid starting point for more improvements in the next version, a 2D design optimized for CMS L1 tracking trigger application.

References

[1] M. Dell'Orso and L. Ristori, "VLSI Structures for Track Finding," Proceedings in Nuclear Instruments and Methods, vol. A278, pp. 436-440, 1989.
[2]T. Liu, J. Hoff, G. Deptuch, R. Yarema, "A New Concept of Vertically Integrated Pattern Recognition Associative Memory", published in the Proceedings of the TIPP 2011 Conference, DOI number 10.1016/j.phpro.2012.02.521
[3] A. Annovi, et al, "Associative memory design for the fast track processor (FTK) at ATLAS, Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2011 IEEE Page(s): 141 – 146

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