Contribution ID: **136** Type: **Poster**

ProtoVIPRAM2D: Realization and Testing

Wednesday 24 September 2014 17:34 (1 minute)

The challenge of the Vertically Integrated Pattern Recognition Associative Memory (VIPRAM) Project is to increase pattern density through aggressive Vertical Integration. Our first step is to implement in conventional VLSI building blocks that can be used in 3D stacking. We are reporting on the first successful implementation of a conventional 2D demonstrator of the VIPRAM chip (protoVIPRAM2D). Detailed measurements achieved with a dedicated test card benchmark the design in terms of yield, speed and power consumption. Measurements are promising for Level 1 Tracking Trigger applications in LHC experiments. The results show that these building blocks are ready for 3D stacking.

Summary

An associative memory based track finding approach has been proposed for a Level 1 Tracking Trigger to cope with increased luminosity at LHC. The VIPRAM (Vertically Integrated Pattern Recognition Associative Memory) Project exploits emerging 3D Vertical Integration technology to build faster and denser Associative Memory devices.

From the beginning, our design methodology has been to develop concepts and circuitry in 2D to confirm functionality and then translate those ideas into 3D. The first step taken by the VIPRAM Project was the development of a 2D prototype (protoVIPRAM2D) in which the associative memory building blocks were designed with an eye toward future, aggressive Vertical Integration. In fact, the associative memory building blocks were laid out as if this was a 3D design. Room was left for as yet non-existent Through Silicon Vias and routing was performed to avoid these areas. To mimic a 3D approach the PRAM array was composed of patterns which were created from four identical CAM cells and a Control Cell resulting in the ability to recognize 4-layer road matches. The readout circuitry was deliberately simplified to allow direct performance studies of the CAM and Control cells. Any system interface including high-speed readout for Level 1 Tracking Trigger applications and architectural options made available by Vertical Integration are the subject of another abstract.

protoVIPRAM2D was designed and fabricated in a 130nm Low Power CMOS process that has been used previously in High-Energy Physics 3D designs. The layout was implemented such that in future designs all cells can be hosted on different 3D tiers and also extended in layer depth to enable more sophisticated tracking. The design has been thoroughly simulated at all levels and the prototype has been tested both for functionality and performance using a custom test setup. The design of the chip will be presented and detailed simulations dealing with timing, signal dispersion and power consumption will be shown. Measurement results obtained will be presented demonstrating full operation of the chip and fully mapping the CAM array with respect to yield and speed benchmarks. Dedicated power and thermal analysis of the chip as well as for 3D integration will be described in a separate abstract.

Given the success of protoVIPRAM2D, a broad spectrum of next steps is possible. This talk will clearly show that the building blocks that comprise protoVIPRAM2D are ready for vertical integration.

Authors: HOFF, Jim (Fermilab); TRIMPL, Marcel (Fermilab); LIU, Tiehui Ted (Fermi National Accelerator Lab. (US))

Co-authors: Dr DEPTUCH, Grzegorz (Fermi National Accelerator Lab. (US)); OLSEN, Jamieson (Fermilab); TRAN, Nhan Viet (Fermi National Accelerator Lab. (US)); JINDARIANI, Sergo (Fermi National Accelerator Lab. (US)); JOSHI, Siddhartha

Presenter: LIU, Tiehui Ted (Fermi National Accelerator Lab. (US))

Session Classification: Second Poster Session

Track Classification: Trigger