Science & Technology Facilities Council

www.stfc.ac.uk

Wafer Testing of ABC130 Readout ASIC

Jens Dopke (a), Greg Farquhar (b), Bruce Gallop (a), Peter W Phillips (a), Richard Shaw (c), Matt Warren (d)
(a) Particle Physics Department, STFC Rutherford Appleton Laboratory, Harwell Oxford, Chilton, Didcot, Oxon, UK, OX11 0QX
(b) Merton College, Oxford, UK, OX1 4JD
(c) Cavendish Laboratory, Department of Physics, University of Cambridge, Cambridge, UK
(d) Department of Physics and Astronomy, University College London, London, UK

Introduction

A new generation of the ATLAS Binary Chip (ABC) readout ASIC has been designed in the IBM 130nm CMOS 8RF process to support ongoing R&D towards the ATLAS Tracker Strip Upgrade. There are two variants of the ABC130 chip, one having an additional Fast Cluster Finder (FCF) block to facilitate studies of self-seeded trigger mechanisms.

The initial batch of wafers, received in November 2013, was found to have a design error in the bi-directional SLVS transceiver blocks. Several chips were corrected by Focused Ion Beam (FIB), which verified the origin of the fault and enabled initial testing to proceed.

In June 2014 further wafers were received in which the error had been corrected. So that faulty chips may be excluded from the build process, a comprehensive functional test sequence has been developed. All five wafers from this batch have been probed, and one has been diced and distributed to the community for further study.

Hardware and Software

The wafers were probed on a Micromanipulator Model 4460 Semiautomatic Test Station. Whilst supplied as an 8” machine, in the original chuck all vacuum grooves were confined in a 4” circle. In this configuration our thinned 8” wafers were found to bow up outside the central region: a custom top plate with additional vacuum rings was manufactured in order to eliminate this effect.

Fig. 1: Probe Station (screened cables help reduce electrical noise).

The epoxy-ring probe card was made to our specification by Probe Test Solutions Limited (PTSL). Some bond pads are present only on FCF die: these needles are omitted such that both ABC130 variants may be tested with the same probe card.

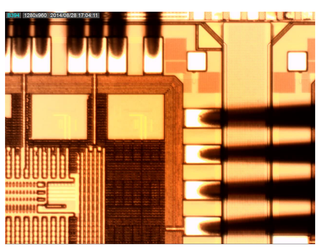

Fig. 2: Probe to Die Contact.

SLAC’s High Speed I/O (HSIO) board, running custom firmware, is used as a readout platform. The interface between HSIO and the device under test (DUT) is provided by a custom driver board based on a Xilinx Spartan-3A FPGA. The driver provides level translation and buffering of fast signals between ABC130 and HSIO; it probes various monitor points by means of ADCs; and it drives the chip’s static control nodes (addresses etc) by means of registers implemented within the Spartan chip.

Software is based on the existing SCTDAQ package used to test the previous ATLAS Strip FE chips. New code facilitates automated control of the probe station, a different model having been used to probe previous chips, and implements a thorough test sequence for the ABC130. The GUI has been redesigned to assist on-wafer testing and to produce pick maps for dicing.

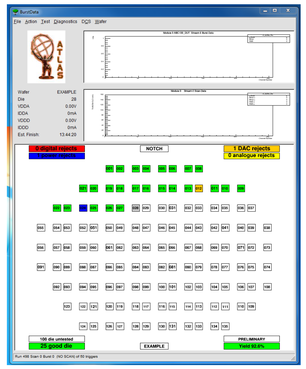

Fig. 3: SCTDAQ ABC130 Wafer GUI.

Test Methodology

The test sequence has four stages: power tests, DAC characterisation, digital tests, and analogue characterisation. The FCF block is not tested here.

Power tests: This test ensures that the DUT may be configured and that the analogue and digital currents drawn are correct.. Additionally, the ABC130’s shunt regulator functionality is tested to verify the chip may operate successfully as part of a serially powered system.

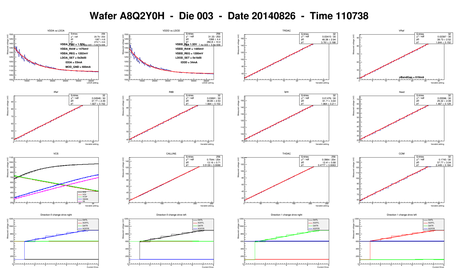

Fig. 4: Typical DAC Characterisation Result

DAC characterisation: The ABC130 contains many DACs. ADCs on the driver board record the output of each DAC over a range of the possible values to confirm proper behaviour.

Digital tests: Test vector blocks engineered to test the digital functionality of the chip are passed to the DUT. Returned data is compared to anticipated references. The test vectors include reading/writing registers, reading chip addresses, passing data through in both directions, reception of simulated flow control signals as expected from neighbouring chips, and using the priority control functionality.

Analogue characterisation: A three point gain test injects charges of 0.5, 1.0, and 1.5 fC across a range of thresholds to assess basic analogue behaviour. An additional threshold scan at 1.5 fC is carried out after adjustment of the trim DACs to verify that all channels may be trimmed.

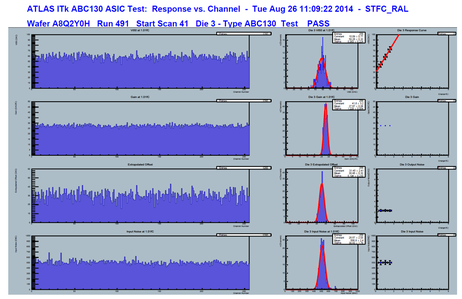

Fig. 5: Typical Three Point Gain Result

Results

Die are classified as rejects if they fail power or digital tests, or have significant analogue defects. A-grade die pass all tests successfully. B-grade die have up to 2 bad or noisy channels, or exhibit slightly anomalous DAC behaviour, but may still be useful during the R&D phase of the project. The die are additionally classified as type “0” or “1”. This information is incorporated into the pick map such that the dicing vendor may respect the four useful streams.

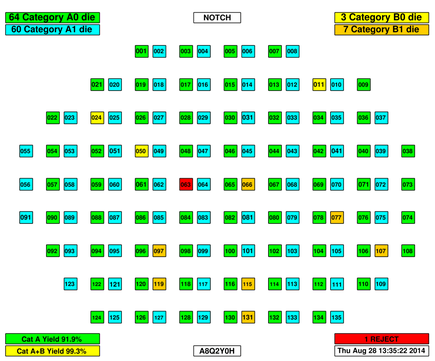

Fig. 6: Pick Map of the wafer with Highest Yield.

	Cat A Yield	Cat A+B Yield
A5Q2XLH	90.4%	99.3%
A8Q2Y0H	91.9%	99.3%
A6Q2XKH	84.4%	95.6%
AYQ2XTH	77.0%	94.1%
AQQ30GH	89.6%	97.8%
Net	**86.7%**	**97.2%**

Fig. 7: Summary of ABC130 Yield.

The gain measured (28-30 DAC counts/fC) is slightly lower than that predicted by simulation. In the context of the wafer probing results a significant contribution to this comes from the use of the same FE settings for all chips of a wafer: It is expected that optimisation of these values shall reduce the spread and increase the mean. Maps of test properties reveal significant variations, both within and between wafers.

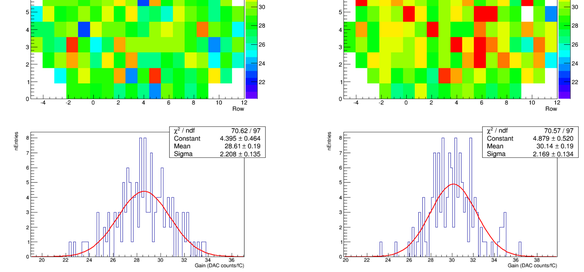

Fig. 8: Gain maps of two wafers.

Diced chips have been wire-bonded to single-chip test boards, where their behaviour has closely matched on-wafer testing.

Conclusions

Over 675 tested die, the net yield of A-grade die was 86.7%, with only 2.8% rejected outright. After minor setup, the testing process may be fully automated and without further optimisation takes approximately 8-9 hours per wafer.

References

The ABC130 ASIC for the ATLAS Silicon Strip Upgrade, F Anghinolfi et al, TWEPP 2014

ATLAS

UNIVERSITY OF OXFORD

UNIVERSITY OF CAMBRIDGE

UCL