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Development of a FEI4 Wafer Level Stress Compensation Layer for Improvement of Thin Pixel Modules 3D Assembly

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Low mass pixel modules are developed for reducing radiation length in CERN LHC atlas system upgrade consisting of a silicon sensor flip-chipped with micro-bumps to a FEI4 read-out integrated chip. Thinning the FEI4 chips to 100 µm results in increasing chip bow leading to co-planarity issues during flip-chip reflow process. We demonstrate that chip deformation can be dynamically compensated adding an appropriate layer onto the wafer back-side. Working with thermo-mechanical models and experimental trials of deposited stacks we are able reducing the bow magnitude by a factor of 3 over the temperature range.

Summary

The pixel modules are the fundamental building blocks of the atlas pixel detector system used in CERN LHC facility. They consist in their basic form of a silicon sensor that is flip-chipped bonded to a CMOS read-out integrated chip (ROIC), the FEI4 chip. One of the main objectives for the ATLAS experiment is to develop an approach towards low mass modules and thus reducing radiation length. From the module perspective this can be achieved by using advanced 3D technology processes that includes the formation of copper and solder micro-bumps on top of the ROIC front-side, the thinning of both the sensor and the CMOS ROIC and finally the flip chip assembly of the 2 chips. The thinning of the silicon chips can lead to low bump connections yield at the solder reflow stage due to bad co-planarity of the two chips and hence poor device resolution. In the case of the large FEI4 ROIC chip (20x19 mm2), which is thinned to 100um, the chip bow varies from - 100 µm at room temperature to + 175 µm at reflow temperature resulting of CTE mismatch between materials in the CMOS stack and the silicon substrate. Our objective is to compensate dynamically the stress of the front side stack by adding a compensating layer to the back-side of the wafer. Utilising our material thermo-mechanical database coupled with a proprietary analytical simulator and measuring the bow of the ROIC at die level we are able to reduce the bow magnitude by approximately a factor of 3 by the introduction of the compensating layer. We show that it is possible to change the sign of the bow at room temperature after deposition of a SiN/Al:Si layer stack at die or wafer level. This amplitude of the correction can be manipulated by the deposition conditions of the SiN/Al:Si stack. Further development of the backside deposition conditions are on-going where the target is to control the room temperature bow close to zero and reducing the bow magnitude through the full solder reflow temperature range hence conserving bump yield and device resolution. In keeping with a 3D process the materials used are compatible with Through Silicon Via (TSV) technology with a TSV last approach in mind should we integrate this technology in the future on FIE4 chips but also on next generation ROIC thanks to the simulations.

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