Secondary Particle Acquisition System for the CERN Beam Wire Scanners Upgrade

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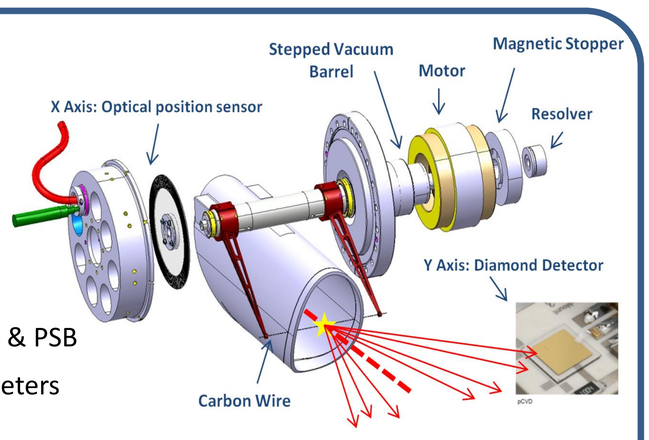
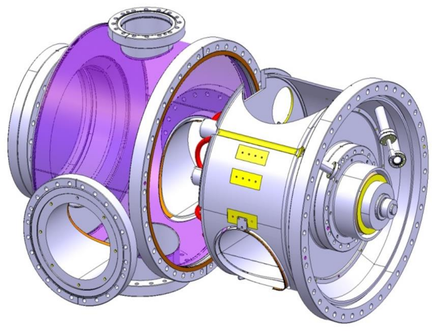
Abstract: *A secondary particle shower acquisition system is under design for the new CERN wire scanner-based beam profile monitors. In these systems a thin wire passes through a circulating beam and the resulting secondary particles are detected to reconstruct the beam profile. It is proposed that the new acquisition system be based on a polycrystalline diamond detector (pCVD). The accompanying electronics should exploit the high dynamic of such detector, with digitization near the detector and optical transmission to the signal processing electronics on the surface. In addition the signal chain must be capable of 40 MHz bunch by bunch measurements.*

Motivation:

- Beam Wire Scanners Upgrade
- New detector used (pCVD)
- High dynamic range needed
- Low noise measurements
- One single system for LHC, SPS, PS & PSB
- Avoid the need of tuneable parameters

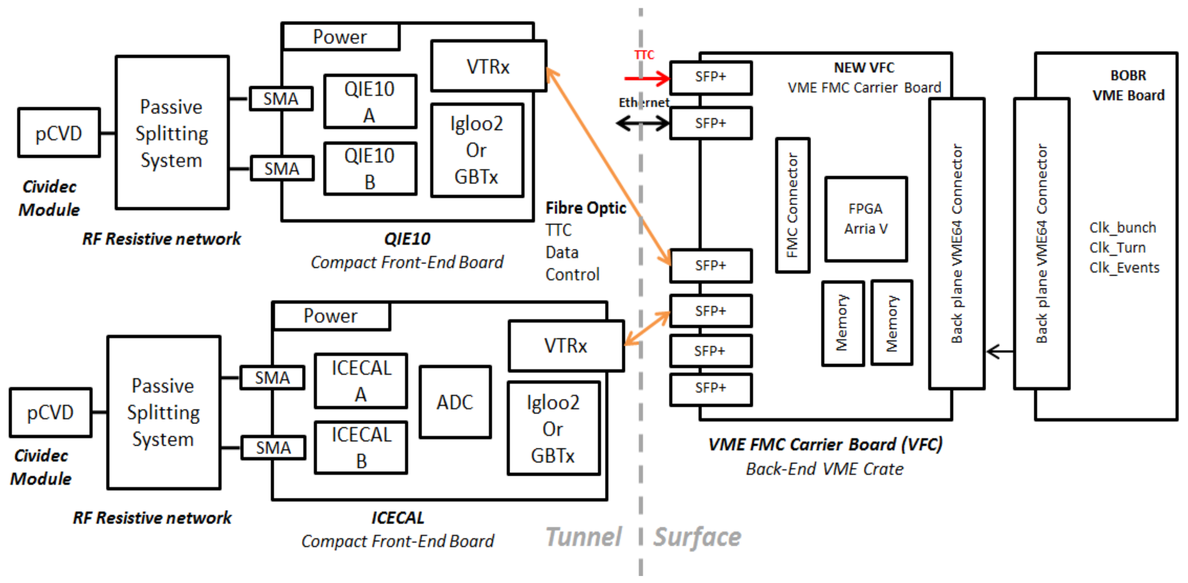


SYSTEM REQUIREMENTS	
Dynamic Range	1.6fC – 1.6nC (1e6)
Integration Window	25ns (40Mhz)
Synchronization	LHC & SPS: Bunch by Bunch
	PS & PSB: Turn by turn
Link Distance	up to 250m
Ionizing Radiation	100Gy/year



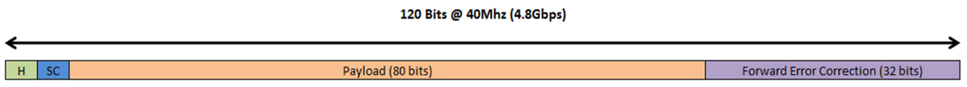
Proposed System Architecture Overview:

The Analog Front-End will be placed near the detector to avoid long coaxial cables and maintain the pCVD signal dynamics and quality. Once digitalized by one of the two possible Front-End architectures, the digital data will be sent through a GBT optical link @ 4.8Gbps, this link provides data transmission, control and synchronization. The Back-End solution envisaged is based on the new VFC board developed by the CERN's BE-BI group.



Optical link with GBT Protocol @ 4.8Gbps on Igloo2 :

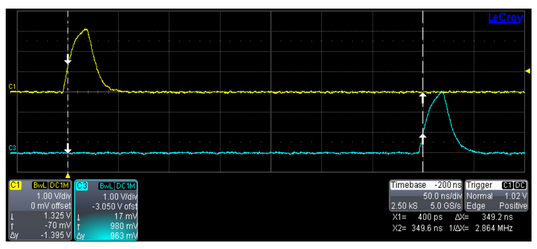
Two alternative solutions are studied for the optical link: The use of the Rad-Hard **GBTx** ASIC developed at CERN, and the **GBT-on-Igloo2** project (an implementation of the GBT protocol on a Flash-Based Igloo2 FPGA from Microsemi). We developed this second option due GBTx unavailability at the moment and for the promising results on igloo2 irradiation tests. The Versatile Link Transceiver (**VTRx**) module will be used for the optical interface. The GBT protocol was selected for the communication between Front-End & Back-End. GBT frames consists on 120bits each 25ns from which 80 bits are payload and 32 bit forward error correction. For the Igloo2 implementation, **GBT-FPGA** code was modified and made available for other users.

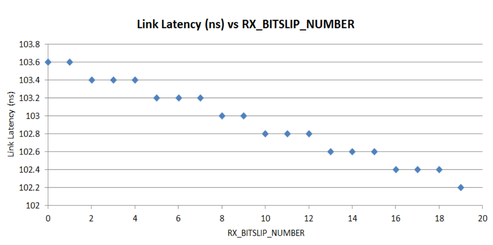


• LHC & SPS bunch-crossing clock recovery in front-end:

The Front-End acquisition system must be synchronous with the beam to provide bunch by bunch capability, therefore it's very important to synchronize Front-End & Back-End systems with deterministic latency. The optical link is synchronous respect to the LHC or SPS 40MHz bunch crossing clock. For synchronization, clock-recovery and alignment techniques are used to maintain a low latency variation and recovered clock phase. The performance tests shown the following results:

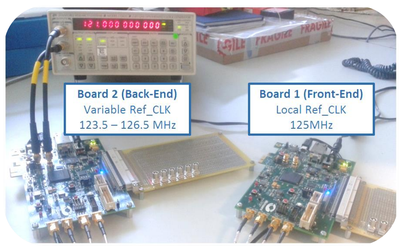
Link Latency Uncertainty: ± 0.7 ns **Recovered Clock Phase Uncertainty:** ± 2.8 %





• Link stability during accelerators ramp:

The system must maintain it's stability during the accelerator's ramp for acquisitions. During this period, the frequency and phase of the bunch-crossing clock will vary slightly and the link synchronization must be kept. In this architecture the front-end will run with a local oscillator (120Mhz) for it's SERDES, while the back-end with 3x LHC or SPS clock. A preliminary test was performed to study the link stability versus the reference clocks difference to assure the operation during the ramp.



Ref Frequency Tolerance Test on Igloo2 with GBT firmware implemented @ 5Gbps

Diff Freq (Mhz)	Board 1 Freq (Mhz)	RX_Locked	RX_Val	GBT_Error_Counter	Comments	Board 2 Freq(Mhz)	RX_Locked	RX_Val	GBT_Error_Counter	Comments
-1.5	125	No	No	Increments	RX_Freq remains constant and stable respect B2 TX_Freq	123.5	No	No	Increments	RX_Freq remains constant and stable respect B1 TX_Freq
-1.25	125	No	Sometimes	Increments	Received frames look like spected but with errors	123.75	No	Sometimes	Increments	Received frames look like spected but with errors
-1	125	Sometimes	Yes	No errors	GBT Frames well received and no error observed	124	Sometimes	Yes	No errors	GBT Frames well received and no error observed
-0.75	125	Sometimes	Yes	No errors	GBT Frames well received and no error observed	124.25	Sometimes	Yes	No errors	GBT Frames well received and no error observed
-0.5	125	Yes	Yes	No errors	GBT Frames well received and no error observed	124.5	Yes	Yes	No errors	GBT Frames well received and no error observed
-0.25	125	Yes	Yes	No errors	GBT Frames well received and no error observed	124.75	Yes	Yes	No errors	GBT Frames well received and no error observed
0	125	Yes	Yes	No errors	GBT Frames well received and no error observed	125	Yes	Yes	No errors	GBT Frames well received and no error observed
0.25	125	Yes	Yes	No errors	GBT Frames well received and no error observed	125.25	Yes	Yes	No errors	GBT Frames well received and no error observed
0.5	125	Yes	Yes	No errors	GBT Frames well received and no error observed	125.5	Yes	Yes	No errors	GBT Frames well received and no error observed
0.75	125	Sometimes	Yes	No errors	GBT Frames well received and no error observed	125.75	Sometimes	Yes	No errors	GBT Frames well received and no error observed
1	125	Sometimes	Yes	No errors	GBT Frames well received and no error observed	126	Sometimes	Yes	No errors	GBT Frames well received and no error observed
1.25	125	Sometimes	Yes	No errors	GBT Frames well received and no error observed	126.25	Sometimes	Yes	Increments	Received frames look like spected but with errors
1.5	125	No	No	Increments	RX_Freq remains constant and stable respect B2 TX_Freq	126.5	No	No	Increments	RX_Freq remains constant and stable respect B1 TX_Freq

Impossible
Caution!
OK

CDR (Mhz): (125.5 - 124.5) = 1Mhz --> 8000 ppm
LHC Frequency Variation(Mhz): (400.789 - 400.790) = 1Khz --> 2.5ppm
SPS Bunch Spacing Variation(ns): (24.97 - 24.95) = 0.02ns --> 800 ppm

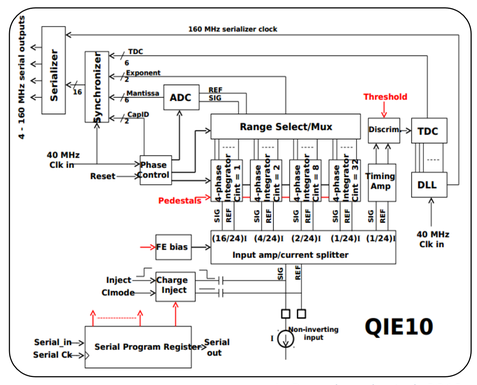
pCVD Readout ASICs:

- QIE10 & ICECAL ASICs compatible with our application.
- Dynamic range coverage by splitting the pCVD signal
- Two Front-End possibilities/prototypes to evaluate.
- Each Front-End will acquire two pCVD channels.
- Both ASICs are Rad-Hard developments for high energy physics.

ASICs SPECIFICATIONS		
	QIE10	ICECAL
Dynamic Range	3.2fC – 340pC (1e5)	4fC – 16pC (4e3)
Integration Window	25ns (40Mhz)	25ns (40Mhz)
Channels per ASIC	1	4
Input Impedance	50 Ω	
Dead-timeless	Yes	
Number of Bits	8	12 (ADC dependent)
Quantification Error	~ 1%	<< 1% (ADC Dependent)
Linearity Error	~ 1% (Logaritmic)	< 1%
TDC Capability	Yes	No
Radiation Resistance (TID)	~ 0.5KGy *	*
ASIC Technology	AMS SiGe BiCMOS 0.35µm	
Designer Entity	Fermilab for CMS/ATLAS	U.Barcelona for LHCb

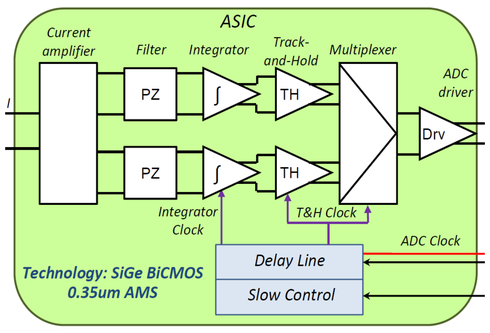
*This topic was under study when this poster was published

QIE10 SCHEME



A. Baumbaugh et al. 2013

ICECAL SCHEME

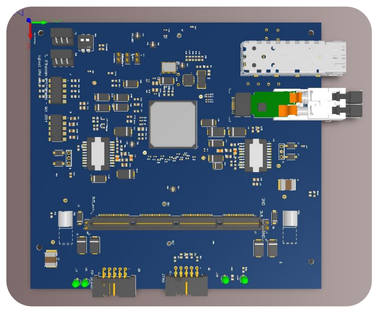


Picture kindly provided by E.Picatoste

Front-End Prototypes:

igloo2 UMd mezzanine:

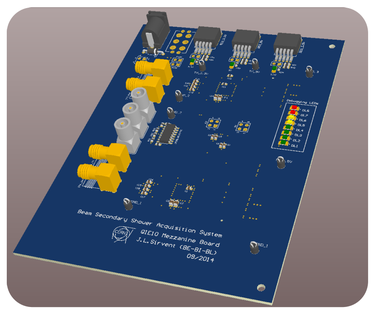
CMS development for the HF calorimeters upgrade. Designed as mezzanine for ngCCM prototype. This board contains the VTRx and will be programmed to emulate the GBTx ASIC.



* Board under development by Tullio Grassi & Tom O'Baron

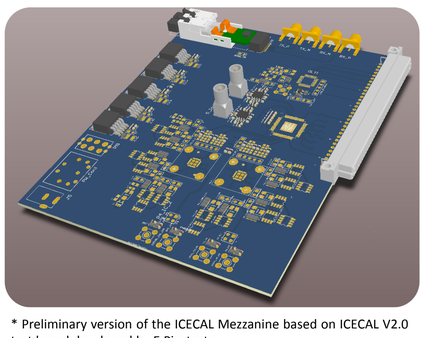
QIE10 Mezzanine:

Will contain 2xQIE10P5+1xDELAY25 for clock tuning. Developed to be connected with igloo2 UMd mezzanine as a sandwich through it's high speed Samtec connector.



ICECAL Mezzanine:

Aims to evaluate the performance of ICECALV2.0 (a pre-production version), where some conditioning is needed. The board contains two channels with a RH ADC. Samtec connector to be added.



* Preliminary version of the ICECAL Mezzanine based on ICECAL V2.0 test board developed by E.Picatoste.

References:

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- E.Picatoste, D.Gascon et al. *"Low noise front end ICECAL ASIC for the upgrade of the LHCb calorimeter"*. TWEPP11. Viena, Austria. September 2011.
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- J.L. Sirvent. *"Position Sensors and Secondary particle shower acquisition for the new CERN BWS"*. 9th DITANET Topical Workshop on Non-Invasive Beam Size Measurements for High Brightness Proton and Heavy Ion Accelerators, 15-18 April 2013. CERN, Geneve (Switzerland)

Conclusions:

A new architecture for the secondary particles acquisition system for the beam wire scanners upgrade has been presented, this is based on Front-End/Back-end approach with optical communication for data transmission and synchronization. The optical link based on the Igloo2 FPGA has been developed and characterized. The possible readout electronics will be evaluated soon and the proof-of-concept evaluation of the system is about to start once the prototype boards be ready.

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