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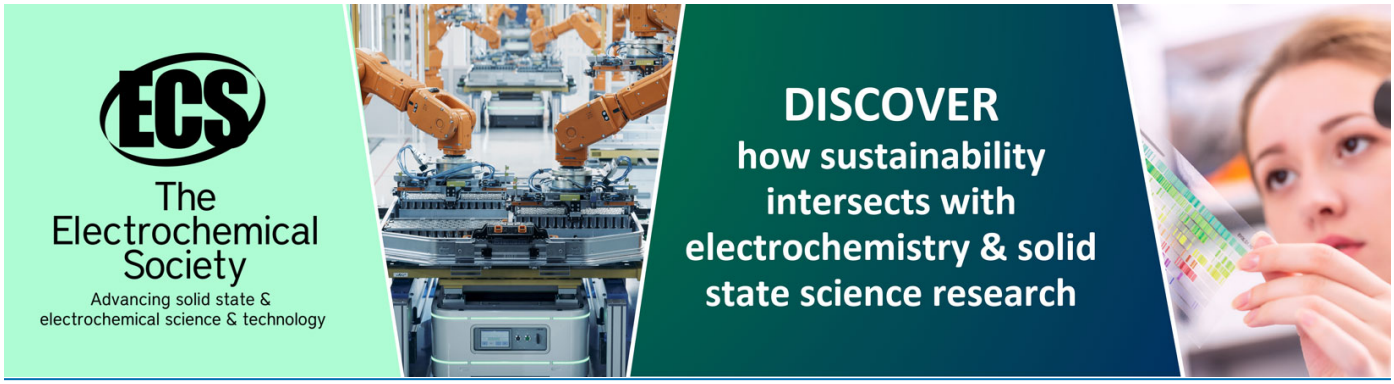

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Low noise 4-channel front end ASIC with on-chip DLL for the upgrade of the LHCb Calorimeter

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ABSTRACT: An integrated circuit for the Upgrade of the LHCb Calorimeter front end electronics is presented. It includes four analog channels, a Delay Locked Loop (DLL) for signal phase synchronization for all channels and an SPI communication protocol based interface. The analog circuit is based on two fully differential interleaved channels with a switched integrator to avoid dead time and it incorporates dedicated solutions to achieve low noise, linearity and spill-over specifications. The included DLL is capable of shifting the phase of the LHC clock (25 ns) in steps of 1 ns. The selected technology is AMS SiGe BiCMOS 0.35 um.

KEYWORDS: Calorimeters; Instrumentation for particle accelerators and storage rings - high energy (linear accelerators, synchrotrons)

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1 The LHCb upgrade

LHCb is one of the four large experiments of the Large Hadron Collider (LHC) located at the CERN laboratory near Geneva [1]. The fields of research of the collaboration are CP violation, charm physics and rare decays of the B meson. More than $3\,\mathrm{fb}^{-1}$ have been recorded since the LHC start-up. The data quality permitted to make important measurements.

However, the upgrade of the LHCb detector is being prepared in order to improve the precision of the measurements in major areas of flavor physics [2]. The upgrade is foreseen to be performed during the shutdown of 2018 and should permit to increase the instantaneous luminosity up to $2 \times 10^{33}\,\mathrm{cm}^{-1}\mathrm{s}^{-1}$. The most important modification will be the reading of the whole detector at 40 MHz, the LHC interaction rate, and consequently the suppression of the trigger hardware level so-called L0. In the new scheme each sub-detector will send its data at 40 MHz to the computer farm on which the software trigger will be running. Estimations of the impact of the software trigger show that the event yield will be more than doubled in B meson hadronic decays.

The calorimeter of LHCb, like the other sub-detectors, will adapt its electronics (common to the electromagnetic and hadronic calorimeters) to the new running conditions of the upgrade. Consequently, a new front-end electronics and a full revision of the electronics architecture is under development.

1.1 Calorimeter analog electronics upgrade motivation

The analogue signal processing in the present ECAL Front End (FE) board ([1, 3, 4]) consists in the integration of a photomultiplier pulse, which has been clipped and transmitted through a 12 m 50 Ω coaxial cable to the FE. The PMT is located at the back of the modules of the detector and the FE board is located in the crates on the calorimeter platform. The clipping line in the PMT base is used in order to reduce the signal tail and spill over. The discharge of the integrator is achieved by delaying the signal and subtracting it at the same integrator.

In order to keep the same average current after the increase in luminosity, that is, to reduce the PMT aging in the upgrade conditions, the gain has to be reduced by a factor 5 with respect to the present operation high voltage value. Therefore, the preamplifier input equivalent noise must be decreased accordingly so that output noise is at the level of 1 LSB (or an equivalent noise charge less than 4 fC). As a result, a 50 Ω termination resistor is not acceptable. An ASIC approach is adopted for this project to cope with integration constraints and a transistor based design required for an active termination scheme.

As the calorimeter measurement must be performed at every bunch crossing (at 40 MHz), the system has to reduce any spill-over effect and the PMT pulses have to be shaped so that the tail extending after 25 ns is not larger than 1% of the signal (table 1 specifies the main requirements on the upgraded FE electronics).

Table 1. Summary of the requirements for the calorimeter analog Front-End.

Requirements	
Energy range	$0 \leq E_t \leq 10$ GeV (ECAL)
Calibration/Resolution	4 fC/2.5 MeV per ADC count
Dynamic range	4096-256 = 3840 cnts: 12 bits
Noise	$\lesssim 1$ ADC cnt (ENC < 4 fC)
Termination	$50 \pm 5\,\Omega$
Baseline shift prevention	Dynamic pedestal subtraction
Max. peak current	4-5 mA over 50 Ω
Spill-over residue level	$\leq 1\%$
Linearity	$< 1\%$
Cross-talk	$< 0.5\%$
Timing	Individual (per channel)

1.2 Line termination and noise

An electronically cooled termination is the solution proposed and implemented in the present ASIC as opposed to the more common termination resistor. The selected implementation is achieved with an active circuit with controlled impedance.

Right after digitization, dynamic pedestal subtraction is performed. It consists on subtracting the smaller of the two previous samples. Hence, it is a type of Correlated Double Sampling (CDS), needed to cancel baseline fluctuation and low frequency (LF) pick-up noise. It has proven to be

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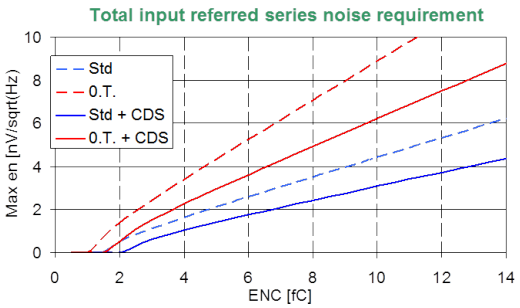

Figure 1. Series noise requirement for different amplifier and signal processing configurations. Parallel noise contribution is neglected.

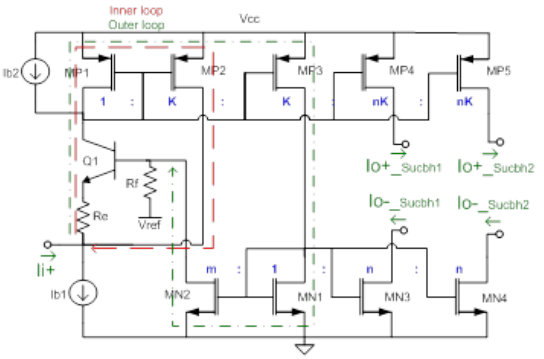

Figure 2. Simplified schematic of the input stage.

crucial for accurate operation, but it increases the noise in the signal bandwidth, ideally by a factor $\sqrt{2}$ provided both samples are not correlated.

The effect of the noise for an active termination and a resistor can be checked in figure 1, in which is represented the maximum allowed series input referred noise e_n requirement for the amplifier as a function of the required equivalent noise charge (ENC). Considering the specified ENC of less than 4 fC, the noise requirement for a cable terminating amplifier is $2.25\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$, whereas the one for the high input impedance voltage amplifier is $1\,\mathrm{nV}/\sqrt{\mathrm{Hz}}$ [5]. Therefore, an active impedance termination offers more room for design, while the requirement of the resistor termination is too stringent.

2 ASIC design

The presented implementation of the ASIC, ICECALv3, includes (figure 3): four analog channels with programmable values to control the key parameters and compensate for process variations; a dedicated Delay Locked Loop (DLL) to synchronize each channel signal phase and a digital interface using SPI protocol.

The design of this chip prototype is also determined by the radiation environment. The design must tolerate SEUs, SETs and SELs. The probability of SELs is reduced by increasing the distance between PMOS and NMOS transistors and inserting double guard rings between them. SEUs are avoided by implementing Triple Modular Redundancy Registers and a fault tolerant Finite State Machine in the SPI Slave. Finally, reset signals are protected from SETs by means of glitch suppressors.

The prototype has been designed in Austriamicrosystems 0.35 um SiGe BiCMOS technology, with 3.3 V power supply.

2.1 Analog channel

The proposed analog processing implementation in an ASIC is shown in figure 3. Due to the difficulty of integrating high quality delay lines, a switched solution is selected as it provides a way of reseting the integrator and avoid dead time. Two alternated switched signal paths (or sub-channels)

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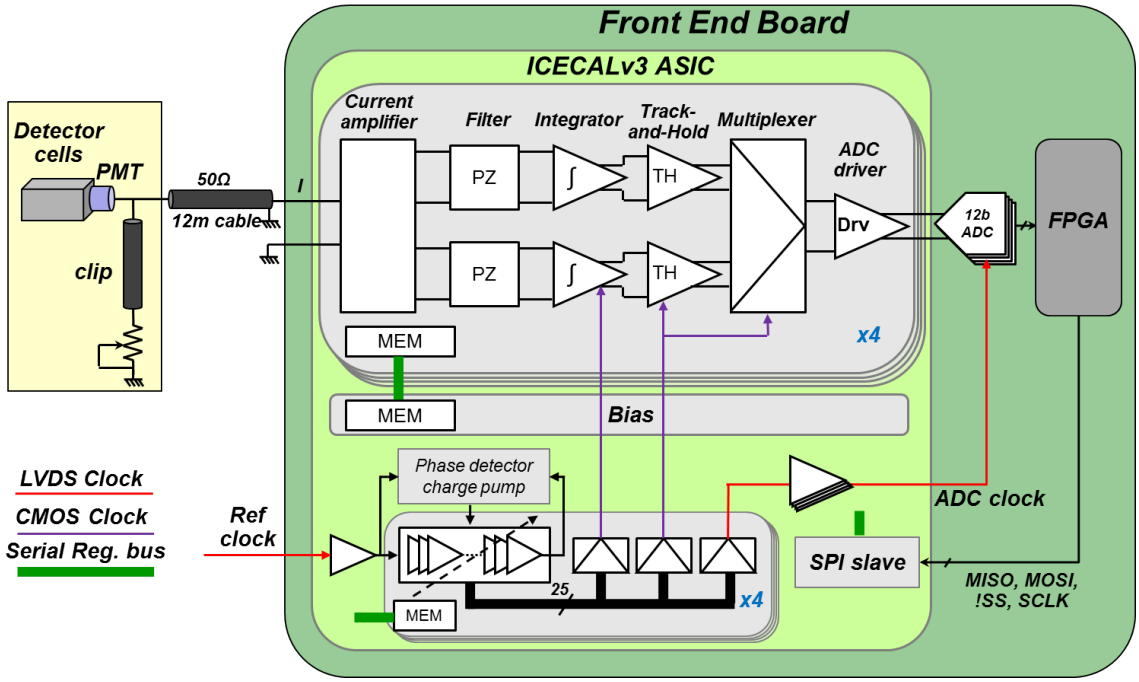

Figure 3. ASIC scheme.

are used to integrate and sample the input current pulses, a scheme successfully implemented in the LHCb Preshower front end ASIC [1].

The analog channel is designed with an input amplifier that includes an electronically cooled termination input stage with double feedback. A passive line termination would induce a too large noise and is avoided. The input current is initially amplified and converted to differential signaling. In a switched system it is very convenient to go as soon as possible to differential configuration in order to reject the common mode noise. Afterwards an alternated switched differential signal paths scheme permits the integration of the signal with no dead time between consecutive events. Each path includes a pole-zero filter in order to compensate for cable effects, a switched integrator with capacitive feedback, a Track-and-Hold for a 12-bit ADC and a MUX to select the correct sub-channel output signal.

2.1.1 Current amplifier input stage

The input amplifier is made of a "super common base" input stage with double feedback and it presents an electronically cooled termination. The two current feedback loops (figure 2) are used to decrease and control the input impedance of a common base transistor with emitter degeneration and provide additional transconductance linearization.

The current mode implementation has several advantages with respect to previous designs [7]: low voltage, DC coupling (no external components or additional pads), all nodes have low impedance (less prone to pick up noise), and ESD robustness is improved (no MOS transistor gate or bipolar base is connected to the input pad).

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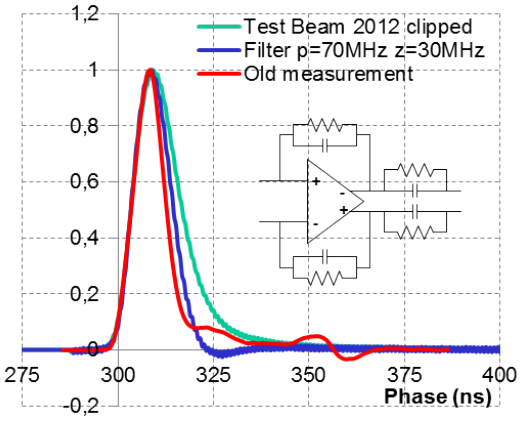

Figure 4. Input signals.

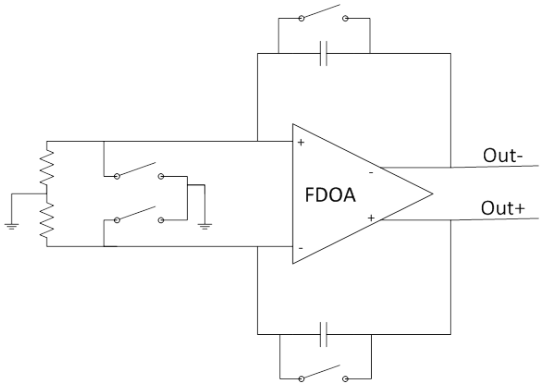

Figure 5. Simplified schematic of the switched integrator.

2.1.2 Pole zero filter stage

There are two specifications that are affected by the shape of the pulse signal. First, the difference in the integrator output should be less than 1% for ± 2 ns (usually referred to as plateau) so the energy from particles with different time of arrival to the detector is measured correctly. Second, the integrated signal on previous and next clock cycles should be less than 1% of the main signal.The part of the signal included in other clock cycles is known as spill over.

A test beam in 2012 showed that the pulse signal presented a longer tail than an old measurement used as the reference due to the long cable effect. As a consequence the plateau and the spill over requirements were not fulfilled. Therefore, a filter stage was designed to cope with the cable effects. A single pole and a single zero can help reducing the long exponential decay of the pulse. Figure 4 plots the old measurement, the one obtained in the 2012 test beam, and the simulation of the pole zero filter.

The pole and zero are obtained with resistors in parallel to variable capacitors that let the user adjust for different signals and compensate for fabrication process. It is even possible to compensate the signal without the clipping at the PMT bases, but with a worse and fixed spill over that could be compensated easily in the digital domain.

2.1.3 Switched integrator

Integration is performed by a fully differential amplifier with capacitive feedback. Since no dead time is allowed, each sub-channel carries out the integration while the other is in reset every 25 ns. CMOS switches are used with a 50 ns cycle clock to carry out both integration and the Track-and-Hold functionalities. The variations in gain are compensated with an adjustable capacitor at the integrator using 5 bits.

An analog multiplexer selects the valid sub-channel output and an output buffer at the end to match the 12-bit ADC input impedance.

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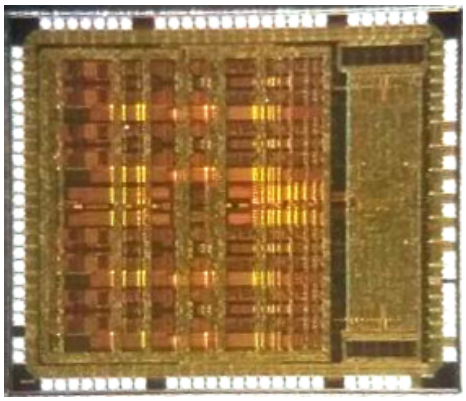

Figure 6. Micro-photograph of the ICECALv3 ASIC prototype.

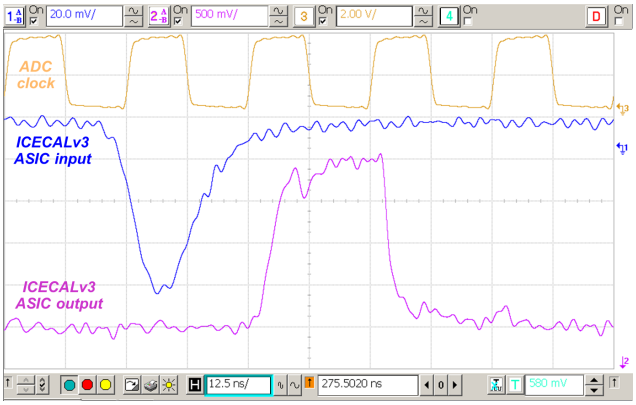

Figure 7. Oscilogram with input and output signals.

2.2 Delay line

Each analog channel includes a delay line based on a DLL [6] so the user can set a delay to compensate the delay introduced by PMT voltage settings, cable lengths or particle time of flight from the interaction point to the calorimeter cells. The present design offers a dedicated line to set the clock phase for the integrator, Track-and-Hold and the external ADC.

The DLL is adjusted by means of two control voltages to ensure that systematic process or environmental variations will not affect the channel time tuning. A fully differential design of the DLL aims at reducing the switching noise produced by delay lines. The clock jitter induced by transient noise is lower than 4 ps.

3 Measurements

3.1 Prototype set up

The test setup is based on a FE board prototype with connectors to a chip dedicated mezzanine and USB to PC communication port. All the data acquisition process is controlled by means of the FE FPGA and the custom software. The signal is replicated from the test beam measurements by an arbitrary function generator synchronized and triggerd by the FE prototype.

3.2 Time alignment

One of the challenges of the detector is to synchronize the data acquisition at the different electronic levels. This is also true inside the FE prototype. First, the clock input to the chip has to be adjusted in order to capture correctly the sub-channel reset. Second, as commented before, the signal has to be integrated at different times for different channels due to PMT high voltage and signal cable length differences, which is taken care by a dedicated internal phase. Third, the sampling time of the ADC will vary due to the board design and the integration time. And fourth, the FPGA will capture the data from the ADC. A dedicated software script ensures, step by step, that all synchronization levels are fulfilled.

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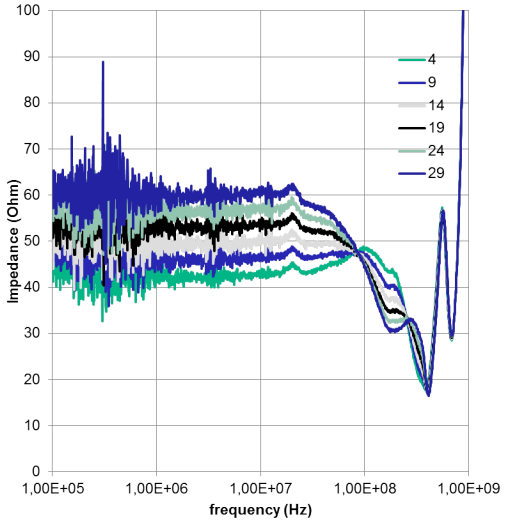

Figure 8. Input impedance for different programmed values (5 bits).

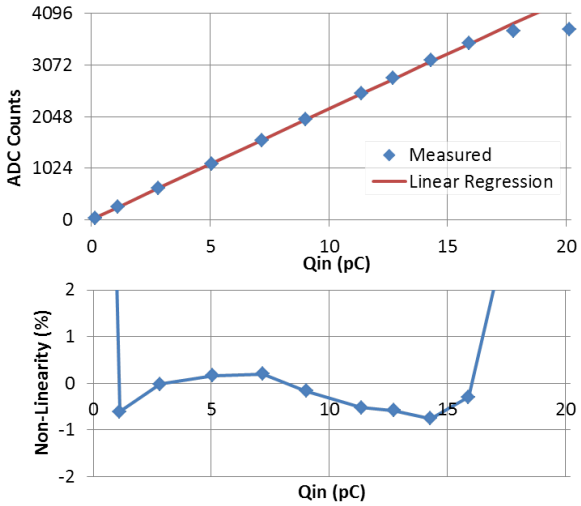

Figure 9. Non-linearity as a function of the input charge.

3.3 Results

Input impedance for different configurations was measured (figure 8) with a network analyzer at the input (Rohde&Schwarz ZVL) with approximate results due to not-optimal connectivity. Ranging approximately form 40 to 60 Ω, the optimum termination impedance corresponds to 14 DAC counts.

As presented in table 1, the expected sensitivity (inverse of gain) is 4.5 fC/LSB. It is possible to adjust the channel gain through the integrator capacitor. The results for all channels are plotted in the histogram in figure 13. The deviation from the value is lower than 2.5%.

Non-linearity has been checked to be $< 1\%$ for the full output range (figure 9). Using the offset stage, designed to add controllable offset levels to the positive and negative pins, it is possible to avoid a limit on the excursion of the Track-and-Hold stage which affects linearity for the higher signal levels. Linearity measurements at low signal values are affected by a large relative error due to the measurements setup noise.

Other important checks include the spill over. In order to have all the signal inside the 25 ns time window, a clipping is added at the PMT base. But, as the long cable to the FE widens the signal pulse, the pole zero stage is adjusted to minimize the output in the previous and next clock cycles, as shown in figure 11. As specified, the spill over is less than 1%, except for the second next clock cycle, which can be up to 2% in some cases.

As commented int section 2.1.2, the ASIC is expected to integrate signals from particles arriving with at different times (± 2 ns) without varying the output more than 1%. This plateau is also affected by the values of the pole and zero. An example of the plateau is shown in figure 10. Most of the plateau values are over 4 ns wide except for a few (less than 10% of the total) which are always more than 3.8 ns. The results in plateau and spill over are a trade-off; obtaining better results in one implies a worsening on the other.

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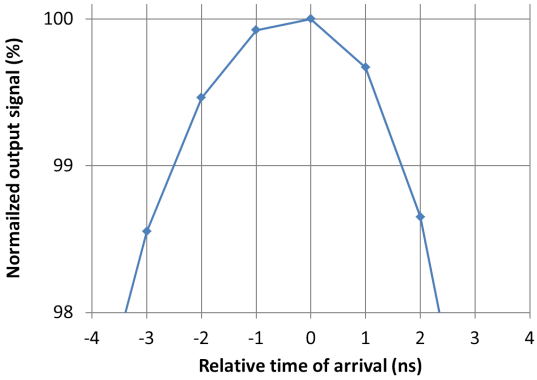

Figure 10. Plateau.

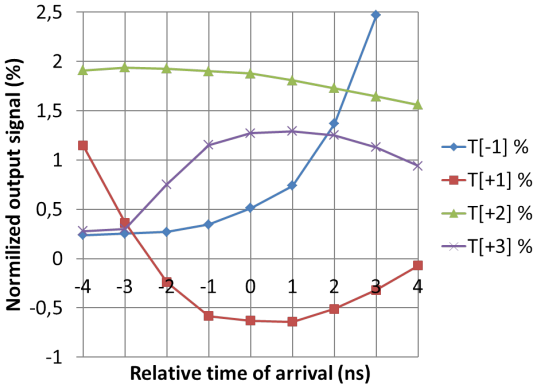

Figure 11. Spill over in the previous and next clock cycles.

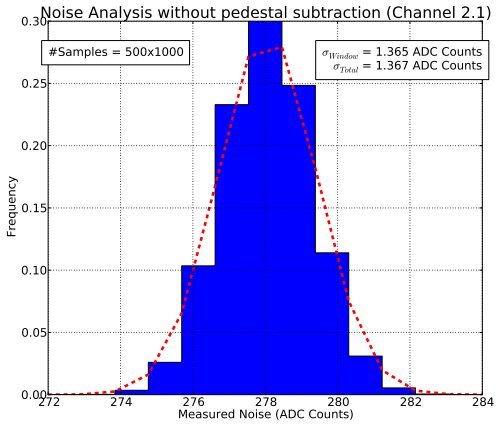

Figure 12. Noise example from a channel.

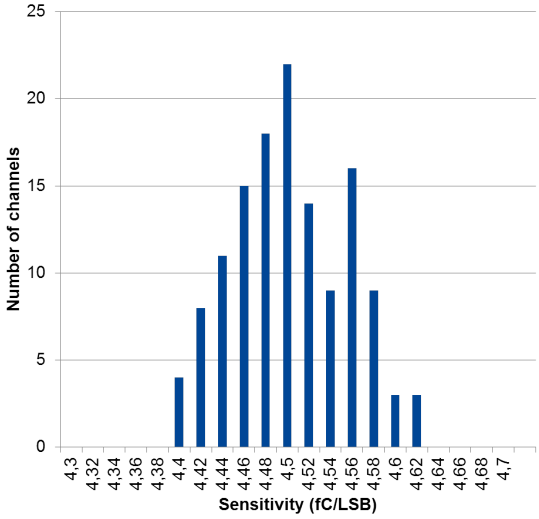

Figure 13. Sensitivity example for one channel.

The output noise of the ASIC depends of the configuration of the different parameters, mainly gain, offset and pole-zero. With the present configuration, the noise is in average 1.38 ± 0.13 ADC counts and 1.70 ± 0.18 ADC counts with pedestal subtraction. The specification states that it should be not greater than 1 ADC count. But this condition can be relaxed, as the noise should be less than the 5 ADC counts expected for the pile up noise.

4 Conclusions

An integrated circuit for the LHCb Calorimeter electronics upgrade has been presented. It includes 4 analog channels, on-chip delay lines for synchronization and an SPI digital interface to configure it. As it has been reported by the measurements performed, the requirements of the analog channel are met. However, more tests are considered to check the performance of the chip in irradiation tests. Even more, the ICECALv3 displays all the functionalities needed to be a good baseline

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solution not just for the analog electronics of the LHCb Calorimeter upgrade, but it could also be useful for many applications with PMT signal and a 40 MHz clock source due to its adjustable parameters, from which gain and pole zero stand out.

Acknowledgments

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