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Low Noise 4-channel Front End ASIC with On-Chip DLL for the Upgrade of the LHCb Calorimeter

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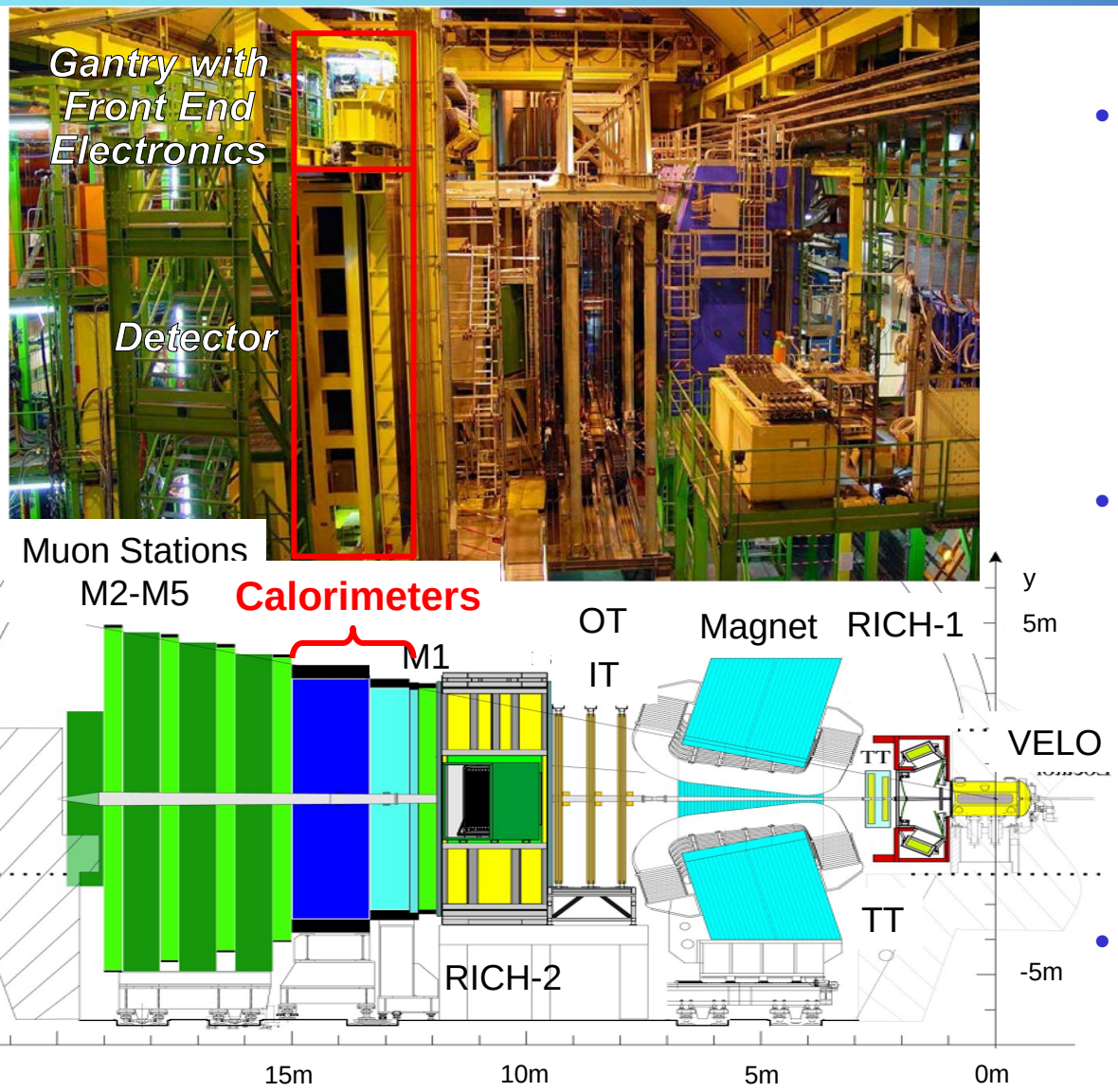
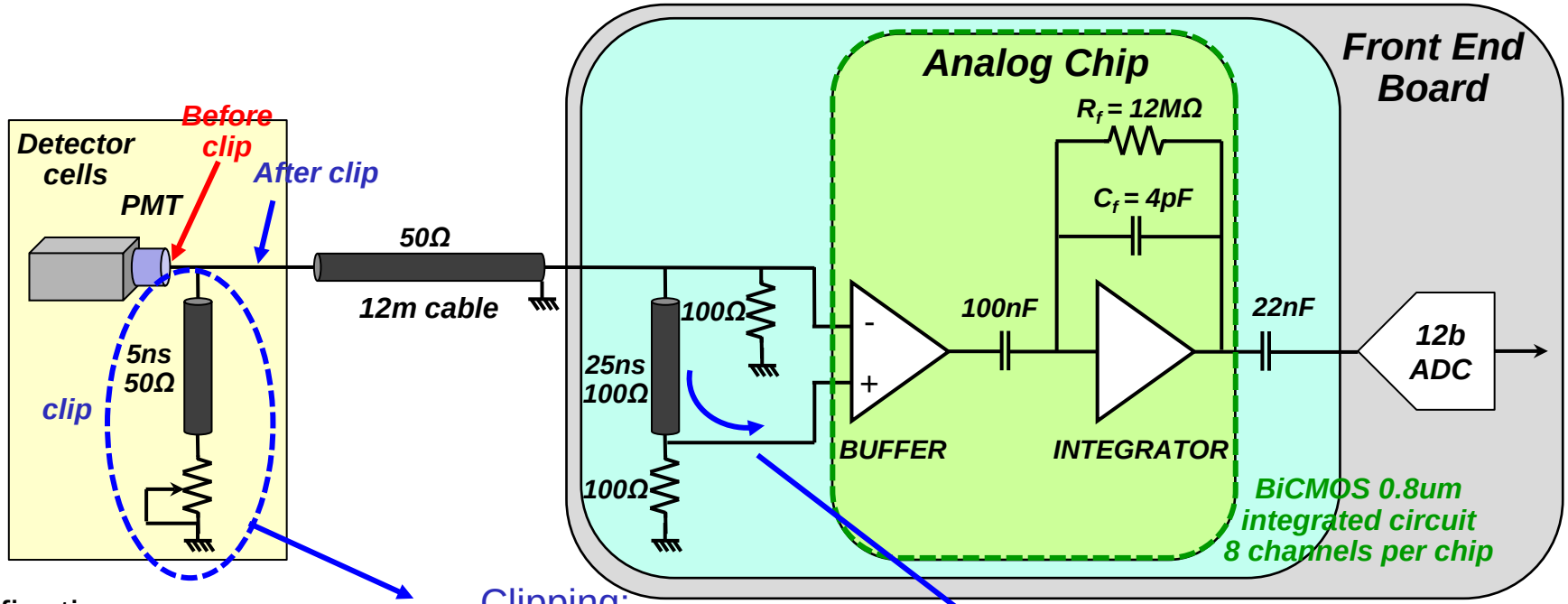
LHCb Upgrade



- Statistical improvement if:
  - Increase of data rate from 1 to 5fb^{-1}/year
  - Increase luminosity to 2x10^{33} cm^{-2}s^{-1}
  - Increase trigger efficiencies
- Current L0 trigger limited by electronics ⇒upgrade:
  - Trigger in software from 1 to 40 MHz
  - Use data from every bunch crossing
  - Upgrade electronics and DAQ
- Scheduled for the long LHC shutdown in 2018.

Current Analog Signal Processing



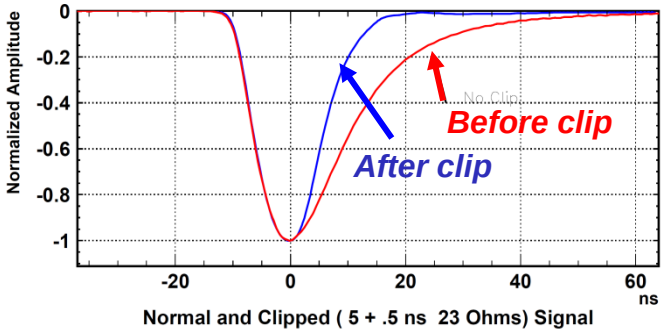
Specifications:

- Pulse shaping in 25ns
- Spill over < 1% after 25ns
- Integrator plateau: 4ns
- Linearity < 1%
- Rise time ~ 5 ns

Clipping:

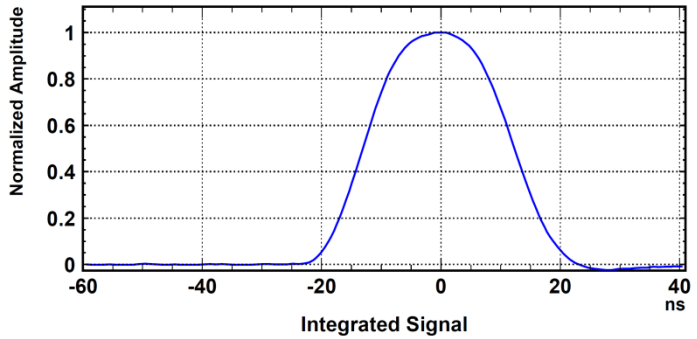
⇒ Reduce signal tail

⇒ Reduce spill over

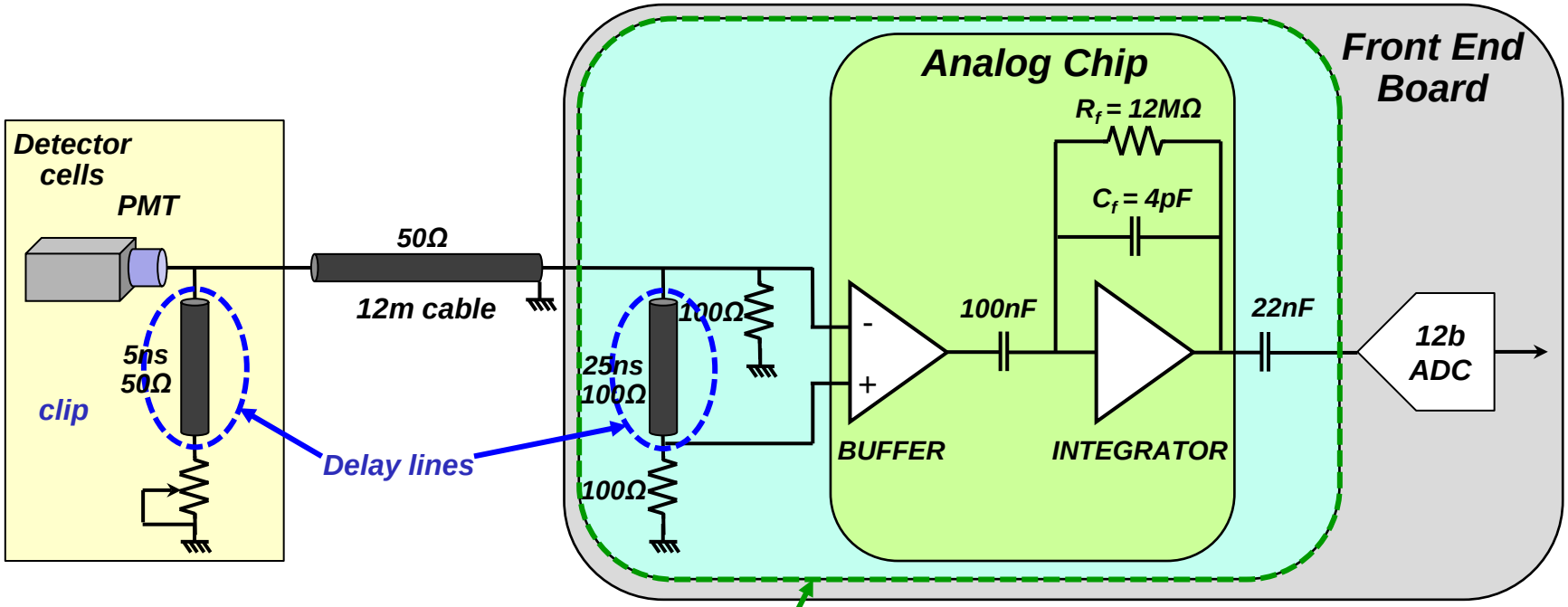


Integrator discharge:

Clipped signal + delayed negative clipped signal



Analog Electronics Upgrade Motivation



PMT current has to be reduced to increase lifetime

⇒ FE electronics gain has to be increased correspondingly

– BUT FE noise should not be increased in the operation!

Proposed solution:

– New ASIC
  - ✓ Increased gain
  - ✓ Reduced noise
  - ✓ Integration / shaping

Radiation tolerance:

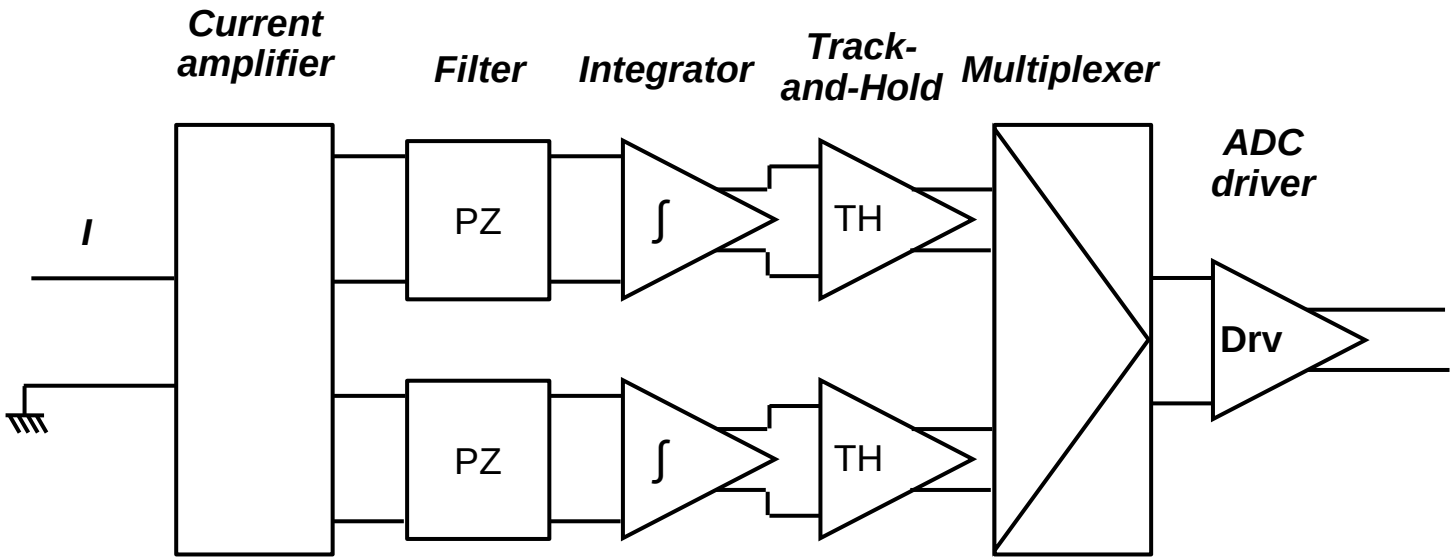
– Dose 100 rad per fb^{-1}

✓ Radiation qualification tests

✓ Design techniques on ASIC

→ Enclosed transistors with guard rings

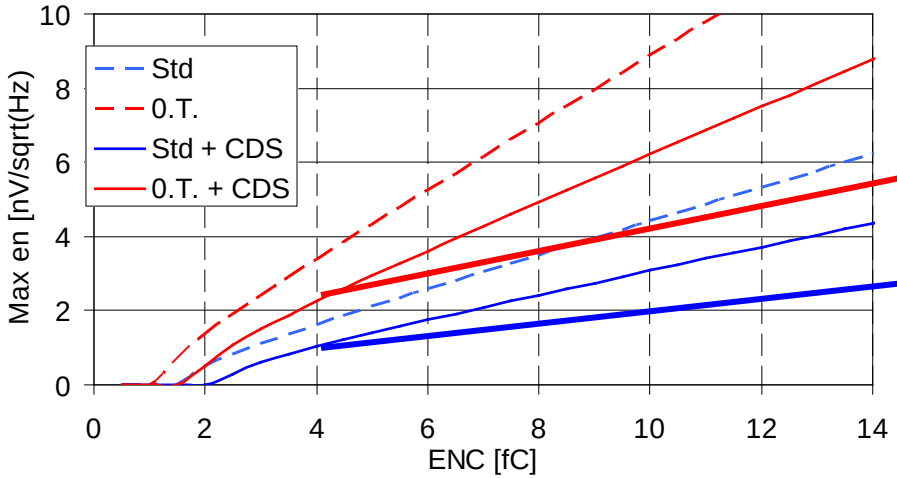
Analog channel signal processing and design



- Very difficult to integrate HQ analog delay lines
- 2 switched alternated paths as in PS/SPD (LHCb Calorimeter)
- Go fully differential to reduce the effect of the switching noise

Analog Signal Processing

Total input referred series noise requirement



Specification:

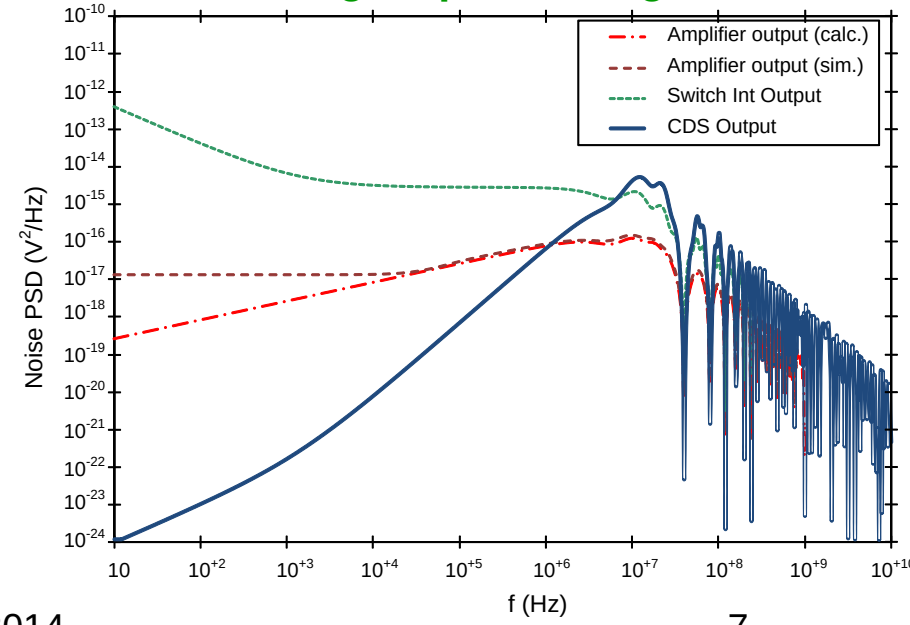
Noise ~≤ 1LSB or ENC < 4fC

Electronically cooled amplifier with e_n< 2 nV/√Hz fulfils requirements,

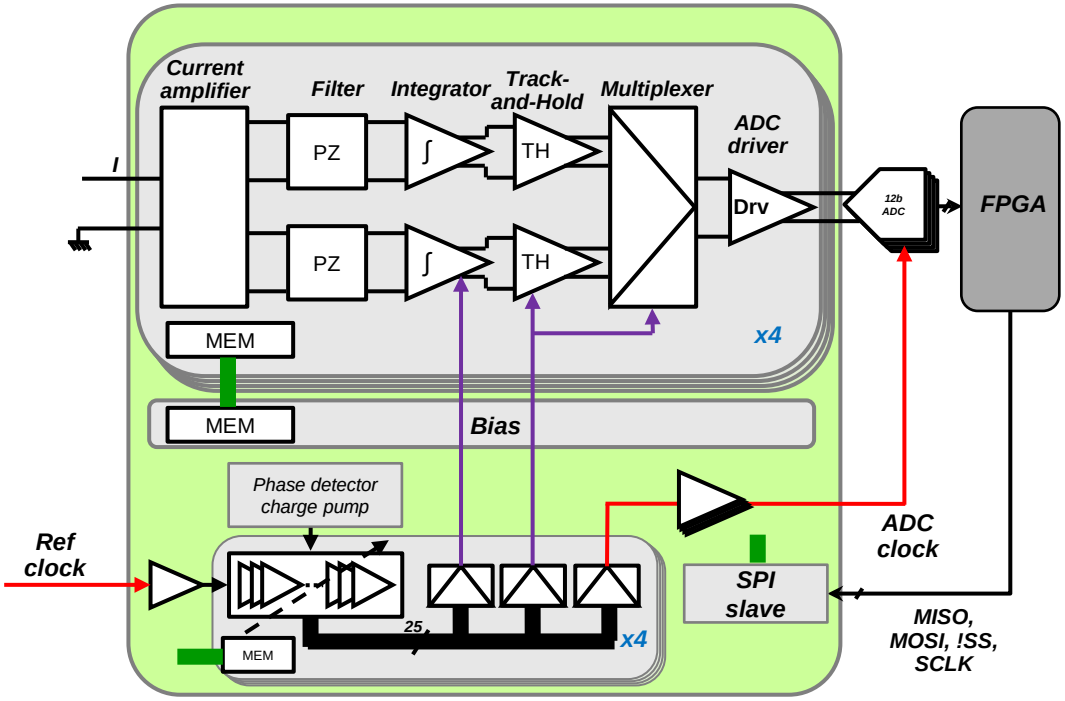
Whereas std amp should have e_n< 1 nV/√Hz !
➔ Input Rterm = 50Ω generates too much noise

- Dynamic pedestal subtraction (CDS):
  - Needed to correct baseline shift
  - And to filter LF noise (pick-up)
    - Has proven to be crucial in LHCb
- Equivalent noise charge (ENC):
  - White noise $ENC^2_{A+I} \approx \frac{1}{2} i^2_{CLIP} T$
- amplifier + integrator (time T) + CDS:
  - Amp BW >> 1/T $ENC^2_{A+I+CDS} \approx i^2_{CLIP} T$

Noise PSD at different stages of the signal processing



ASIC: ICECALv3



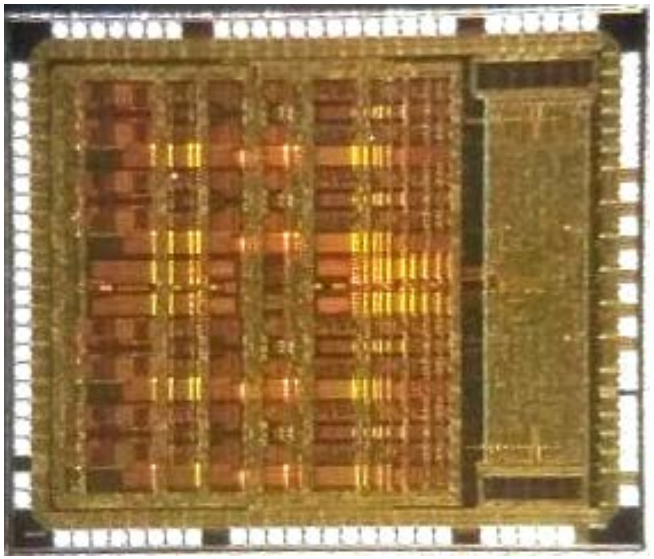
- Complete 4 analog channels
- Tunable parameters
- 4 DLL for synchronization

ICECALv3 chip:

SiGe BiCMOS 0.35um

AMS 10.5 mm^2

Received: July 2014



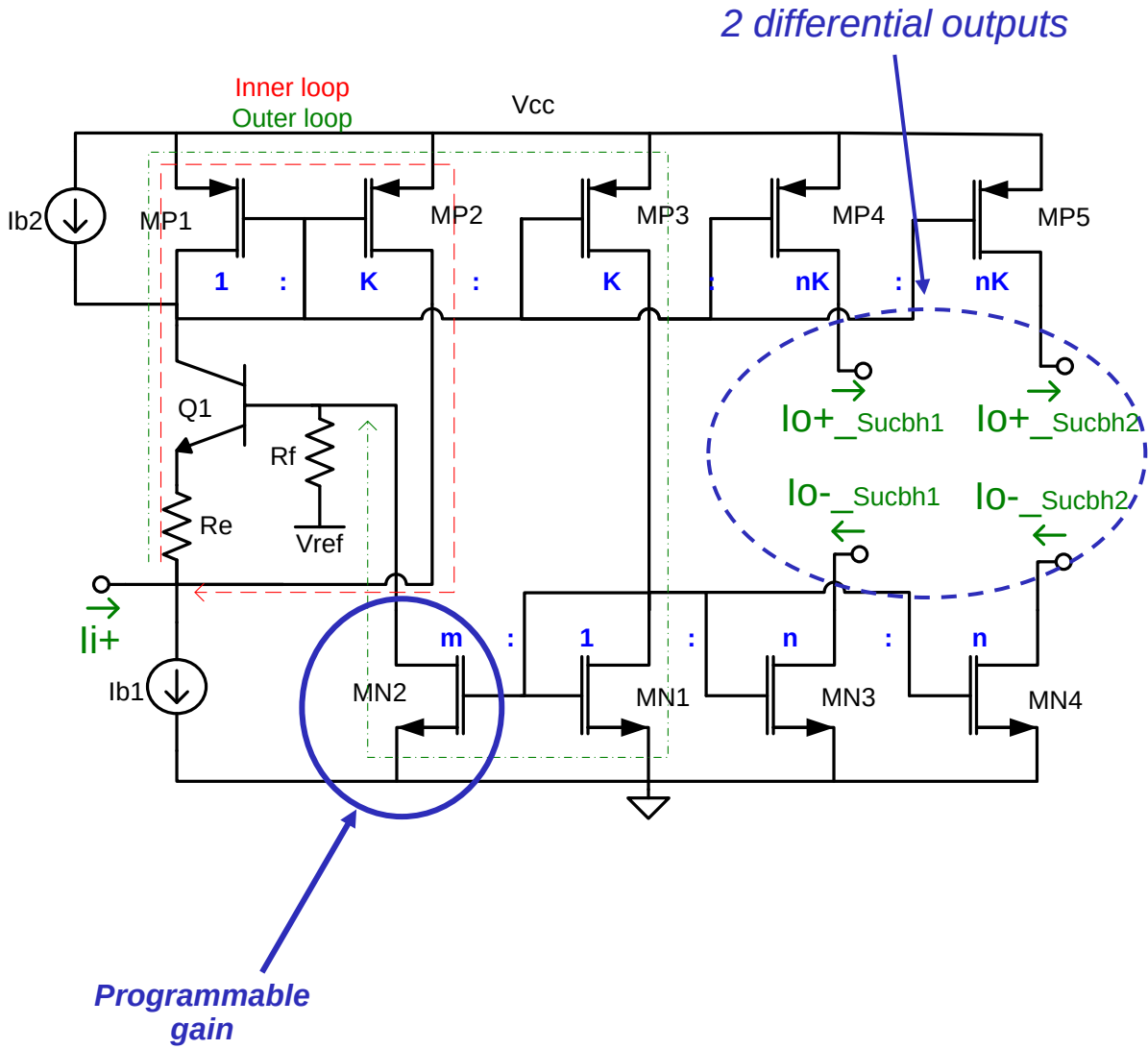
- Purpose: test key points of the circuit
  - Input impedance control by current feedback
  - Low noise performance
  - Dynamic range: Linearity
- Also, to test critical aspects of a switched solution:
  - Offset between subchannels
  - Plateau and spill over of the integrator output

Current Amplifier Input Stage

- Current mode feedback:
  - Inner loop: lower Z_{in}
    - Current feedback (gain): mirror: K
  - Outer loop: control Z_{in}
    - Current feedback: mirror: m
    - Current gain: m
- Electronically cooled input impedance

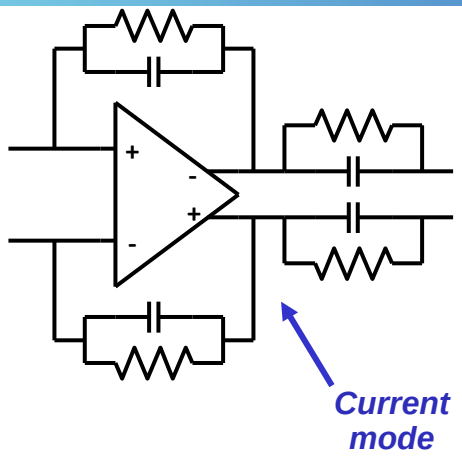
$$Z_i \approx \frac{1/g_{m1} + R_e}{1+K} + \frac{K}{1+K} mR_f$$

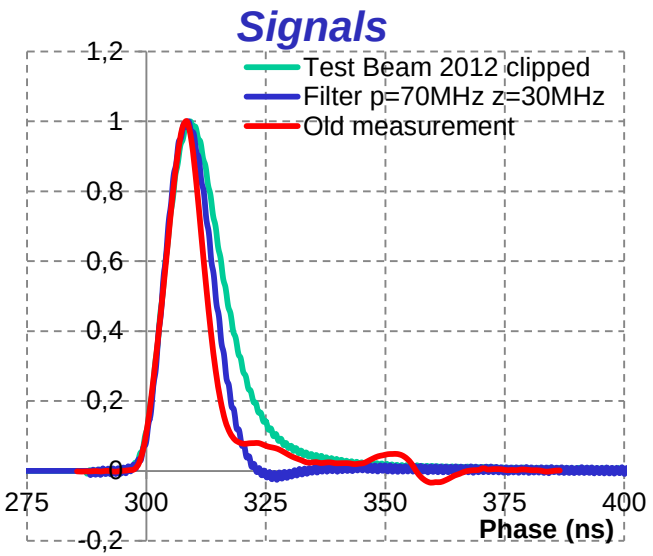
- Current feedback with programmable gain
  - Compensate Z_{in}
  - 5 bits

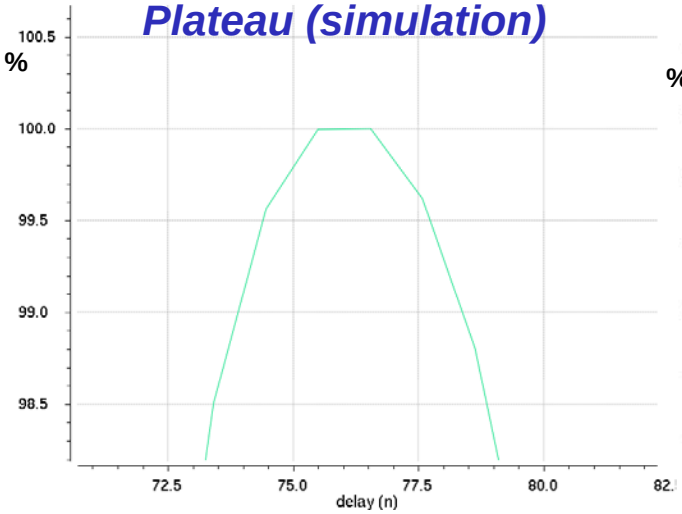


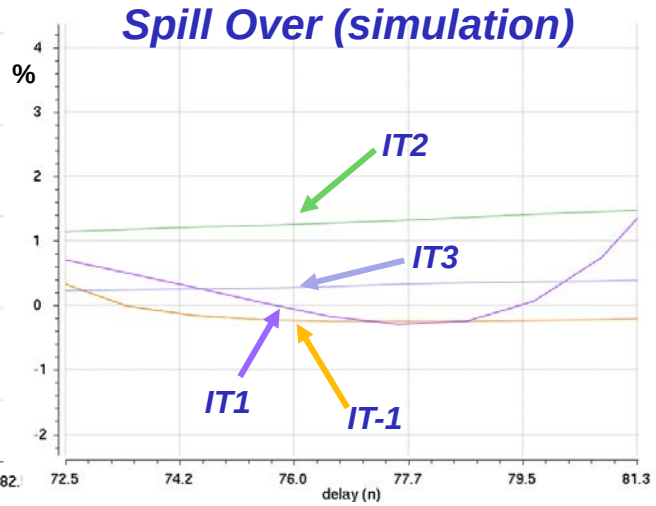
Pole zero filter stage

- Problem :
  - Signal from test beam is wider than expected
- Solution: pole-zero filter
  - Pole at 70 MHz
  - Zero at 30 MHz
- To reduce signal LF component:
  - Better plateau
  - Reduce spill over
- Variable capacitors:
  - Adjust for variations
  - Cope with different signals
  - Pole 6 bits
    Zero 5 bits

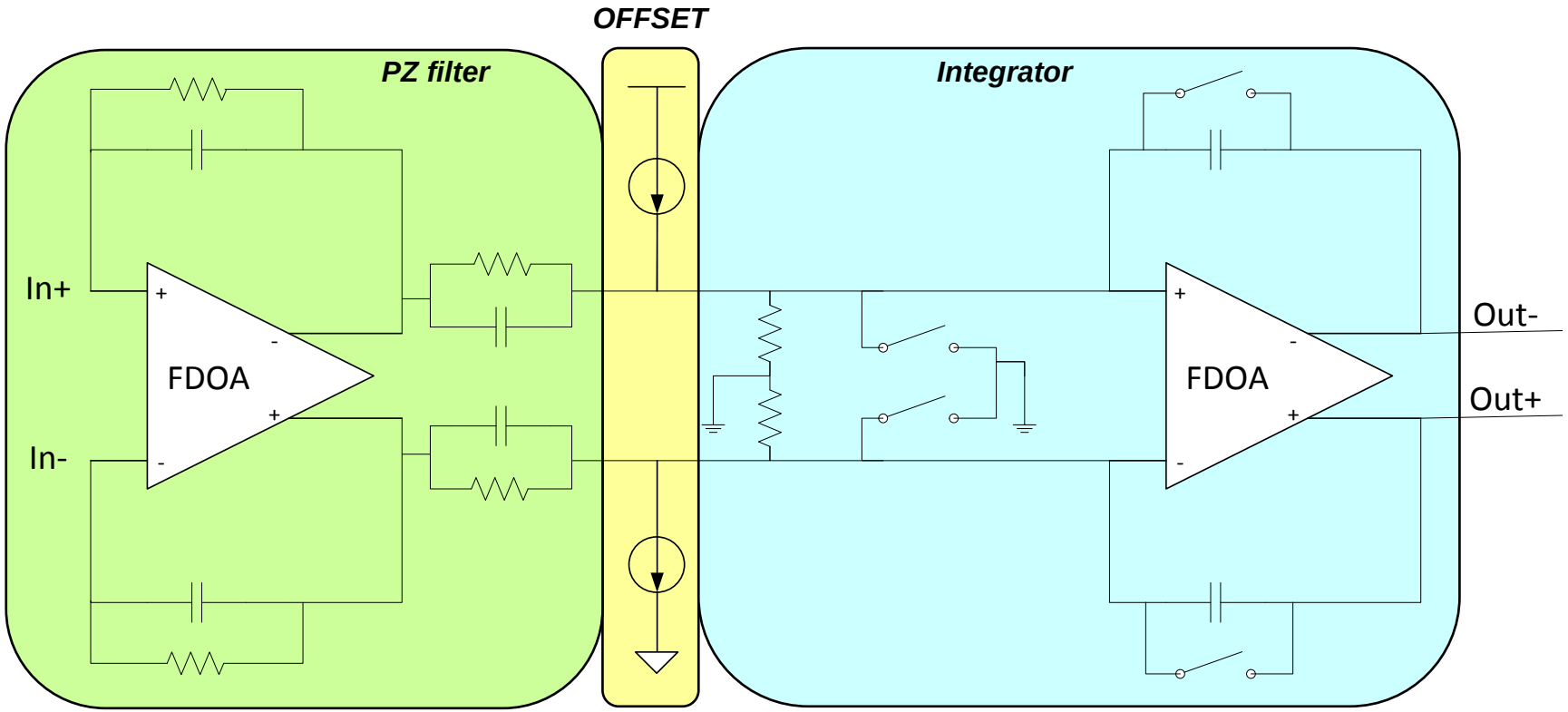








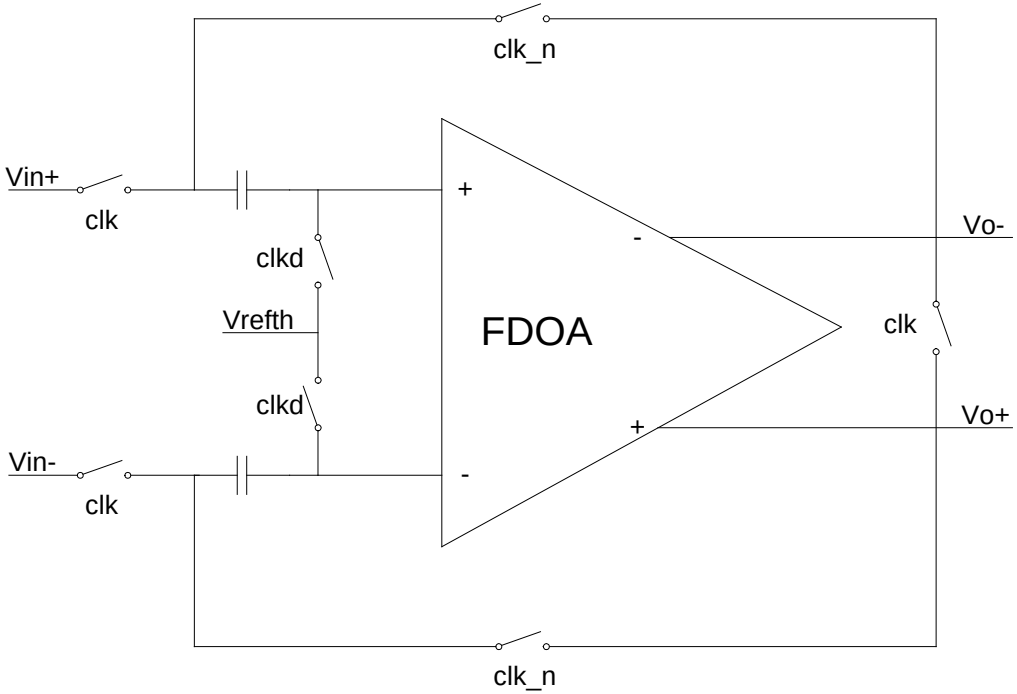
Offset

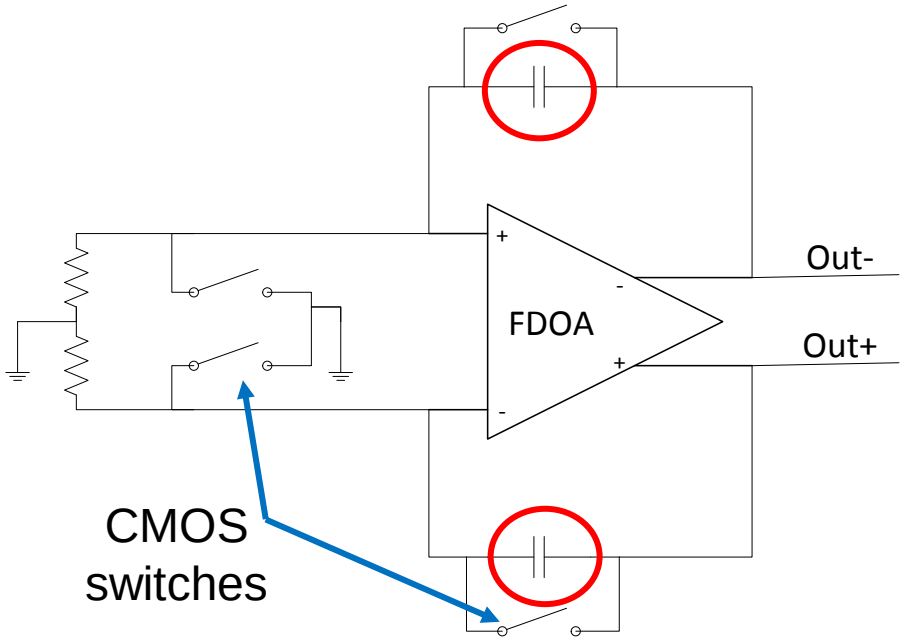


- Programmable offset created by current at the integrator input:
  - Modify the integrator output voltage by integrating a fixed current
  - Programmable level: 0 to 1.5 V in differential mode.
  - 6 bits: 4 MSB common and 2 LSB different for each subchannel

Switched Integrator / Track-and-Hold

- Switched integrator
  - 2 states:
    - Integration
    - reset
- Programmable capacitor value
  - Compensate variations in gain
  - 5 bits





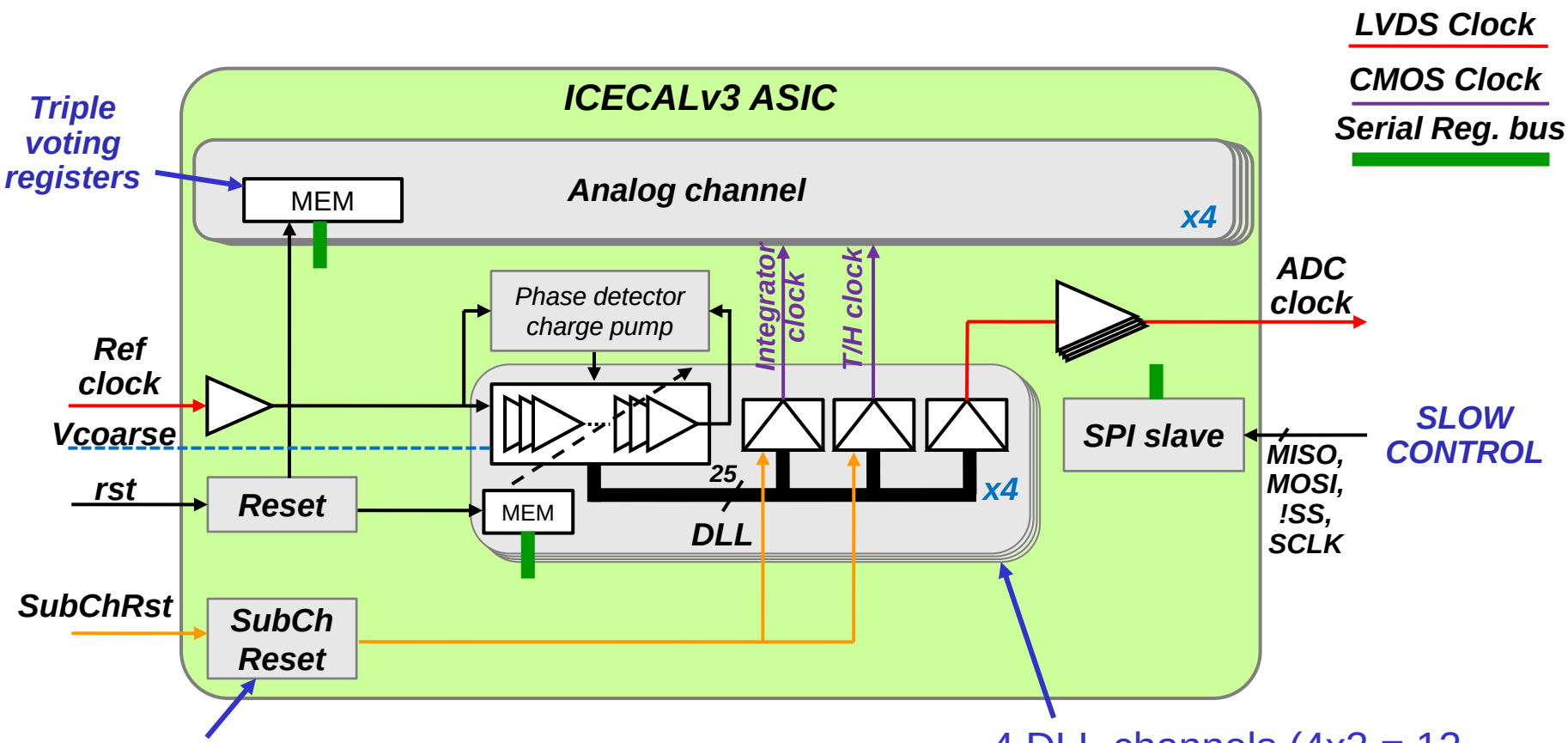
- Track-And-Hold:
  - 12 bits

Delay Line

- We need delay lines:
  - To synchronise ICECAL integrator, track & hold and the external ADC.

- Challenges:
  - Radiation hardness:
    - SEU → TMR (triple voting).
    - SET → glitch suppressors.
    - SEL → guard rings (full custom digital design).
  - Delay line variability:
    - Process variations → **external** adjust (coarse).
    - Environmental variations → **internal** locked loop adjust (vControl).
  - Noise:
    - Stringent noise requirements of the ASIC analog components (ICECALv3) → differential design, guard rings..

Delay Line



Sub-channel reset:

– to fix the sub-channel in use (e.g start always with first sub-channel)

4 DLL channels (4x3 = 12 independent sub-channels):

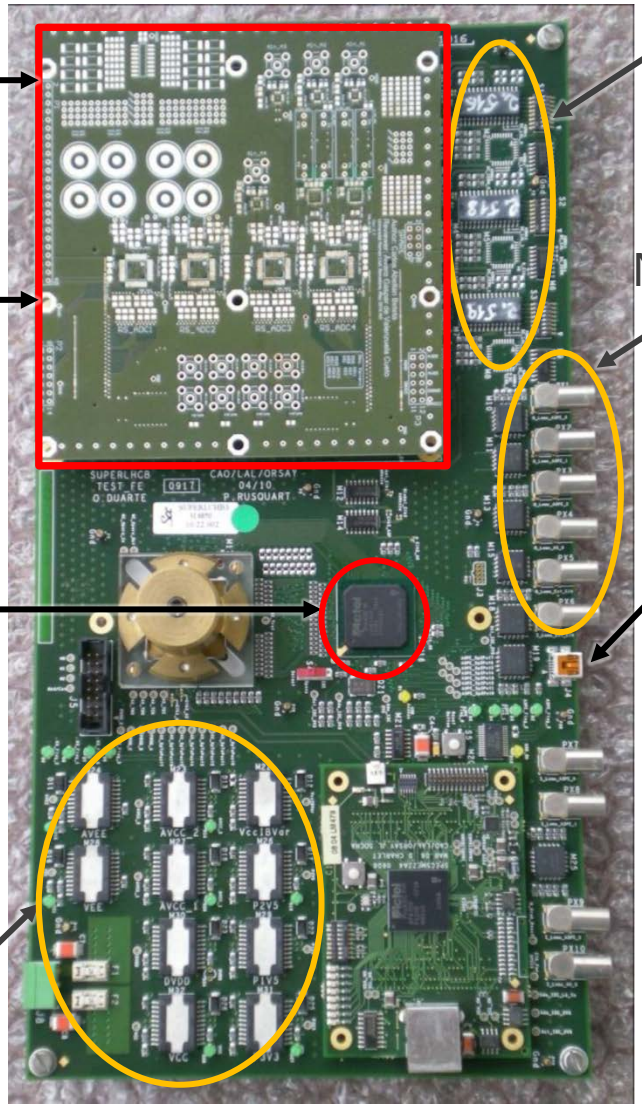
– 25 configurable clock phases (1-ns step).

Front End Board Prototype Tests

Analog Mezzanine (ASIC/COTS)

WAVEFORM GENERATOR

Test signal

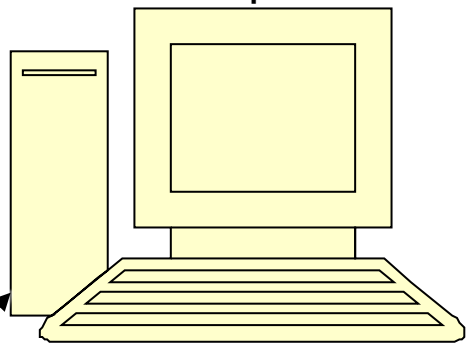


Delay Chips

NIM I/O

USB

PC for control and data acquisition



FPGA Actel A3PE1500

Verilog blocks:

- USB and control board
- General functionality
- DAQ

Regulators

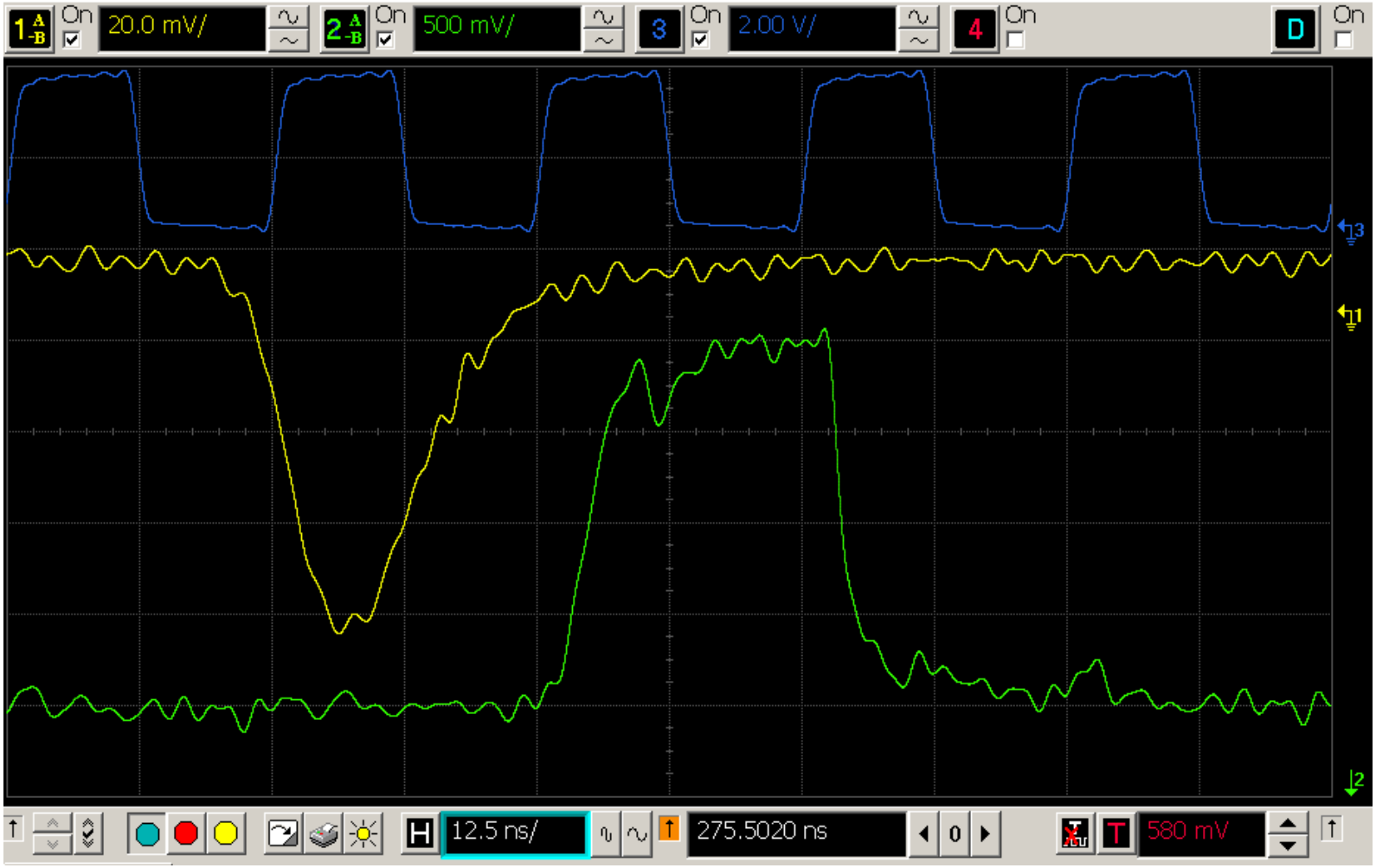
- Tests:
  - Time alignment
  - Linearity
  - Noise
  - Integral plateau
  - Spill over
- Status:
  - Automatization almost ready
  - More precise configuration values required

Measurements: analog I/O example

ADC clock

ICECALv3 ASIC input

ICECALv3 ASIC output

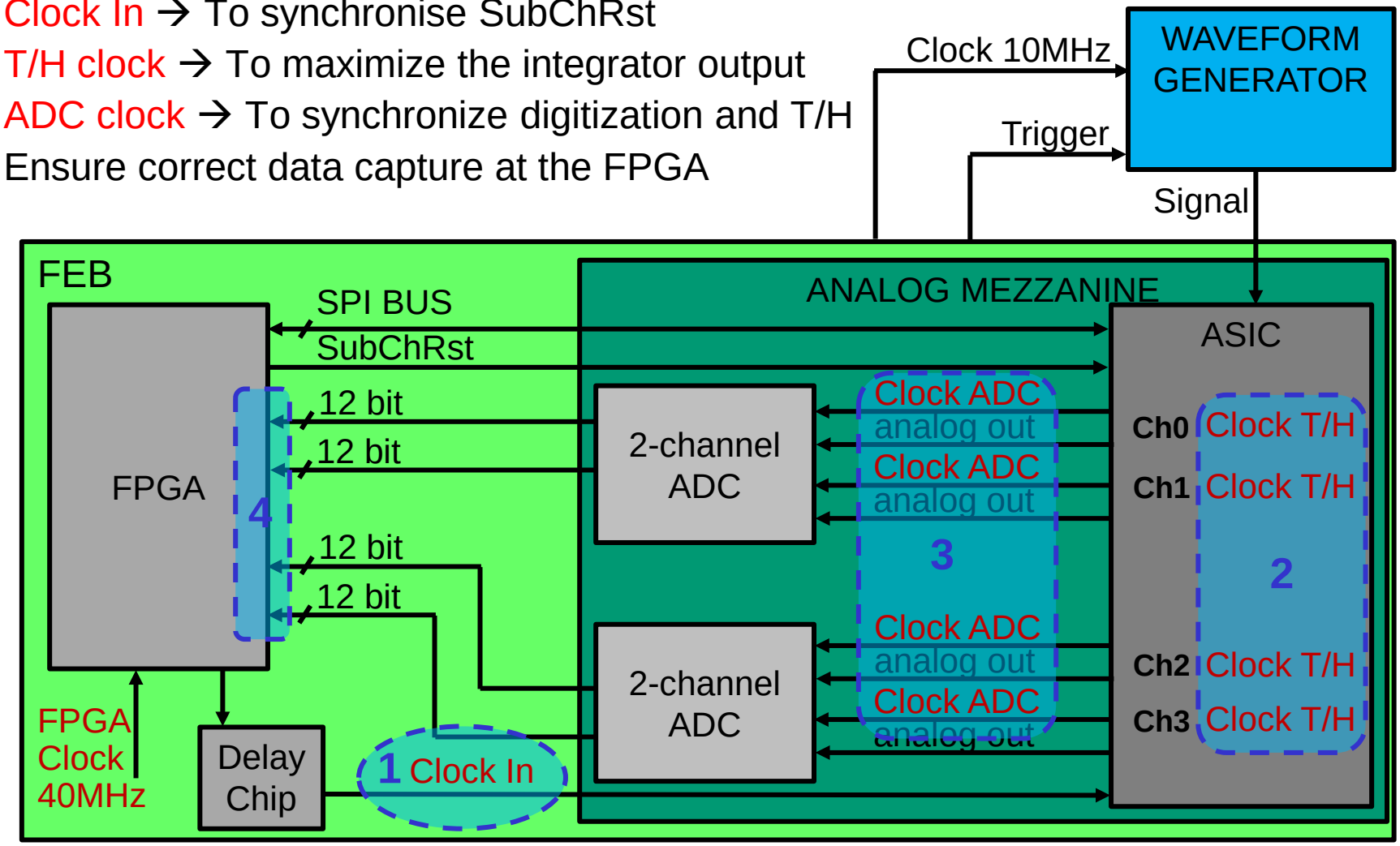


ICECALv3 time alignment

Clock phases to be adjusted:

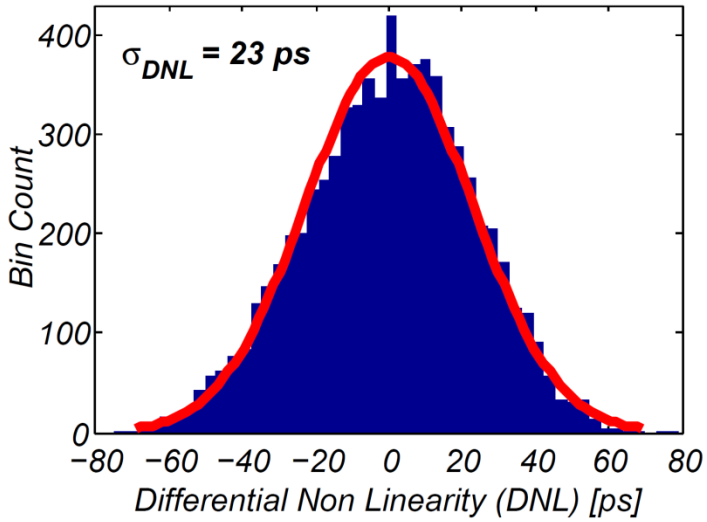
1) Clock In → To synchronise SubChRst
2) T/H clock → To maximize the integrator output
3) ADC clock → To synchronize digitization and T/H
4) Ensure correct data capture at the FPGA

(Synchronization in prototype is equivalent to the final detector)

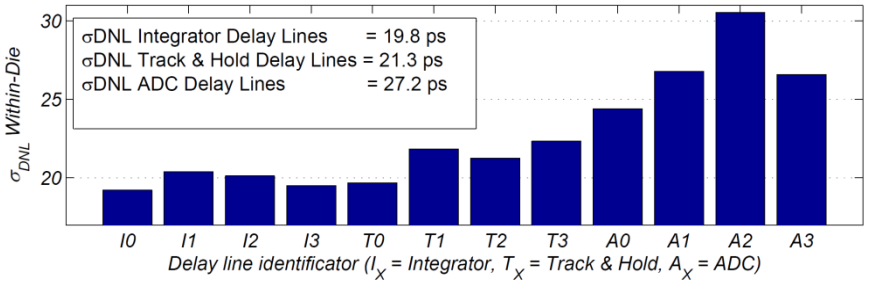


Delay line measurements

- Measurements from a standalone prototype (25 chips tested)
- The LVDS clock outputs are measured by means of a 1 GHz bandwidth differential probe and a 20 Gsps oscilloscope
- Linearity
  - Sweep the 25 possible phases
  - 1ns expected
  - ➢ $DNL_i = abs(Delay_i - Delay_{i-1})$

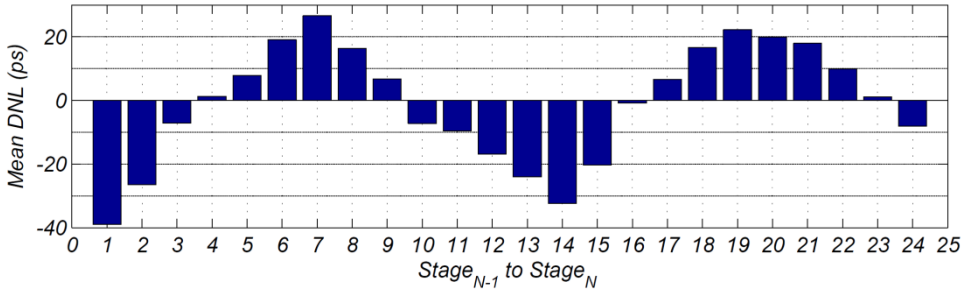


Within-Die variations measurements



Difference is caused by the lack of symmetry in the ADC clock delay lines

Mean DNL for each VCDL stage

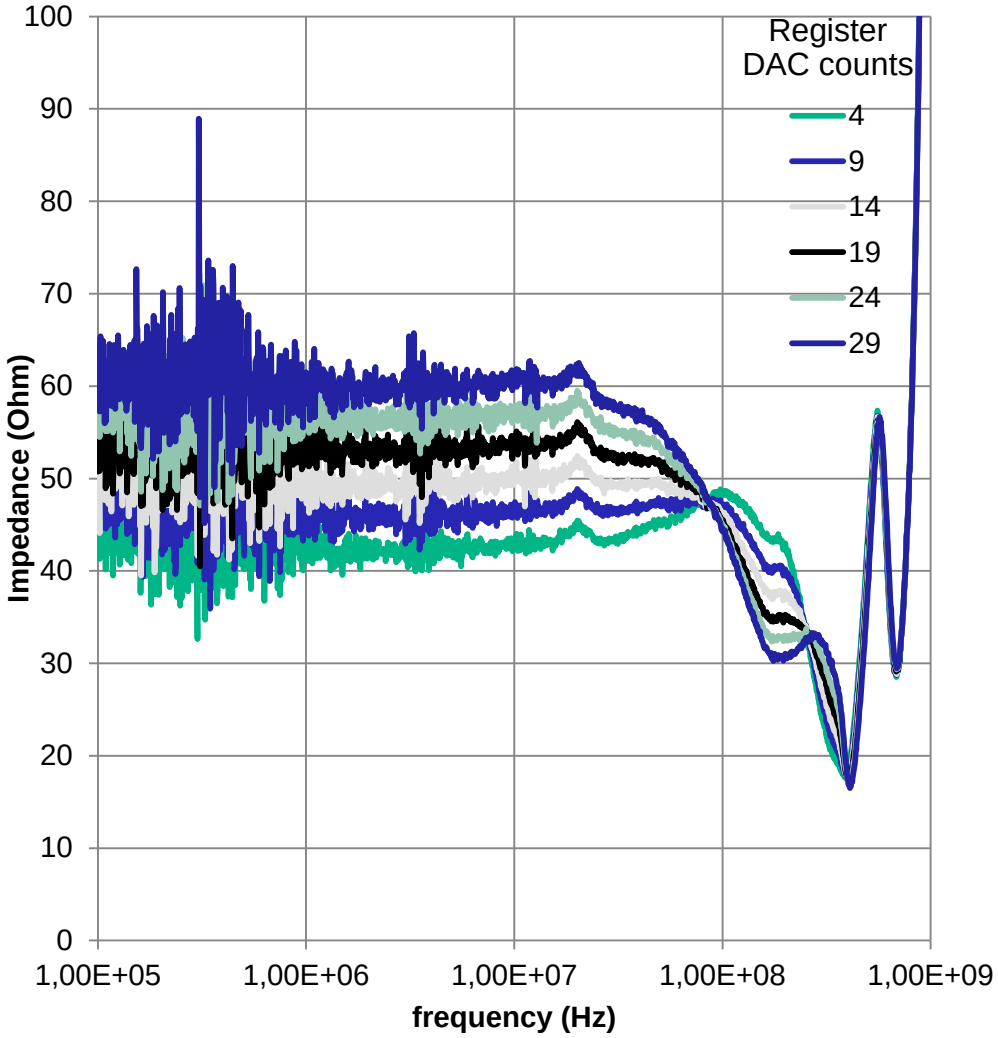


Periodical behavior that matches with the multiplexor layout design pattern

Radiation hard programmable delay line for LHCb calorimeter upgrade

J. Mauricio et al 2014 JINST 9 C01016

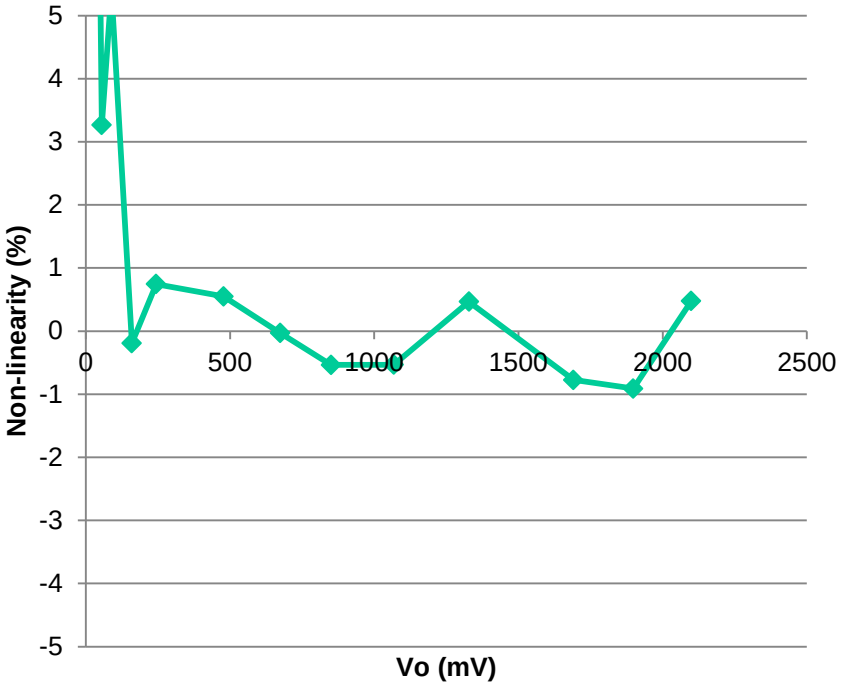
Input Impedance



- Measurement setup
  - Network analyzer at the input (Rohde&Schwarz ZVL)
  - Approximate results due to not-optimal connectivity
- Plot:
  - Input impedance for different configurations
  - Range: ~40 to 60 Ω
  - 50Ω corresponds to 14 DAC counts

Linearity and noise

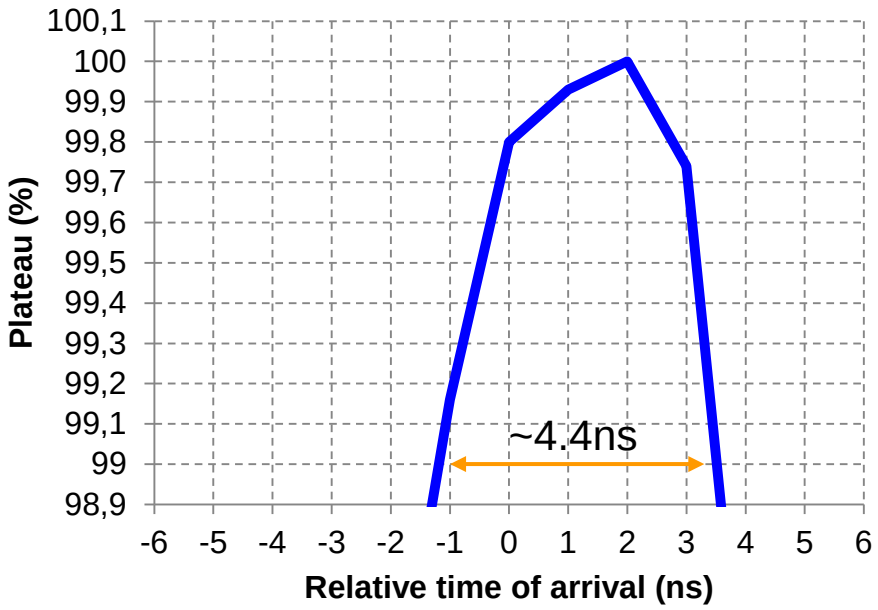
- Linearity:
  - Spec: better than 1% in the whole signal range
  - Needed to add a little offset respect default value to avoid non linearity for $V_0 > 1.5V$
  - Waveform generator noise affects linearity for low values

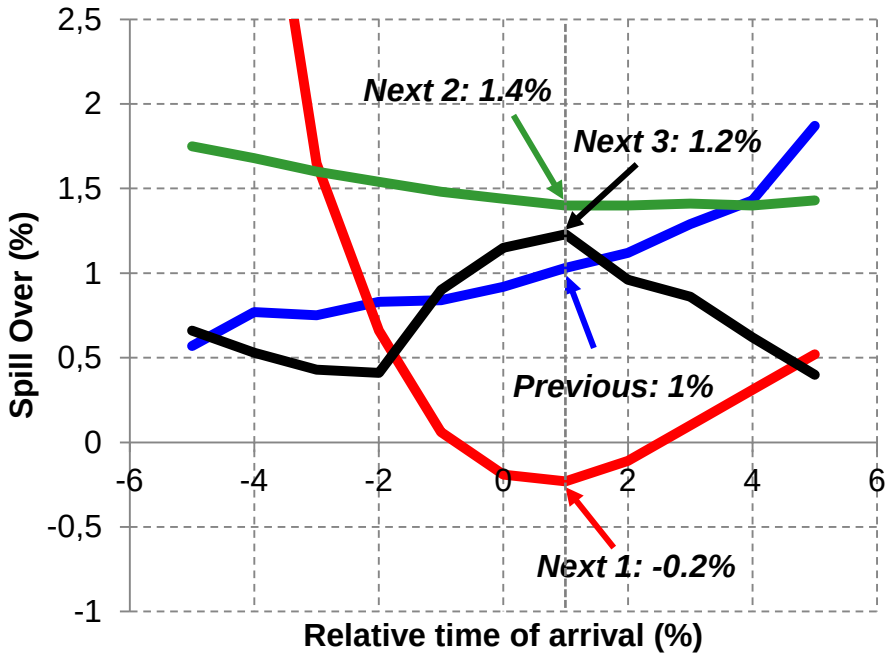


- Noise:
  - Spec: ~1 ADC count
  - Measured noise without cable at the input:
    - 1.4 ADC counts
    - 1.7 ADC counts with pedestal subtraction
  - More measurements needed with the setup grounding reviewed
  - If the gain or offset configuration varies, the noise will be affected.

Plateau and spill over

- Plateau:
  - Spec: less than 1% variation in ±2ns
  - PZ filter default configuration is enough
- Spill over:
  - Spec: less than 1% for all previous and next clock cycles
  - Need to adjust the PZ filter for final configuration of all the chips





Outlook

- ICECALv3, an integrated circuit for the Upgrade of the LHCb Calorimeter Front End electronics has been presented.
  - Analog architecture based on:
    - Current mode preamplifier with cooled termination for reduced input noise
    - 2 fully differential interleaved channels to avoid dead time
    - Switched integrator and a Track-and-Hold
    - A pole-zero filter to optimize plateau and minimize spill over
    - Configurable parameters to compensate for fabrication process and calibration
  - 4 channels
  - Delay lines on-chip for synchronization
- Measurement and test campaign ongoing
  - First results are positive
  - More precise configuration parameters required
  - Automatization almost ready for the 30 chips

Further applications

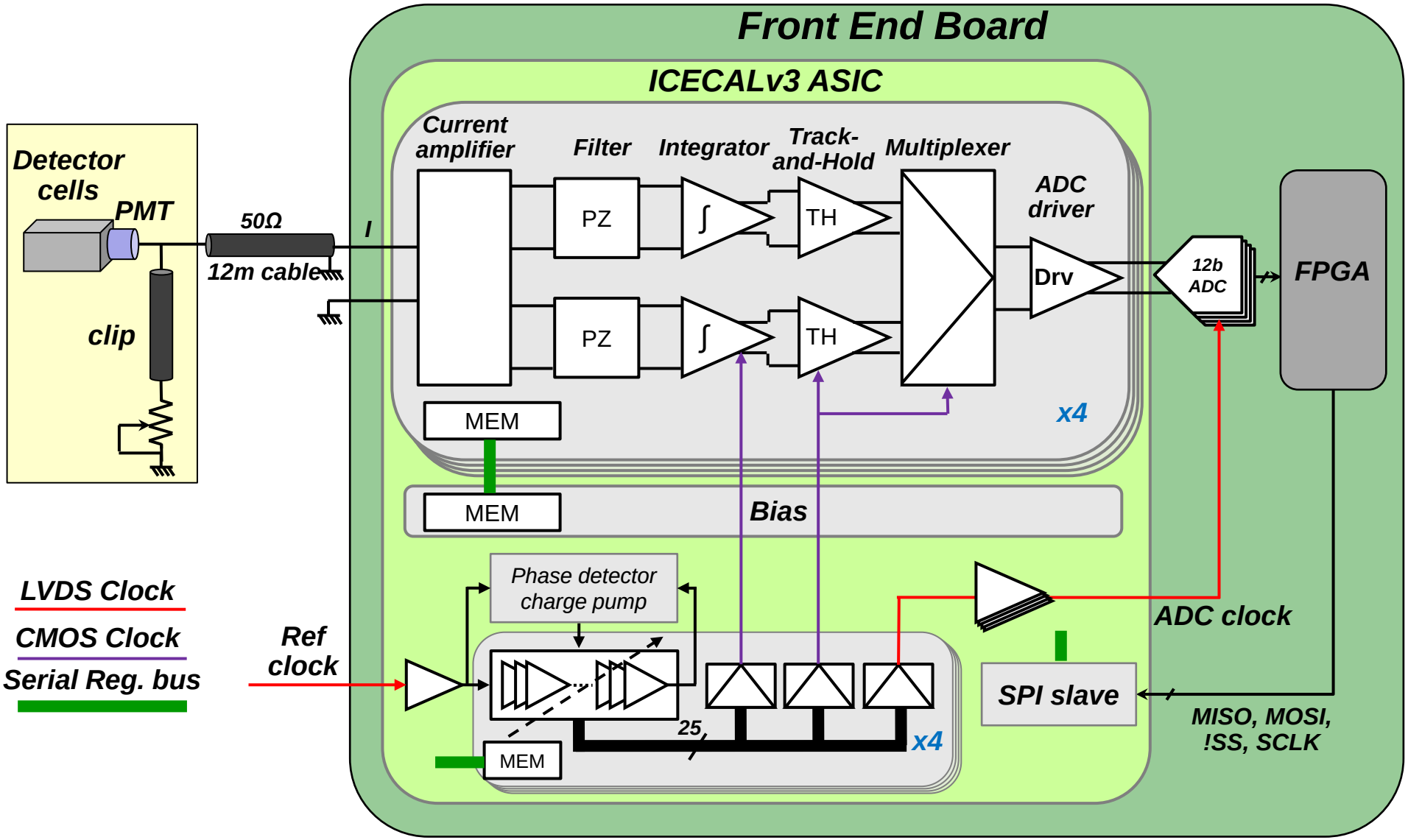
- ICECALv3, could be useful for many applications with PMT signal and a 40 MHz clock source.
  - Adjustable parameters:
    - Gain
    - Pole zero filter

- Other detectors interest:
  - Secondary Particle Acquisition System for the CERN Beam Wire Scanners Upgrade (see poster from J. L. Sirvent today)
    - Tests with the ICECALv2 (preamp + integrator + T/H)

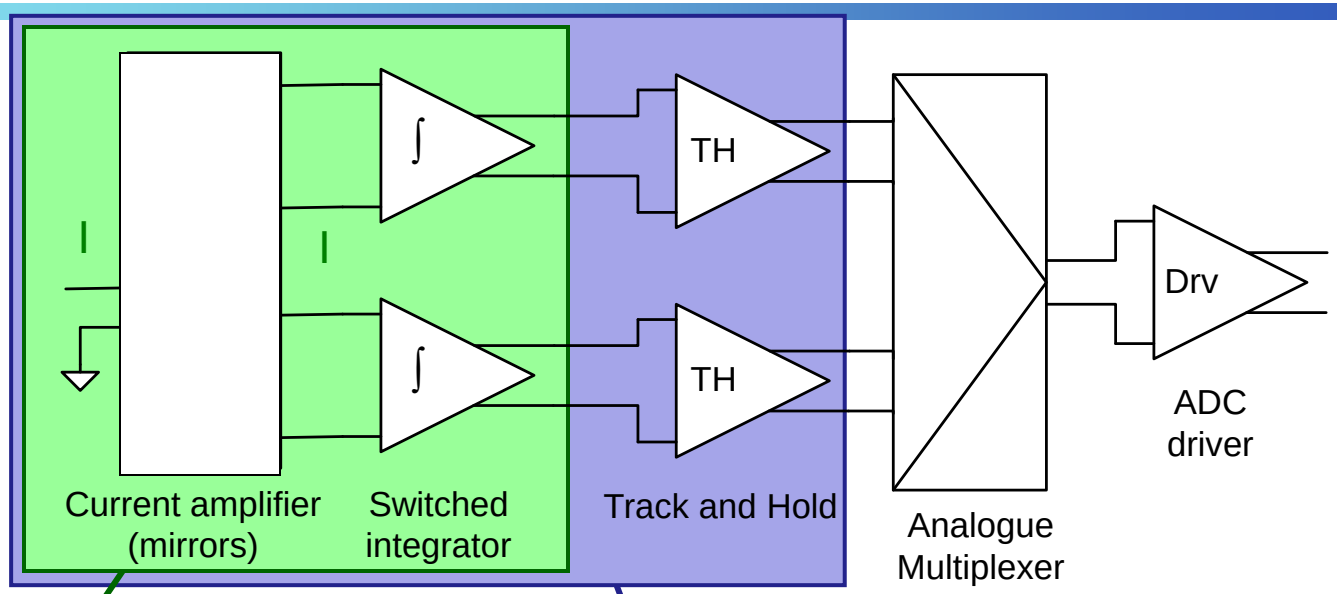
Thank you for your attention!

Back-up:

ICECALv3 architecture

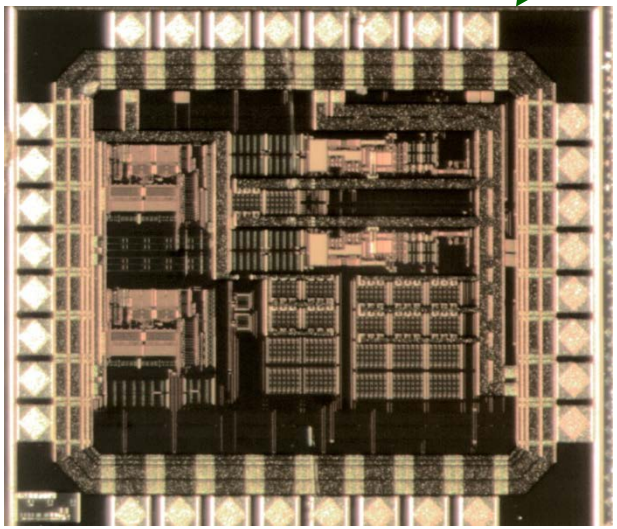


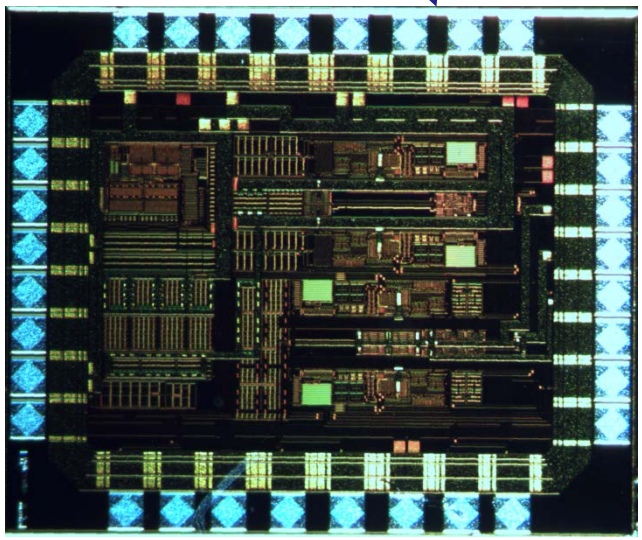
Previous prototypes



ICECALv1 chip:

SiGe BiCMOS 0.35um
AMS 2 mm^2
Received: October 2010
12 chips





ICECALv2 chip:

SiGe BiCMOS 0.35um
AMS 2 mm^2
Received: September 2011

Choice of Technology

- SiGe BiCMOS is preferred:
  - SiGe HBTs have higher gm/Ibias than MOS: less noise, less Zi variation
  - SiGe HBTs have higher ft (>50 GHz): easier to design high GBW amplifiers
- Several technologies available:
  - IBM
  - IHP
  - AMS BiCMOS 0.35 um

	IBM	IHP	AMS
HBT ft	> 100 GHz	190 GHz	60 GHz
CMOS	0.13 um	0.13 um	0.35 um
Proto Cost [€ /mm^2]	> 3 K	> 3 K	1 K

- AMS is preferred
  - Factor 2 or 3 cheaper
  - Too deep submicron CMOS not required / not wanted:
    - Few channels per chip (4 ?)
    - Smaller supply voltage
    - Worst matching
  - Radiation hardness seems to be high enough
    - 30 Krad seems to be OK (checked by other Upgrade projects)

Specifications

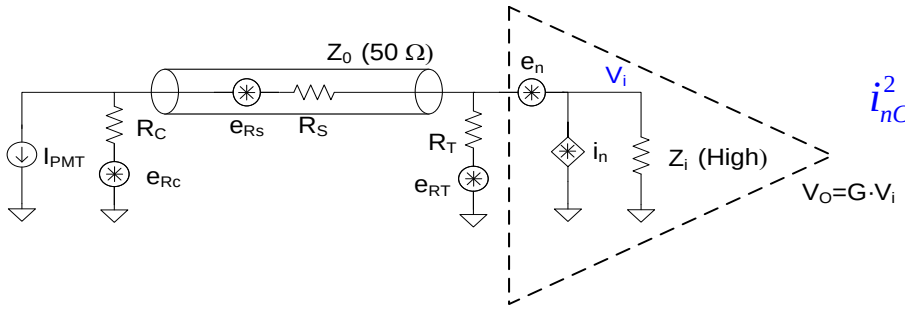
Energy range	0-10 GeV/c (ECAL) Transverse energy
Calibration	4 fC /2.5 MeV / LSB
Dynamic range	4096-256=3840 :12 bit
Noise	<≈1 LSB or ENC < 4 fC
Termination	50 ± 5 Ω
Shaping	25 ns (99 % of the charge)
Spill-over noise	< LSB
AC coupling	5-20 μs
Baseline shift Prevention	Dynamic pedestal subtraction (CDS) Pedestal is the smallest of 2 prev. samples
Max. peak current	4-5 mA (clipped)
Spill-over correction	Clipping
Linearity	< 1%
Crosstalk	< 0.5 %
Timing	Individual (per channel)

- **Signal processing elements (analog):**
  - **Amplification**
  - **Integration / shaping**
- **Dynamic pedestal subtraction (CDS):**
  - **Needed to correct baseline shift**
  - **And to filter LF noise (pick-up)**
    - **Has proven to be crucial in LHCb**
  - **Noise Power Spectral Density (PSD) in signal increases by ~ sqrt(2)**

Analog Signal Processing

- Noise contributions of

(1) Std high Zin amplifier

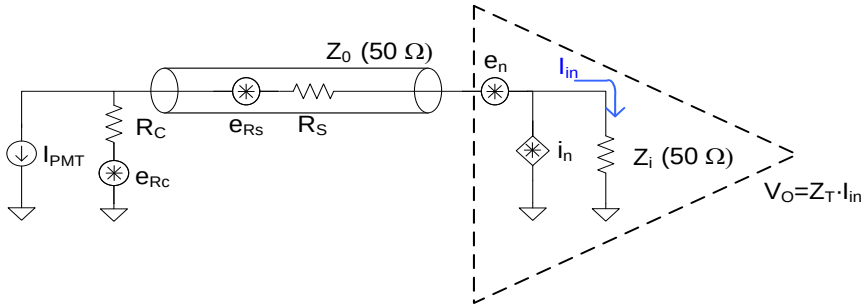


Referred to the clipped PMT current i_{nCLIP}

$$i_{nCLIP}^2 = \frac{e_n^2}{|Z_0|^2} + i_n^2 \left|\frac{1}{2}\right|^2 + \frac{4KT}{R_T}\left|\frac{1}{2}\right|^2 + \frac{4KT}{R_C}\left|\frac{R_C}{Z_0 + R_C}\right|^2 + \frac{4KTR_S}{|R_S + Z_0|^2}$$

Typically dominant contributions

(2) Electronically cooled amplifier

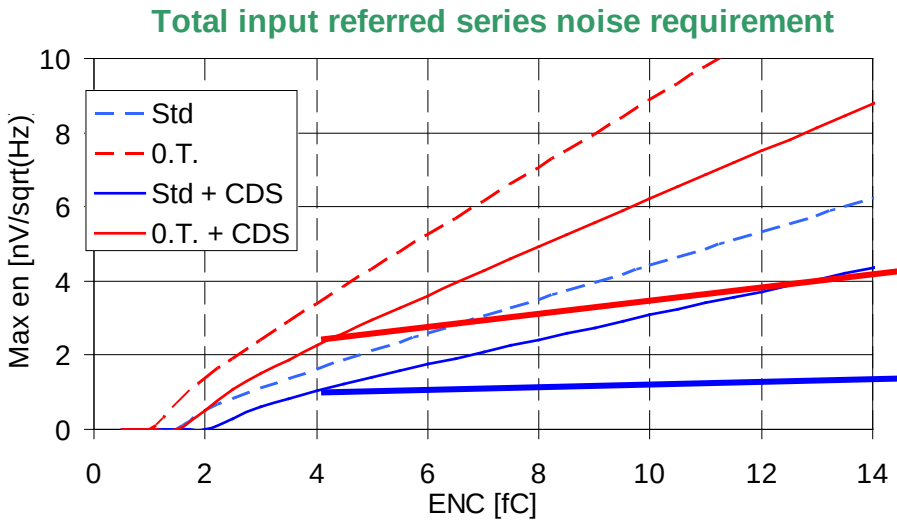


$$i_{nCLIP}^2 = \frac{e_n^2}{|2Z_0|^2} + i_n^2 \left|\frac{1}{2}\right|^2 + \frac{4KT}{R_C}\left|\frac{R_C}{Z_0 + R_C}\right|^2 + \frac{4KTR_S}{|R_S + Z_0|^2}$$

Analog Signal Processing

- Equivalent noise charge (ENC): amplifier + integrator (time T) + CDS:
  - White noise $ENC^2_{A+I} \approx \frac{1}{2} i^2_{CLIP} T$
    - Resistive source imp.
  - Amp BW >> 1/T $ENC^2_{A+I+CDS} \approx i^2_{CLIP} T$

- Assumptions:
  - Cable modelled as lumped element*
  - Cable seen as Z_0 at HF from amp. side*
  - $R_T=Z_0$ (V amp) and $Z_i=Z_0$ (I amp)
  - Uncorrelated noise for CDS



- R_C=21 Ω
- R_S=18 Ω
- i_n neglected

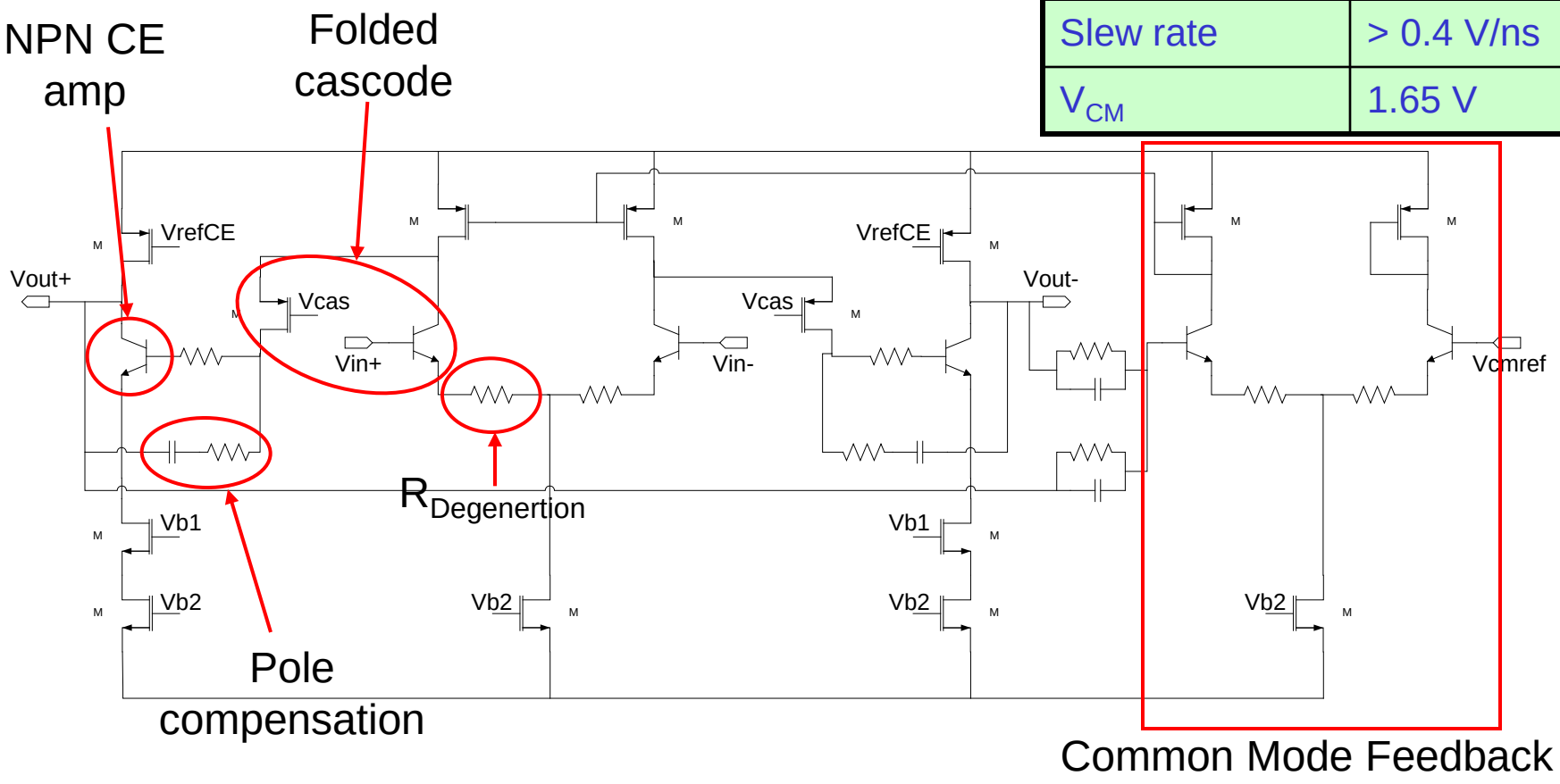
·* R.L. Chase, C. de La Taille et alt., NIM A330, 1993

- OT with e_n< 2 nV/sqrt(Hz) fulfils requirements,
- Whereas std amp should have e_n< 1 nV/sqrt(Hz) !

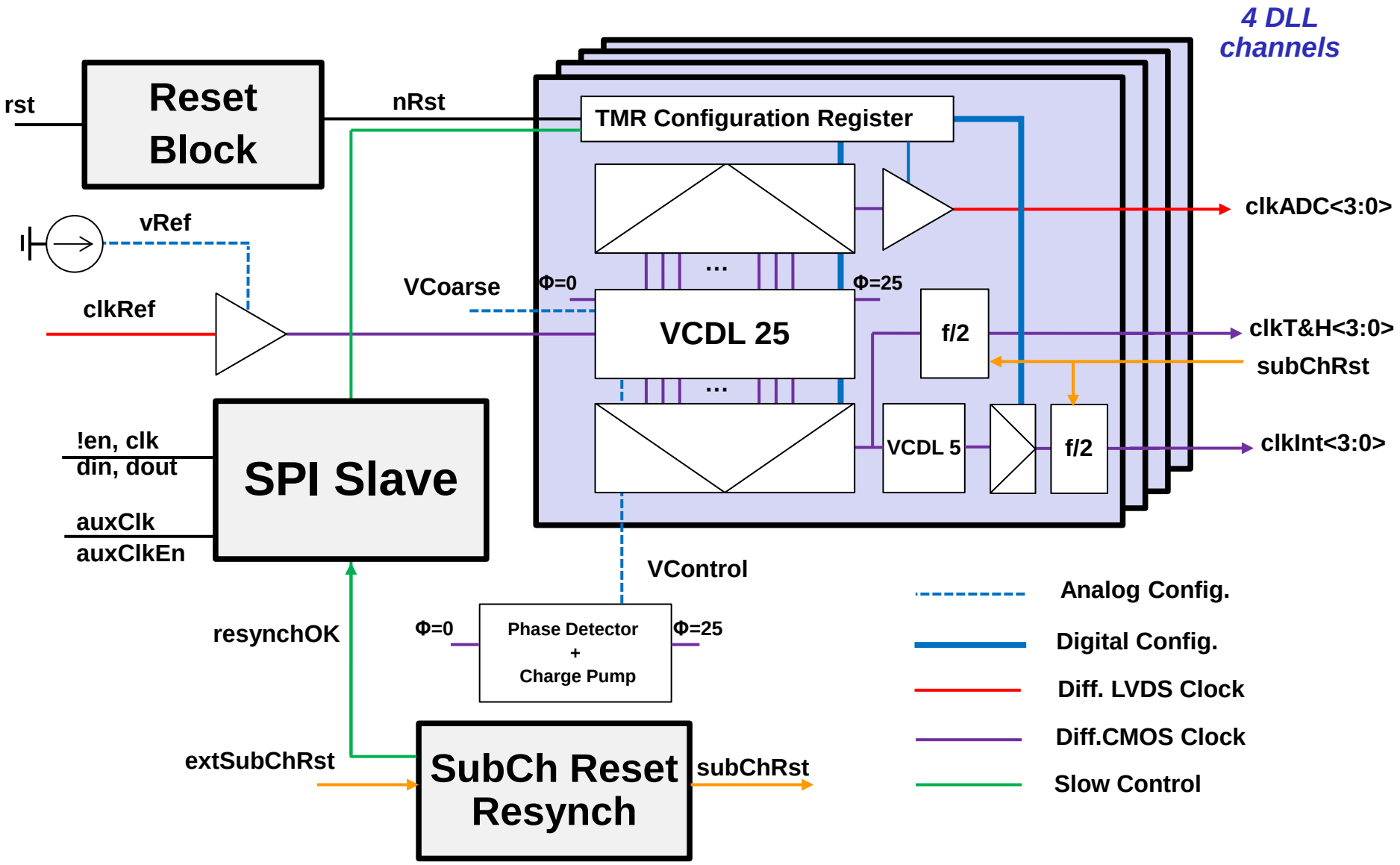
Channel Architecture: FDOA

- Fully differential Op Amp:
  - Folded cascode + Miller stage with CMFB

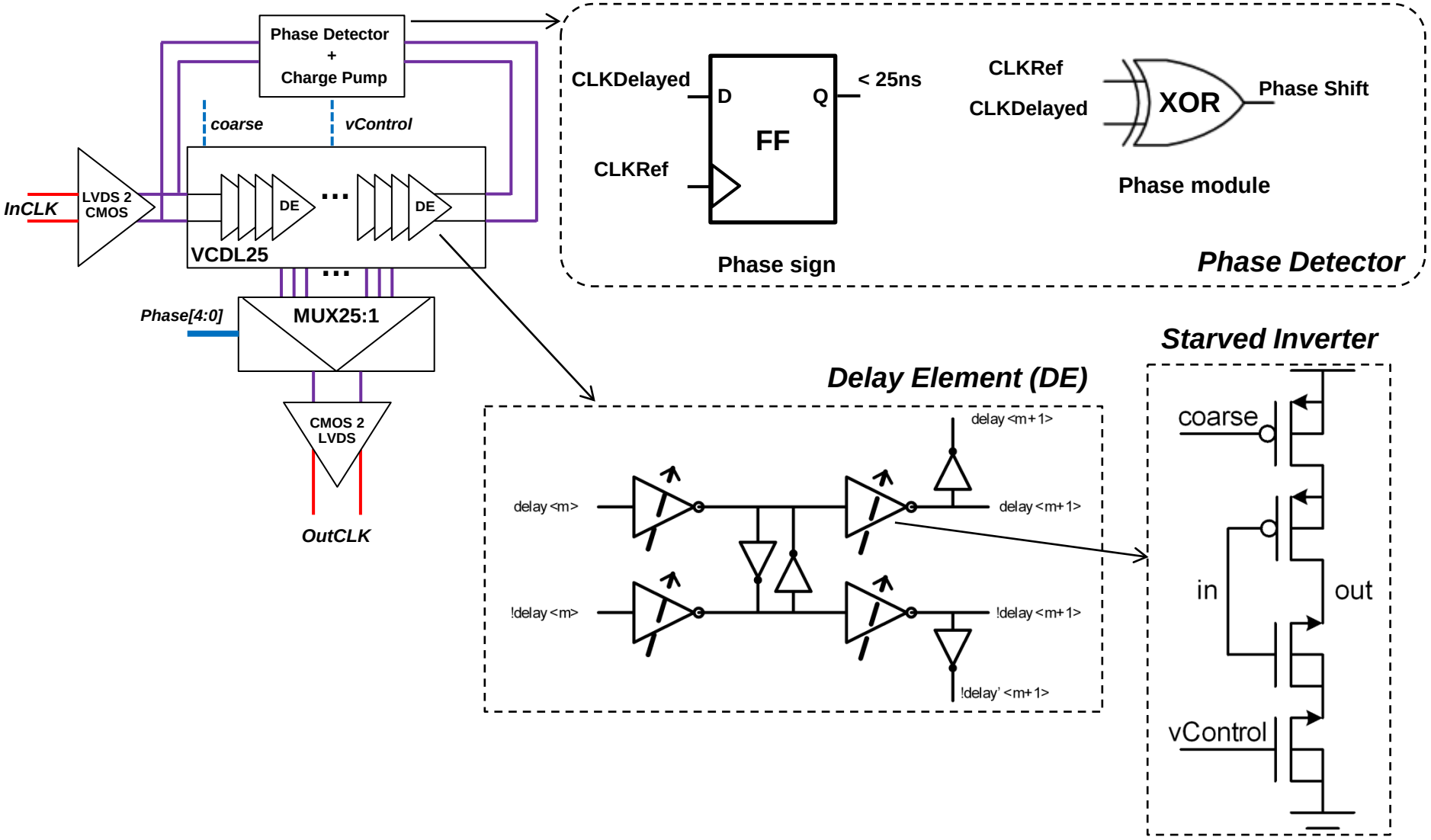
FDOA specifications	
Parameter	**Value**
Gain bandwidth	500 MHz
Phase margin	> 65º
Slew rate	> 0.4 V/ns
V_{CM}	1.65 V



Delay Chip Block Overview

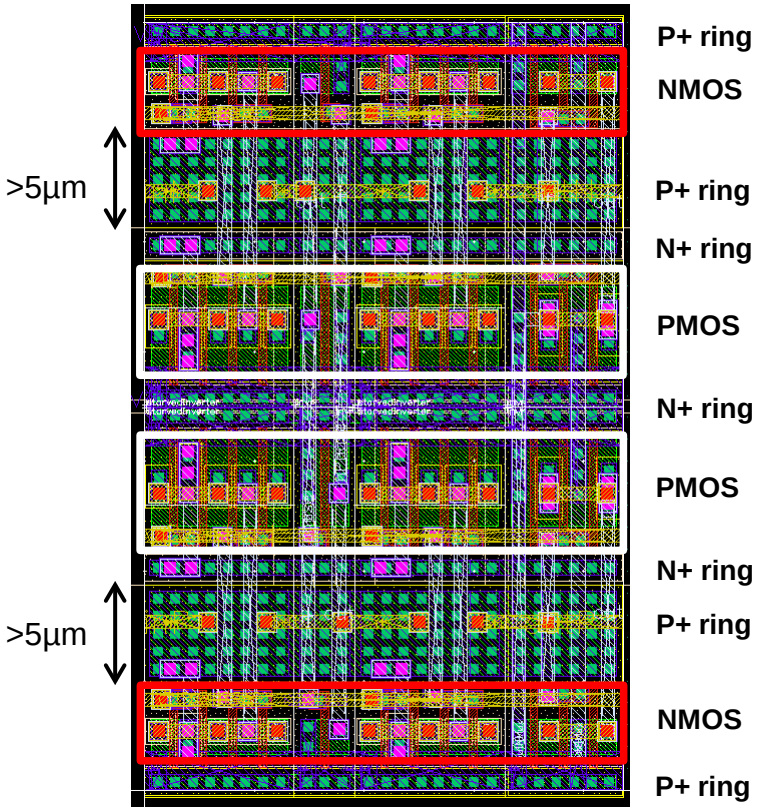


Delay Line: design overview



Delay Line features

- 4 DLL Channels (4x3 = 12 independent sub-channels):
  - 25 configurable clock phases (1-ns step).
  - Peak-to-peak Jitter: 3 ps.
  - Differential Non Linearity (DNL): 18 ps.
  - Delay Range: 17.45 ~ 39.88 ns.
  - DLL Locking time: 2.5 ~ 10 µs.
  - DLL peak-to-peak ripple voltage ~ 1 mV.
  - ~280 mW of power consumption.
  - Technology: AMS 0.35 CMOS.
- Reset:
  - Glitch supressor (≤ 8ns) ensures that SETs do not accidentally reset the chip.
- Reliability (SEL avoidance):
  - Extra design rules:
    - ≥ 5µm between N-DIFF layer and NWELL.
    - Guard rings between PMOS and NMOS.



Example: Delay Element

Slow control

- We need slow control:
  - To configure and check the status of delay lines.
  - To configure ICECALv3 analog blocks.

- Challenges:
  - Radiation hardness:
    - SEU → TMR (triple voting).
    - SEL → guard rings (full custom digital design).

- Features:
  - SPI slave:
    - Works fine @ 20 Mbps.
    - Up to 32 configuration registers and 32 status registers.
    - Also implements a software reset pulse (to reset DLL charge pumps).
  - Serial registers:
    - 16 bits R/W TMR registers (configuration).
    - 8 bits RO (status). No memory.