Contribution ID: **95** Type: **Oral**

Low Noise 4-channel Front End ASIC with On-Chip DLL for the Upgrade of the LHCb Calorimeter

Wednesday 24 September 2014 11:35 (25 minutes)

An integrated circuit for the Upgrade of the LHCb Calorimeter front end electronics is presented. It includes four analog channels, a Delay Locked Loop (DLL) for signal phase synchronization for all channels and an SPI communication protocol based interface. The analog circuit is based on two fully differential interleaved channels with a switched integrator to avoid dead time and includes dedicated solutions to achieve low noise, linearity and spill-over specifications. The included DLL is capable of shifting the phase of the LHC clock (25 ns) in steps of 1ns. The selected technology is AMS SiGe BiCMOS 0.35um.

Summary

LHCb is one of the four large experiments of the Large Hadron Collider (LHC) located at the CERN laboratory near Geneva. Although it has already been covering a relevant part of its proposed physics program, a large increase of data is required in order to distinguish between models of new physics and an upgrade of the detector is planned.

The analogue signal processing of the upgraded calorimeter front-end board (FEB) consists in the integration of a photomultiplier pulse, which has been clipped and transmitted through a 12m 50Ω coaxial cable to the FEB. The main requirement is a reduction of the preamplifier input noise so that the total input referred noise voltage is smaller than 1nV/√Hz. As a consequence, a 50Ω termination resistor is not acceptable. An ASIC approach is adopted for this project to cope with integration constraints and a transistor based design required for the active termination scheme.

The presented implementation of the ASIC includes: four analog channels with programmable values to control the key parameters and compensate for process variations; a dedicated Delay Locked Loop (DLL) to synchronize each channel signal phase and a digital interface using SPI protocol.

The analog channel is designed with an input amplifier that includes an electronically cooled termination input stage with double feedback. A passive line termination would induce too large a noise and is avoided. Afterwards an alternated switched differential signal paths scheme permits the integration of the signal with no dead time between consecutive events. Each path includes a pole-zero filter in order to compensate for cable effects, a switched integrator with capacitive feedback, a Track-and-Hold for a 12-bit ADC and a MUX to select the correct sub-channel output signal. A fully differential signal processing is adopted in order to minimize the impact of common mode noise, which is important in a switched system.

Each analog channel includes a delay line based on a DLL so the user can set a delay to compensate the delay introduced by PMT voltage settings, cable lengths or particle time of flight from the interaction point to the calorimeter cells. The DLL is adjusted by means of two control voltages to ensure that systematic process or environmental variations will not affect the channel time tuning. A fully differential design of the DLL aims at reducing the switching noise produced by delay lines. The clock jitter induced by transient noise is lower than 4ps.

The design of this chip prototype is also determined by the radiation environment. The design must tolerate SEUs, SETs and SELs. The probability of SELs is reduced by increasing the distance between PMOS and NMOS transistors and inserting double guard rings between them. SEUs are avoided by implementing Triple

Modular Redundancy Registers and a fault tolerant Finite State Machine in the SPI Slave. Finally, reset signals are protected from SETs by means of glitch suppressors.

The prototype has been designed in Austriamicrosystems 0.35um SiGe BiCMOS technology, with 3.3V power supply.

Author: PICATOSTE OLLOQUI, Eduardo (University of Barcelona (ES))

Co-authors: BEIGBEDER-BEAU, Christophe (Universite de Paris-Sud 11 (FR)); GASCON, David (University of Barcelona (ES)); MACHEFERT, Frederic (Universite de Paris-Sud 11 (FR)); LEFRANCOIS, Jacques (Universite de Paris-Sud 11 (FR)); MAURICIO FERRE, Juan (University of Barcelona (ES)); DUARTE, Olivier (Universite de Paris-Sud 11 (FR)); VILASIS CARDONA, Xavier (University of Barcelona (ES))

Presenter: PICATOSTE OLLOQUI, Eduardo (University of Barcelona (ES))

Session Classification: ASICs

Track Classification: ASICs