Contribution ID: **29** Type: **Poster**

Analogue Sum ASIC for L1 Trigger Decision in Cherenkov Telescopes Cameras

Wednesday 24 September 2014 17:07 (1 minute)

An application specific integrated circuit (ASIC) has been developed for level 1 trigger decisions in Cherenkov Telescope cameras. The ASIC comprises 7 input differential analogue channels and 2 output digital differential channels. Analogue inputs are provided by the previous trigger stage implemented in the so-called L0 ASIC. The L1 ASIC computes the analogue sum of three configurable sets of inputs, and provides digital output signals when any of the sums is above configurable voltage thresholds. The analogue signal processing stage has been specifically developed for this application by means of a low noise differential architecture that provides 500MHz bandwith.

Summary

Trigger decision in Cherenkov telescopes is based in the detection of a concentration of signal both in space and time. A mixed signal L1 ASIC has been developed for analogue sum trigger implementation, in combination with a previous stage L0 ASIC.

L1 ASIC comprises 7 input differential analogue channels and two output differential digital channels. The two basic functionalities of the circuit are the calculation of the analogue sum of the input channels and the discrimination of the resulting voltage pulse in order to generate digital trigger outputs. Input pulses are replicated and connected to three analogue adders through a set of high bandwidth switches, thus, any group of signals can be summed up in any of the three adders. The output of the adders are connected to two group of discriminators, with independent threshold definition each group, in order to generate high level and low level threshold triggers. Threshold voltages are generated by two independent differential DACs. The outputs of the discriminators are combined in two OR gates, which outputs are connected to LVDS transmitters that provide the digital trigger outputs of the ASIC.

A fully differential low noise and high bandwidth architecture has been designed for the analogue signal processing stage of the circuit, which has been specifically developed for this application. It provides a bandwidth of 500MHz with around 0,2 phe noise per input. The gain of the analogue stage is near to one and the linear range is more than 1V, therefore the ASIC is able to handle signals of more than 100phe, assuming a gain of 10mV/phe at the input, with a minimum signal-to-noise ratio of 5.

Six differential leading edge voltage discriminators are used for trigger signal generation, one per adder and per voltage threshold. The transition time of the digital pulse is around 1ns and the minimum repetition time, or double trigger resolution, is 5ns. Voltage thresholds are provided by two differential voltage DACs with 10 bit resolution. The reference voltage circuit of the DACs has been designed to match the operational range of the adder in order to optimize the resolution in the threshold definition, obtaining around 1,27mV resolution, that is, around 0,1phe, and therefore below the noise level of the analogue circuit.

The slow control comprises a set of seven 16-bit registers that can be written and read by a serial link. The registers contain the data used to control the input stage switches, the DAC used to define the bias current of the differential pairs in the ASIC, the DACs for voltage threshold generation and the enable of LVDS transmitters.

A first version of the ASIC was submitted last June 2013 for manufacture in a 350nm SiGe BiCMOS Multi Project Wafer run. The preliminary results of the characterization of this ASIC are very satisfactory. A detailed

description of the architecture of the circuit and the results about functionality and performances will be shown in this contribution.

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Session Classification: Second Poster Session

Track Classification: ASICs