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High-speed, High-resolution, Radiation-tolerant SAR ADC for Particle Physics Experiments

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We present the design of a 12-bit, 160-MSPS two-step SAR ADC in 40-nm CMOS with calibration and radiation test results. The ADC measured 67.5-dB SNDR and ≥85-dB SFDR that displayed minimal degradation after being exposed to a total ionizing dose of up to 1 Mrad. The power consumption is 4.5 and 6.1 mW at 80 and 160 MSPS, respectively. The small die size also opens up good potential for single event error treatment using redundancy techniques. The experimental results reveal great potential of SAR ADC for high-energy particle physics experiments.

Summary

The 25-ns bunch crossing time of Large Hadron Collider (LHC) dictates a sample rate of at least 40 MSPS and a resolution of 12 bits for precision energy measurement. The operating conditions of LHC also require the detector front-end readout system including the ADC to be radiation-tolerant and to exhibit low-power consumption, which rule out most ADC products commercially available.

In the last decade, great progress has been made for the switched-capacitor successive-approximation-register (SAR) ADC for mainstream deployment at 12-14 bits, 50-200 MSPS. The intrinsic advantages of SAR including a scaling-friendly architecture, low-power consumption, in conjunction with a small die size have all made SAR the preferred choice for system-on-a-chip (SoC) integrations. In addition, the built-in redundancy and digital calibration have also lifted many critical limiting factors on the SAR architecture, such as the conversion speed and on-chip matching accuracy of monolithic metal capacitors.

This paper reports the design of a 12-bit, 160-MSPS two-step SAR ADC in 40-nm CMOS and its irradiation testing results. The ADC is partitioned as a 5b+8b two-step structure with one-bit inter-stage redundancy. Aided by the digital background calibration, the total input capacitance of the first stage is reduced to the thermal noise limit, yielding a wide input bandwidth and fast sample rate. In experiments, the prototype SAR ADC measured a near 68-dB SNDR and a ≥85-dB SFDR. When exposed to a total ionizing dose (TID) from 0 to 1.0 Mrad, the measured SNDR degraded no more than 0.5 dB and the SFDR degraded no more than 4 dB in the worst case. The total ADC power consumption remains nearly constant at 4.5 and 6.1 mW at 80 and 160 MSPS, respectively.

The positive TID results make it possible to design SAR ADCs in deeply scaled processes for short-term radiation effect cure, e.g., treating the single event upset (SEU) without additional process requirements. For example, the most vulnerable digital logics can be replicated to combat soft errors by applying a majority voting algorithm. Reliable quantization results can be obtained with low error probabilities using digital and analog redundancy techniques. The small die size and low power of SAR also leave ample room for the redundancy circuitry without much additional area or power cost.

In summary, the low-power consumption, small chip area, increasing conversion speed, and enhanced resolution and linearity of SAR ADC bode well for high-energy particle detector applications. The TID testing results confirm its benign property of long-term radiation tolerance and opens up great potential for treating short-term radiation effects using redundant circuit techniques.

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