Contribution ID: **0** Type: **Oral**

TDCPix: Tracking for the NA62 GigaTracker

Tuesday 23 September 2014 09:50 (25 minutes)

The TDCPix is a hybrid pixel detector readout ASIC designed for the NA62 GigaTracker detector. The asynchronously operating pixel array consists of 1800 pixels, each 300x300μm^2. The requirements are a single-hit timing resolution better than 200ps RMS and read-out efficiency of 99% or better. The time-walk effect is compensated by in-pixel time-over-threshold discriminators connected to an array of 720 TDC channels. The TDCpix processes up to 80 Mhits/cm^2 and provides the hit data without need of a trigger in a continuous data stream via four 3.2Gb/s serialisers.

Summary

The TDCPix is a hybrid pixel detector readout ASIC designed for the NA62 GigaTracker detector. The driving requirements are a single-hit timing resolution better than 200ps RMS and a hit loss of less than 1% in the presence of a (highly non-uniform) beam rate up to 80MHz/cm^2. This hit rate leads to an expected data rate at the output of the chip which can reach 6Gb/s.

The TDCPix comprises an asynchronously operating pixel array with 1800 pixels organised as 40 columns of 45 pixels, each one 300x300μm^2. The front end input stage has been optimised for a detector capacitance of 250fF and the predicted ENC with the fully depleted detector is better than 250e^-. The base-line detector is expected to be a standard P-on-N planar pixel detector 200μm thick, although the front end remains programmable such that other detector technologies may be evaluated. The pre-amplifier was designed with a peaking time of 5ns to provide the required timing performance. Rather than distribute a high precision reference signal to the pixel array, the discriminated hit signals are driven to the end of column region via dedicated transmission lines. There, each column is instrumented with a 720 channel Delay Locked Loop based time-to-digital converter (TDC) with a nominal bin size of 97ps. The TDC measures both the discriminator leading and trailing edge times permitting a time-over-threshold approach to the required discriminator time-walk correction.

Hits from the TDCs are sent to data buffering and concentrating logic. The read-out uses four 3.2Gb/s serialisers with the high speed clock being provided by a low-noise on-chip Phase Locked Loop. The high data rates negate the possibility of buffering the data stream whilst awaiting a trigger, thus a self triggering architecture with continuous data readout has been adopted.

All configuration and state logic in the design deemed critical for the correct operation of the chip has been triplicated to provide increased single event effect tolerance. On-chip digital-to-analogue converters provide threshold generation and trimming and are configurable through a single-signal configuration interface. The configuration and DAQ interfaces include a DC-balanced protocol layer permitting direct optical connections when the detector assembly is installed in the experiment. Dedicated calibration circuitry is included to enable the required timing resolution to be reached.

The chip was manufactured in a commercial 130nm process during the second half of 2013 and testing began at the start of 2014. Bump bonding of the TDCPix chip to a P-on-N detector is currently being scheduled.

A detailed description of the ASIC architecture and performance will be presented alongside results from the single chip assembly, if it becomes available in time.

Primary author: NOY, Matthew (CERN)

Co-authors: KLUGE, Alex (CERN); Dr AGLIERI RINELLA, Gianluca (CERN); KAPLON, Jan (CERN); POLTORAK, Karolina (AGH University of Science and Technology (PL)); PERKTOLD, Lukas (Graz University of Technology (AT)); PERRIN-TERRIN, Mathieu (CERN); MOREL, Michel (CERN); BONACINI, Sandro (CERN)

Presenter: NOY, Matthew (CERN)

Session Classification: ASICs

Track Classification: ASICs