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The CMS HCAL FEE Control Module

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In the CMS Hadron Calorimeter, the Clock Control Module distributes the system clock to the readout modules and supports control and monitoring of the front-end electronics. This year an upgrade prototype, called ngCCM, has been built and used for a beam-test of the upgraded Forward HCAL. The ngCCM uses a 4.8 Gbps GBT-like optical link to the counting room along with a redundant mechanism in case the primary link fails. Notably, it is possible to reprogram FPGAs in the front-end via the GBT link. We describe the ngCCM and its integration within the Forward HCAL.

Summary

The upgrade prototype ngCCM for the Forward Hadron Calorimeter (HF) is a 6U/6HP sized Eurocard board. It is to be installed in an environment with moderate levels of radiation and magnetic field, in the middle of a 14-slot Eurocard chassis with custom backplane and surrounded by readout modules and a calibration module. It provides the clock from the counting room to these modules and provides a path by which the counting room can control and monitor these front-end electronic modules. The ngCCM consists of two boards, a mother-board and a mezzanine board. In the first prototype iteration, the mezzanine board is a GBT emulator designed into a Xilinx Virtex-5 and handles the 4.8Gbps optical link with the counting room. The connector between the mezzanine and the motherboard supports bidirectional data transfer using differential SLVS or LVDS sig-nalling. This non-rad-tol mezzanine design was required in order to support system-level tests performed at the Fermilab Test Beam Facility. The tests were completed successfully. A rad-tol mezzanine, currently under development, will use a Microsemi Igloo2 FPGA to support the GBT-like optical link. The motherboard hosts the mezzanine board and provides the interface to the backplane. Multiple Microsemi ProASIC3L FP-GAs are used to translate the SLVS/LVDS differential signals from the mezzanine and they also contain logic for accessing on-board ADCs which are used to monitor system temperatures and voltages. CERN-developed AMIS5MP DC/DC converters are used to provide the needed voltages. New features were added with the upgrade electronics. One exciting feature is the ability to reprogram over the optical link the FPGAs in the readout modules and the FPGAs in the ngCCM itself. This will allow updates to the HF electronics without requiring physical access. Another feature is the addition of circuitry to support a secondary path for the clock and data. The secondary path consists of optical links that connect pairs of ngCCMs in different chassis. If the primary link of either ngCCM fails, the ngCCM with a working primary link can forward the clock and data to the other ngCCM. The switch-over between primary and secondary links is controlled directly by level-sensitive signals from the counting room. The secondary clock is directly multiplexed with the primary clock on the ngCCM. The secondary data path is handled by a Microsemi Igloo2 FPGA. This secondary link supports most features of the primary link but with added data latency. The only feature not supported by the secondary link is the reprogramming of FPGAs. The motherboard was designed to be radiation tolerant by using mostly commercial components that have been observed in the past to have good performance in the expected environment of the HF electronics. Once a radiation tolerant mezzanine board is available, radiation testing will be conducted to verify the radiation tolerance of the ngCCM. We present the upgrade prototype ngCCM design, production testing and integration in the ongoing CMS HF phase-1 upgrade project.

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