Front End Electronics for SOI Monolithic Pixel Sensor

T. Miyoshi, Y. Arai, Y. Fujita, K. Hara[1], S. Honda[1], Y. Ikegami, Y. Ikemoto, I. Kurachi, S. Mitsui, A. Takeda[2], K. Tauchi, T. Tsuboyama, M. Yamada

High Energy Accelerator Research Organization (KEK)
[1]Univ. of Tsukuba
[2]Kyoto University

23/9/2014 (Tuesday)
11:35 - 12:00
ASICs

v.3

Outlines

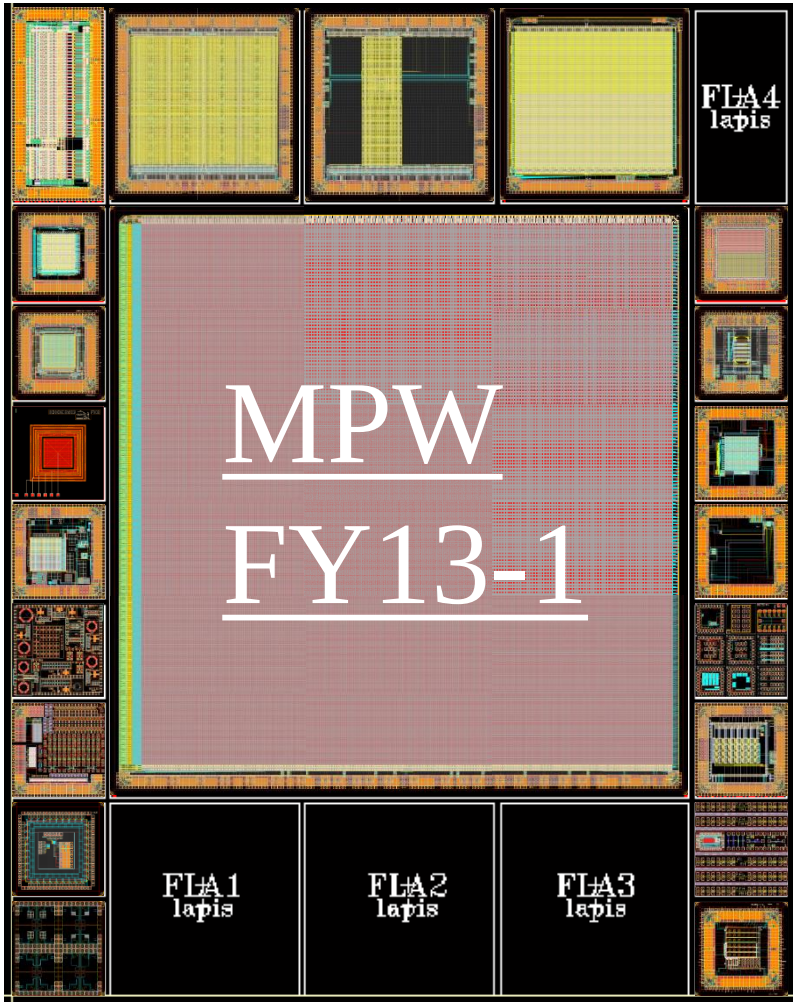
Introduction

Progress of SOI sensors

Sensor layout
Pixel layout and circuit

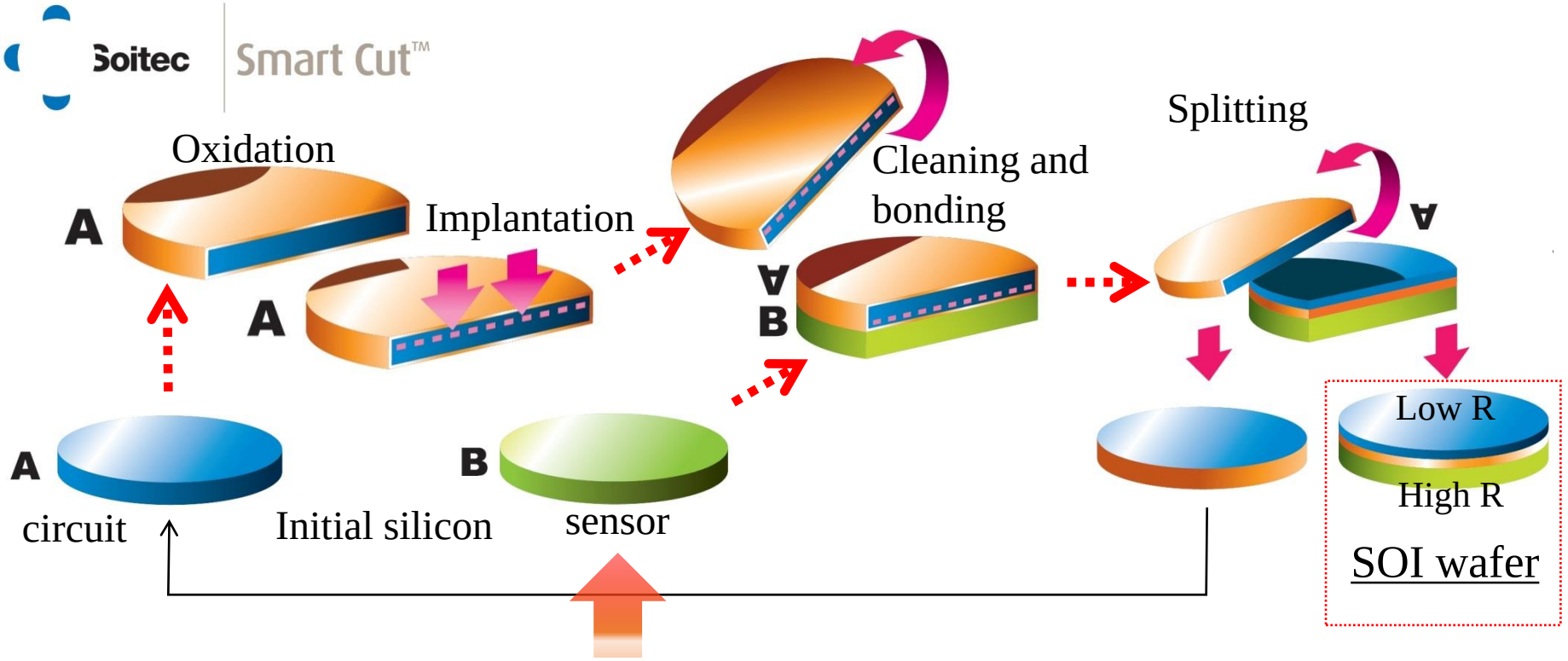
Current issues and solutions

Future plan and summary



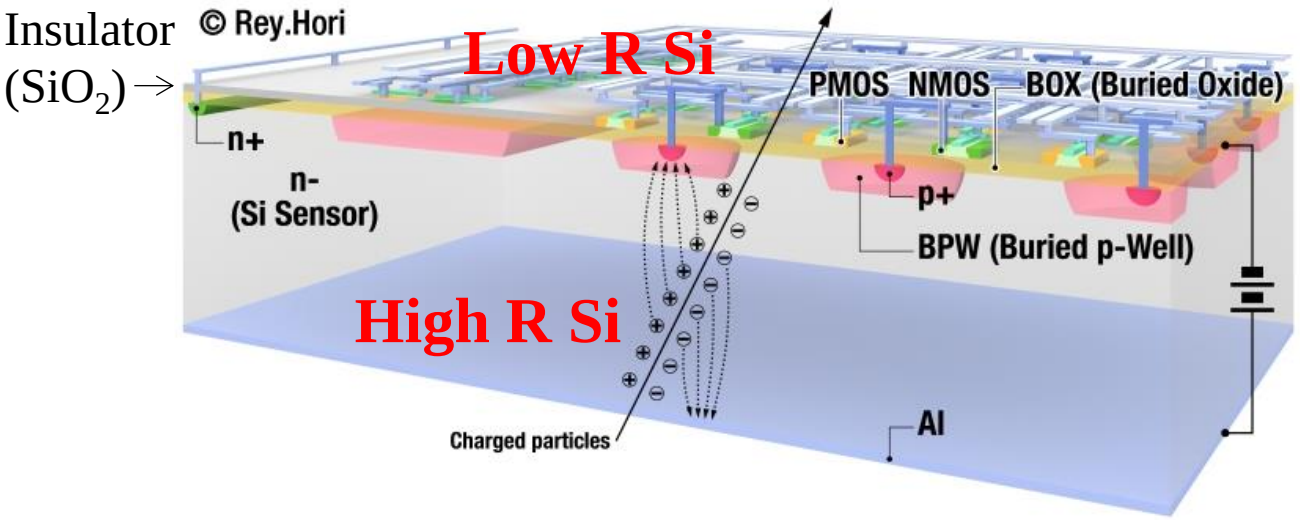
SOI Wafer for monolithic sensor

Smart cut™ by Soitec



High Resistivity Silicon: Two choices
N-type Czochralski, NCZ, 700 Ohm-cm, 300 μm-thick
N-type Float Zone, NFZ, 2-7k Ohm-cm, 500 μm-thick

SOI Monolithic pixel sensor

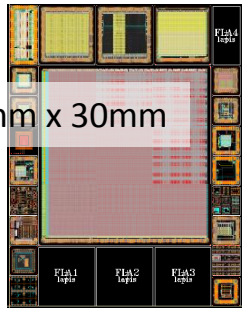


Targets
High-Energy Physics
X-ray astronomy
Material science
Non-Destructive inspection
Medical application

The features of SOI monolithic pixel sensor

- No mechanical bump bonding. Fabricated with semiconductor process only
- Fully depleted (thick & thin) sensing region
  with low sense node capacitance (~10 fF@17 μm pixel) → high sensor gain
- SOI-CMOS; Analog and digital circuit can be closer → smaller pixel size
- Wide temperature range (1-570K)
- Low single event cross section
- Technology based on industry standards; cost benefit

Process Summary



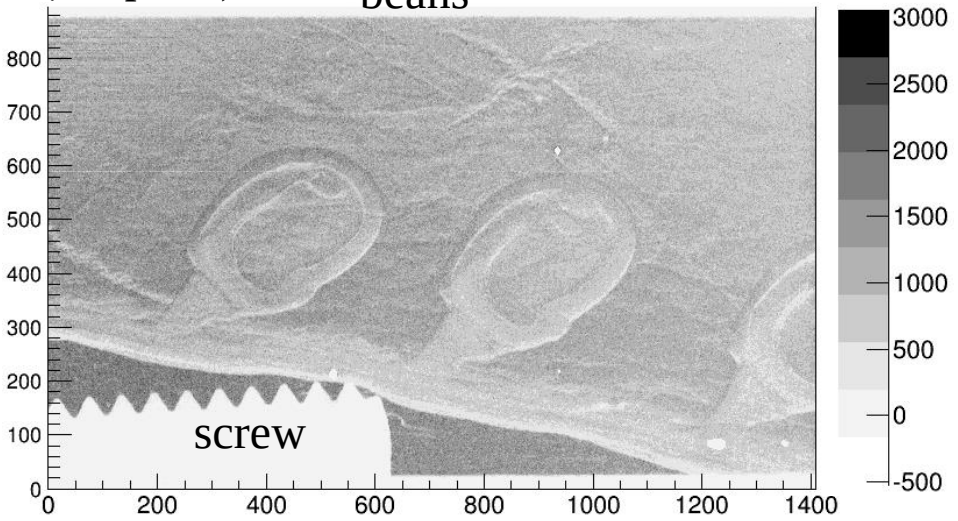
- KEK organizes MPW runs twice a year
- Mask is shared to reduce cost of a design
- Including pixel detector chip and SOI-CMOS circuit chip

Process (Lapis Semiconductor Co. Ltd.)	0.2μm Low-Leakage Fully-Depleted (FD) SOI CMOS 1 Poly, 5 Metal layers (MIM Capacitor and DMOS option) Core (I/O) voltage : 1.8 (3.3) V
SOI wafer (200 mm ϕ =8 inch)	Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer thickness: 725 μm → thinned up to 300 μm (Lapis) or ~50 μm (commercial process) Handle wafer type: NCZ, NFZ, PFZ, double SOI
Backside process (2011~)	Mechanical Grind →Chemical Etching →Back side Implant →Laser Annealing → Al plating

Progress of SOI monolithic sensors

Integration-type pixel sensors

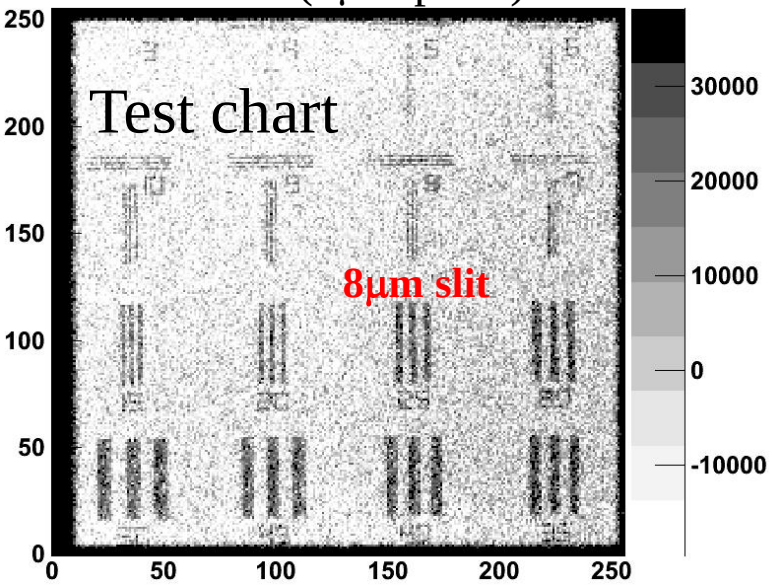
(12μm pixel)



X-ray phase-contrast image (INTPIX5)
16 keV monochromatic

(8μm pixel)

X-ray tube
Target:Cr

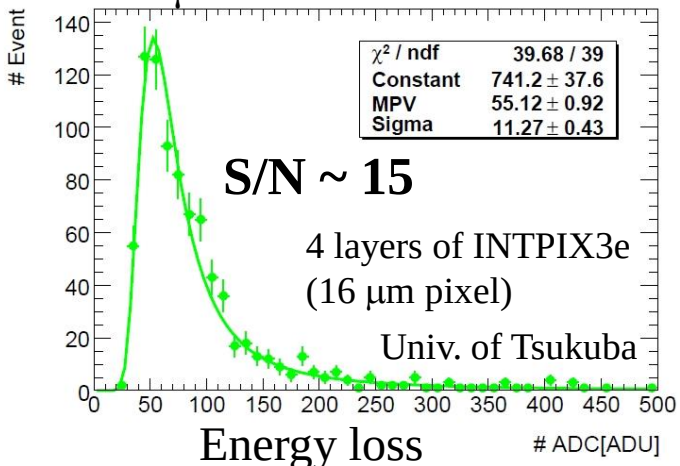


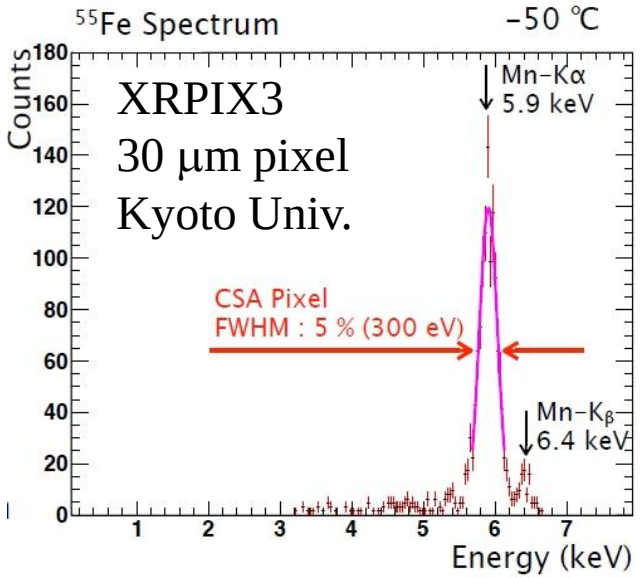
X-ray image (FPIX)

CERN beam test in 2011

CERN SPS NORTH H4-H6
π+ 55%, p 39%, K 5%

50μm-thick CZ INTPIX3e

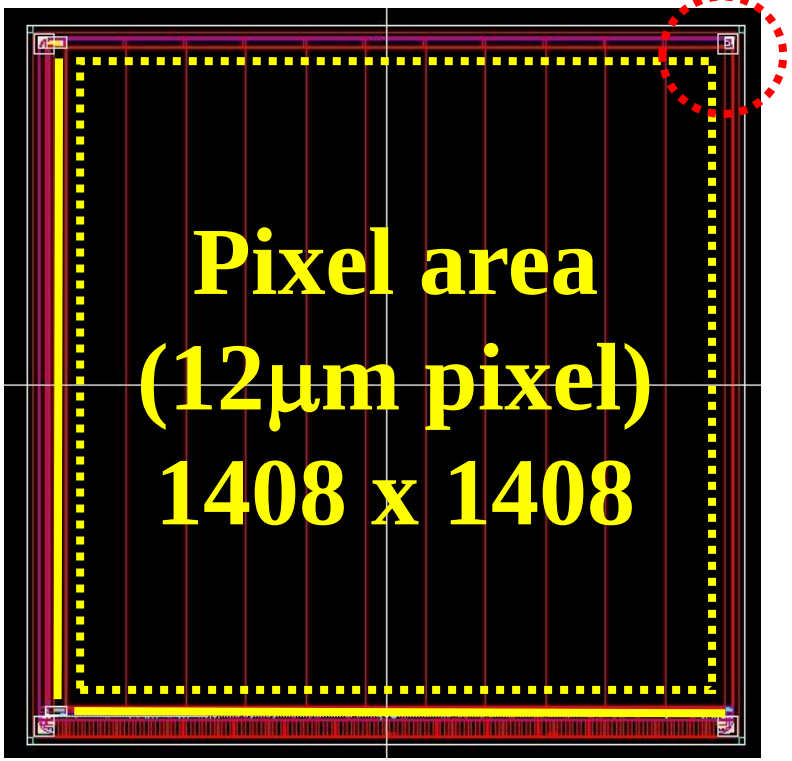


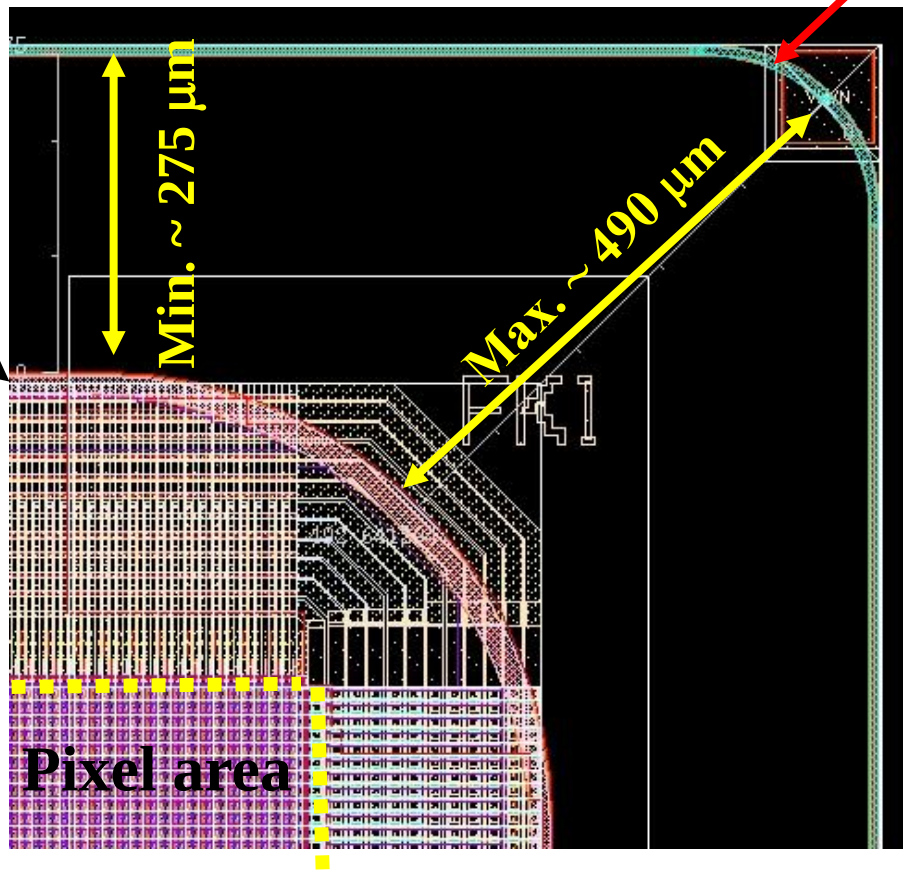


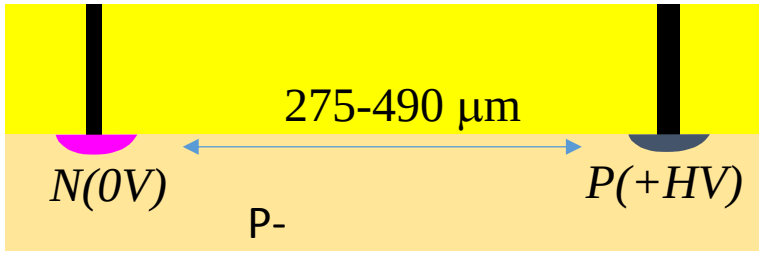
An example of Sensor layout (1)

INTPIX7 (MPW FY13-1)

Integration-type pixel sensor





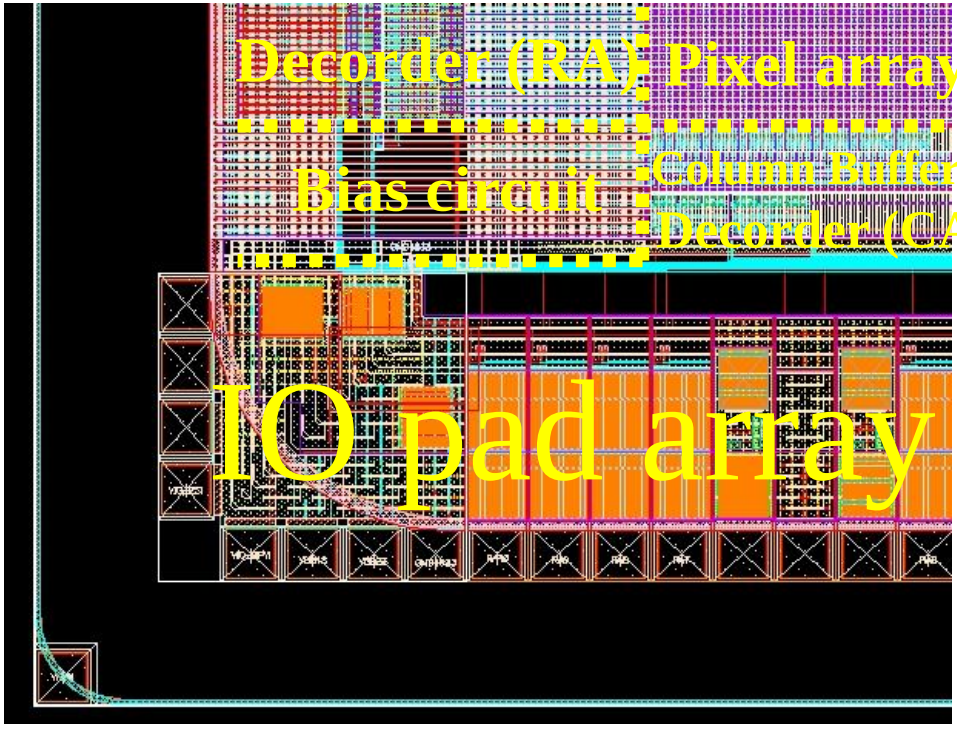


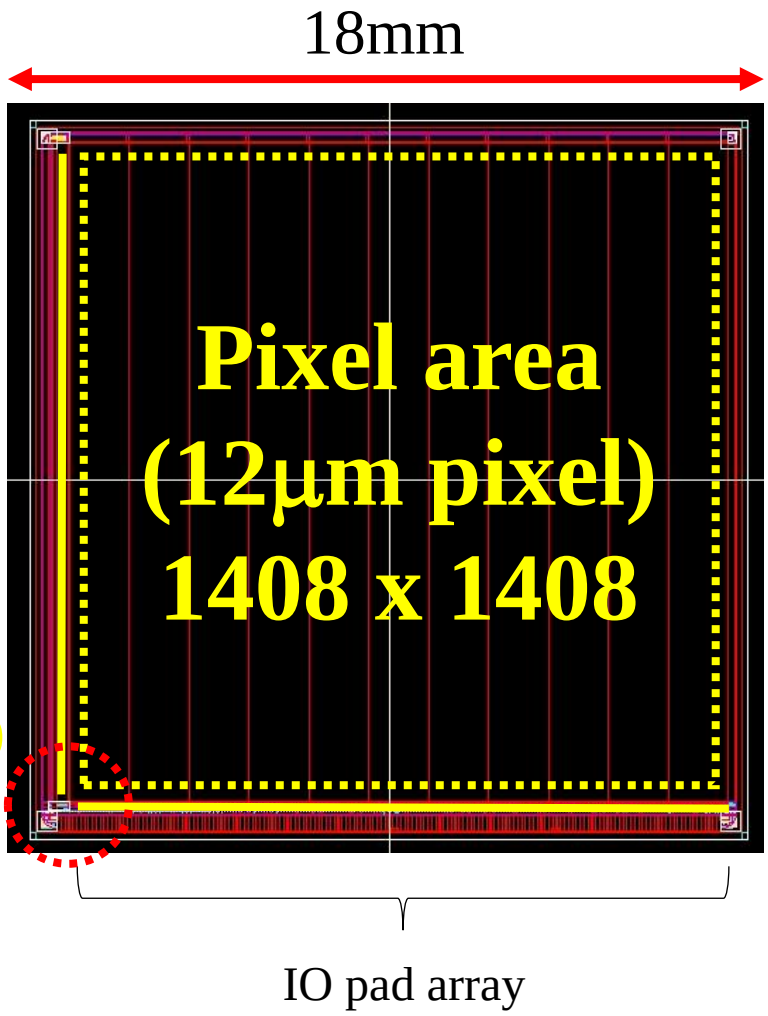
Enge of the chip (side view)

An example of Sensor layout (2)

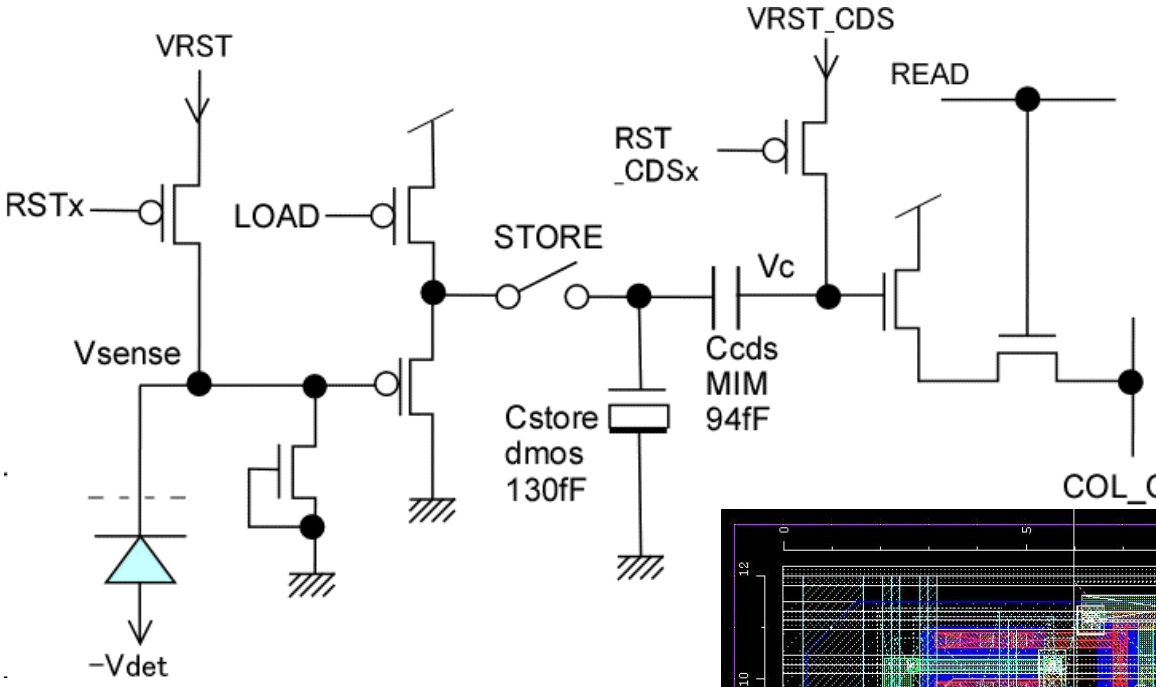
INTPIX7 (MPW FY13-1)

- Pixel array
- Raw Address (RA) decoder
- Column Address (CA) decoder
- Column buffer, analog buffer,
- Bias circuit





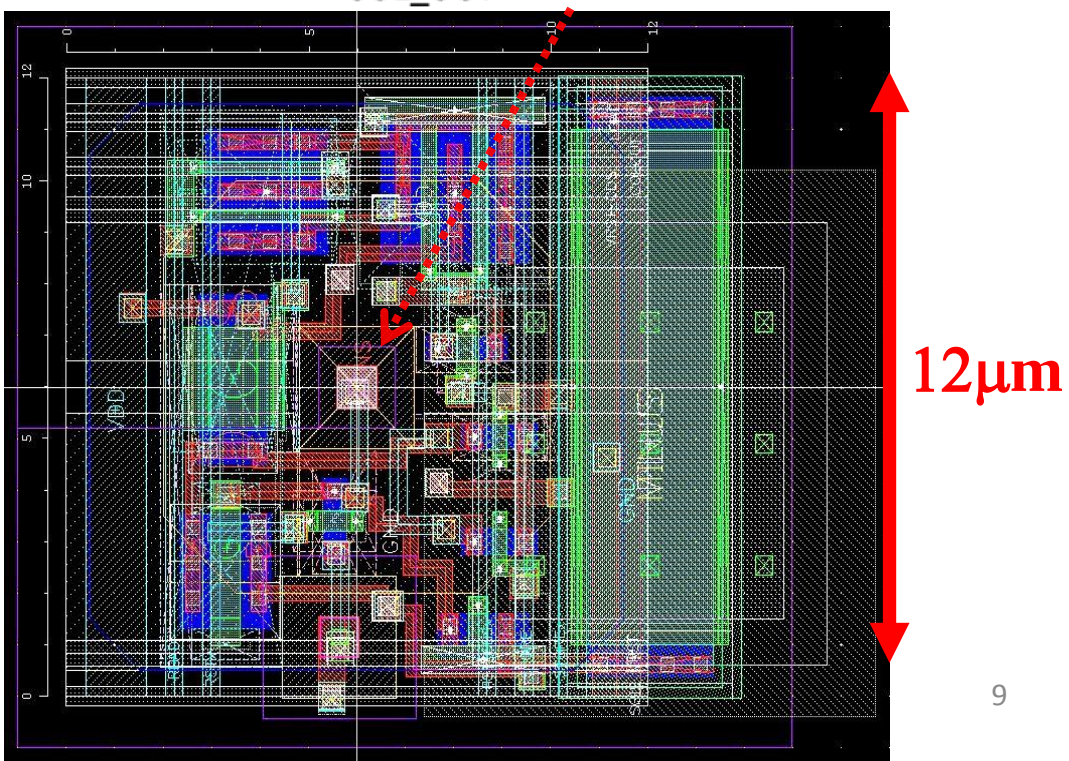
Pixel layout and circuit (1) INTPIX7



Pixel size 12μm
CDS circuit in pixel

Sense node 1
+
Transistor 9
+
MIM capacitor 1

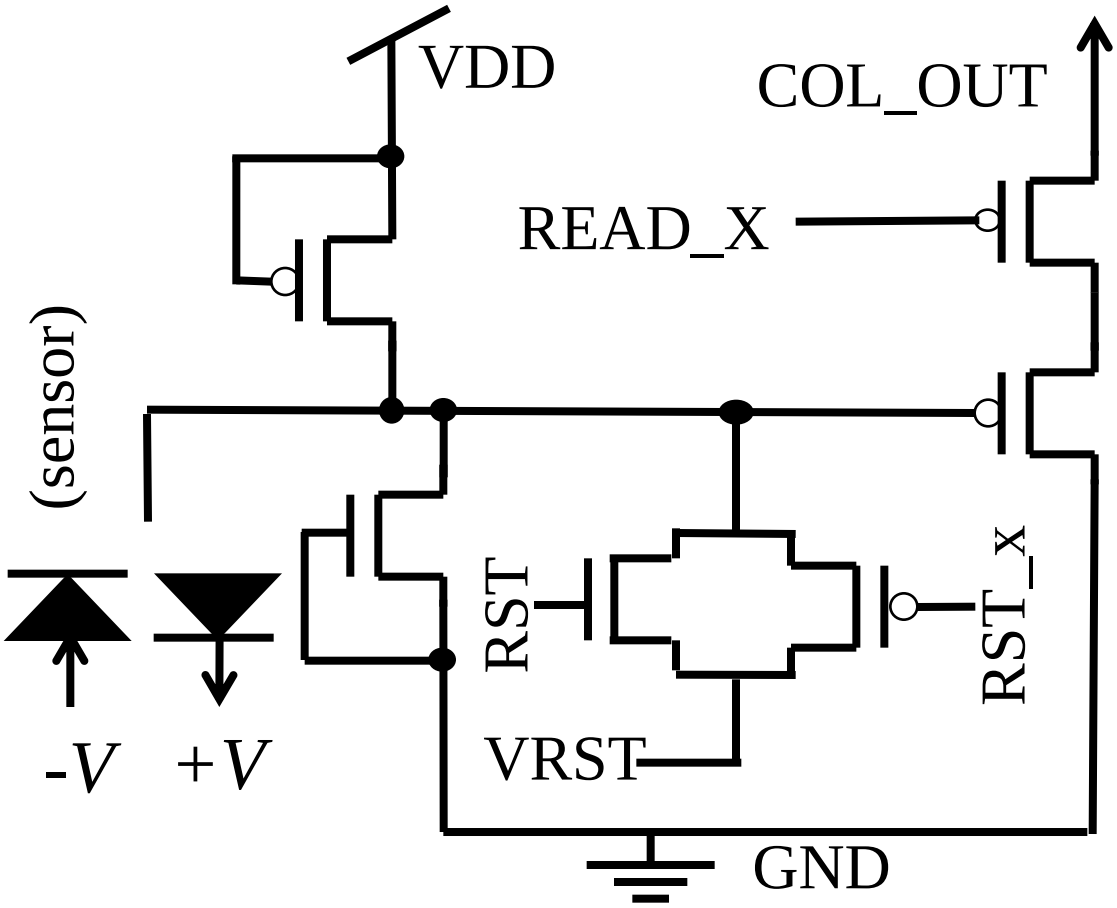
in 12 μm^2

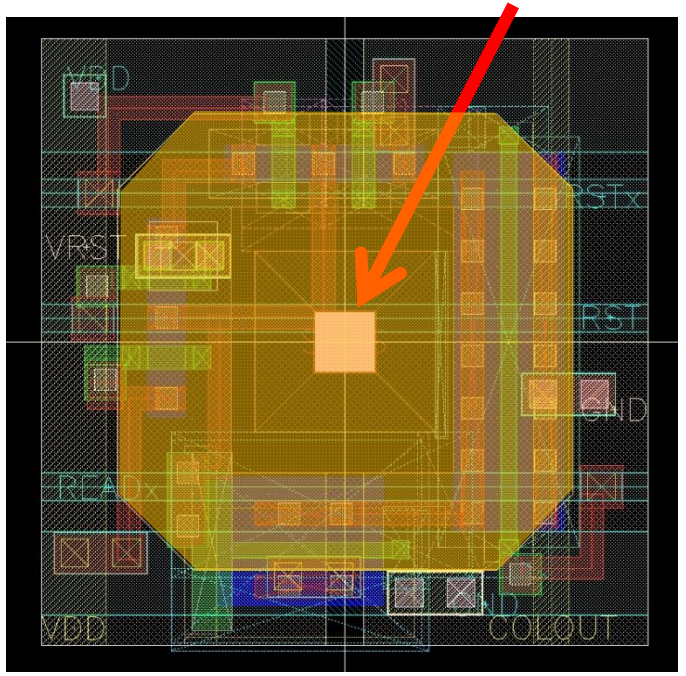


Pixel layout and circuit (2) FPIX

Pixel size 8μm

No STORE, no storage capacitor





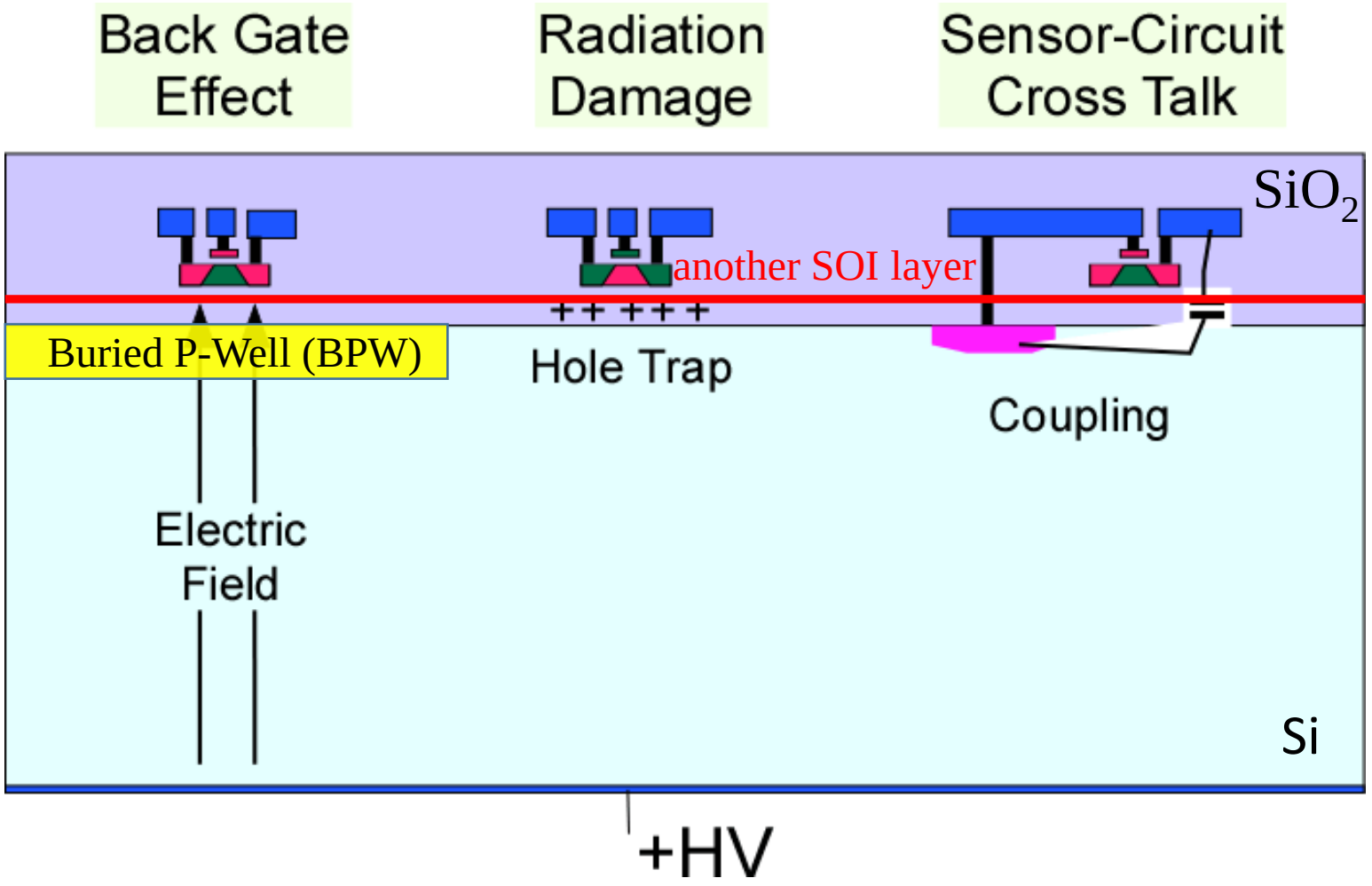
8μm

Sense node 1+Transistor 6

In 8 μm^2

Min. distance between sense node and transistor ~ 1μm

Current issues and solutions

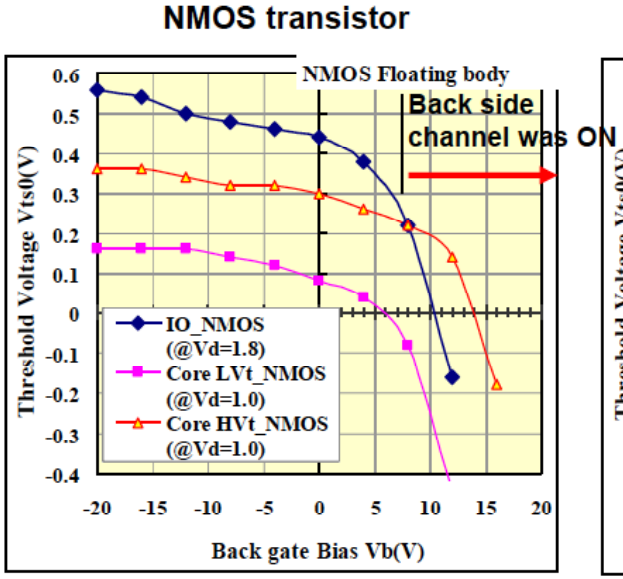


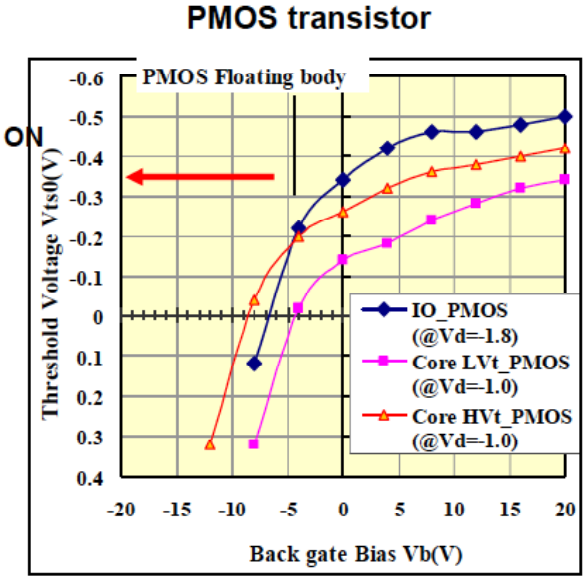
1. BPW process : effective to analog circuit in a pixel

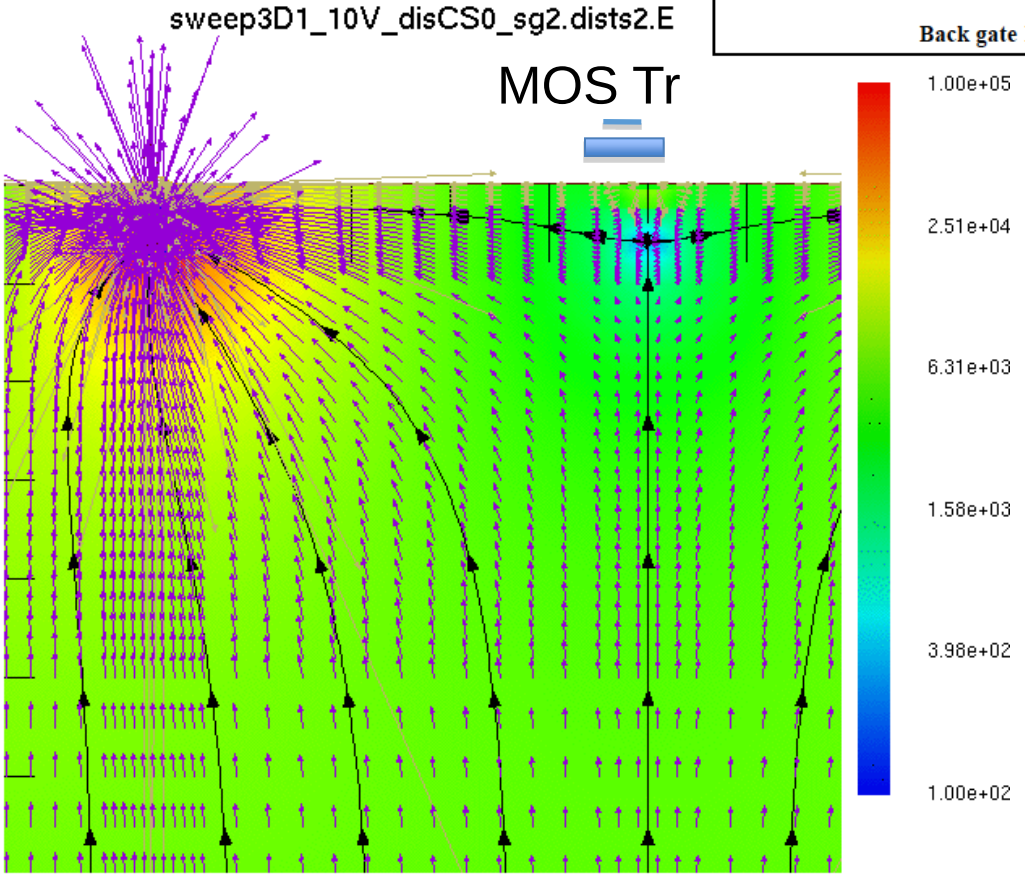
2. Double SOI wafer : effective to digital circuit in a pixel

Back-gate effect

TCAD simulation
HyENEXSS (TAC, Japan)





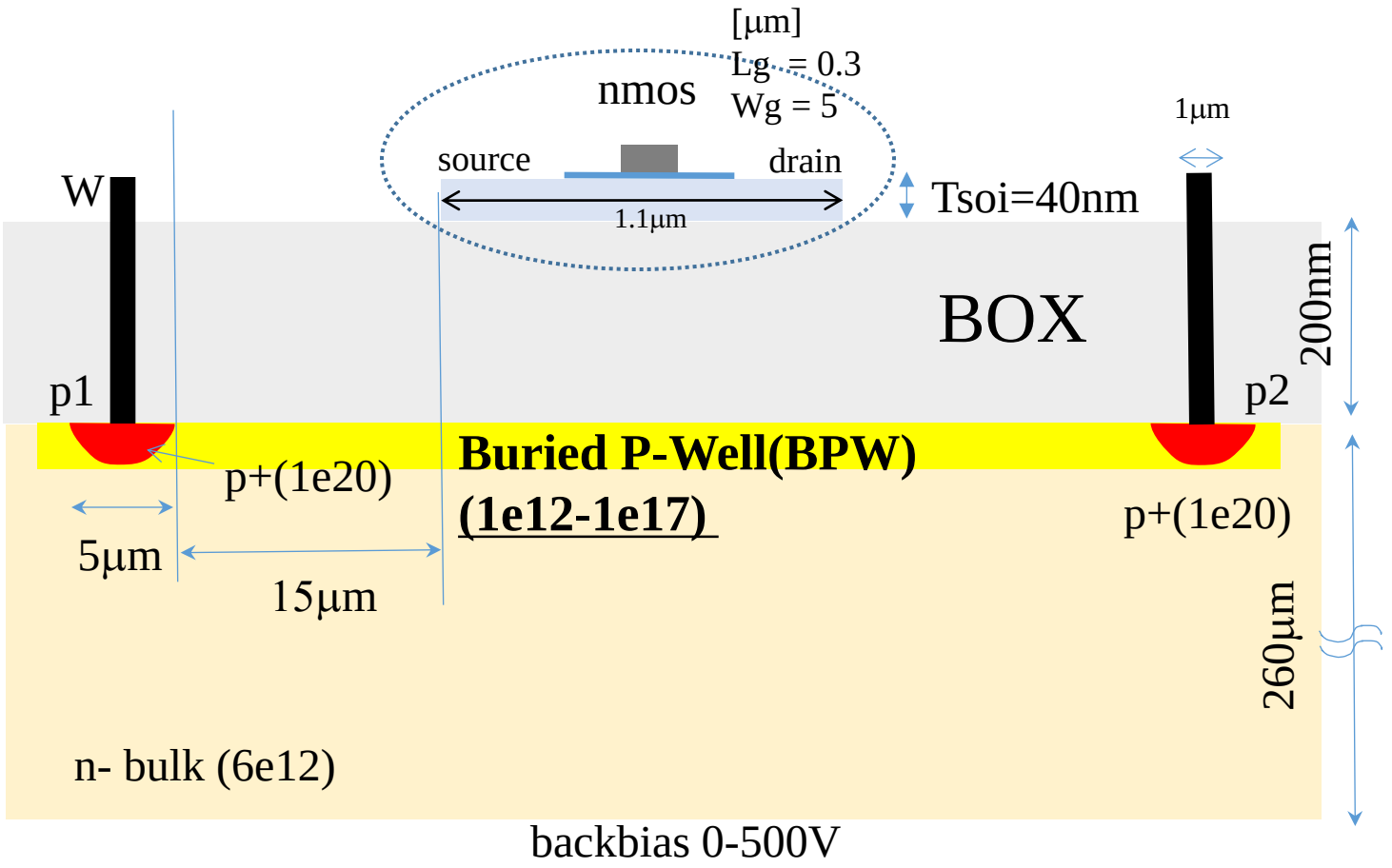


Threshold Variation

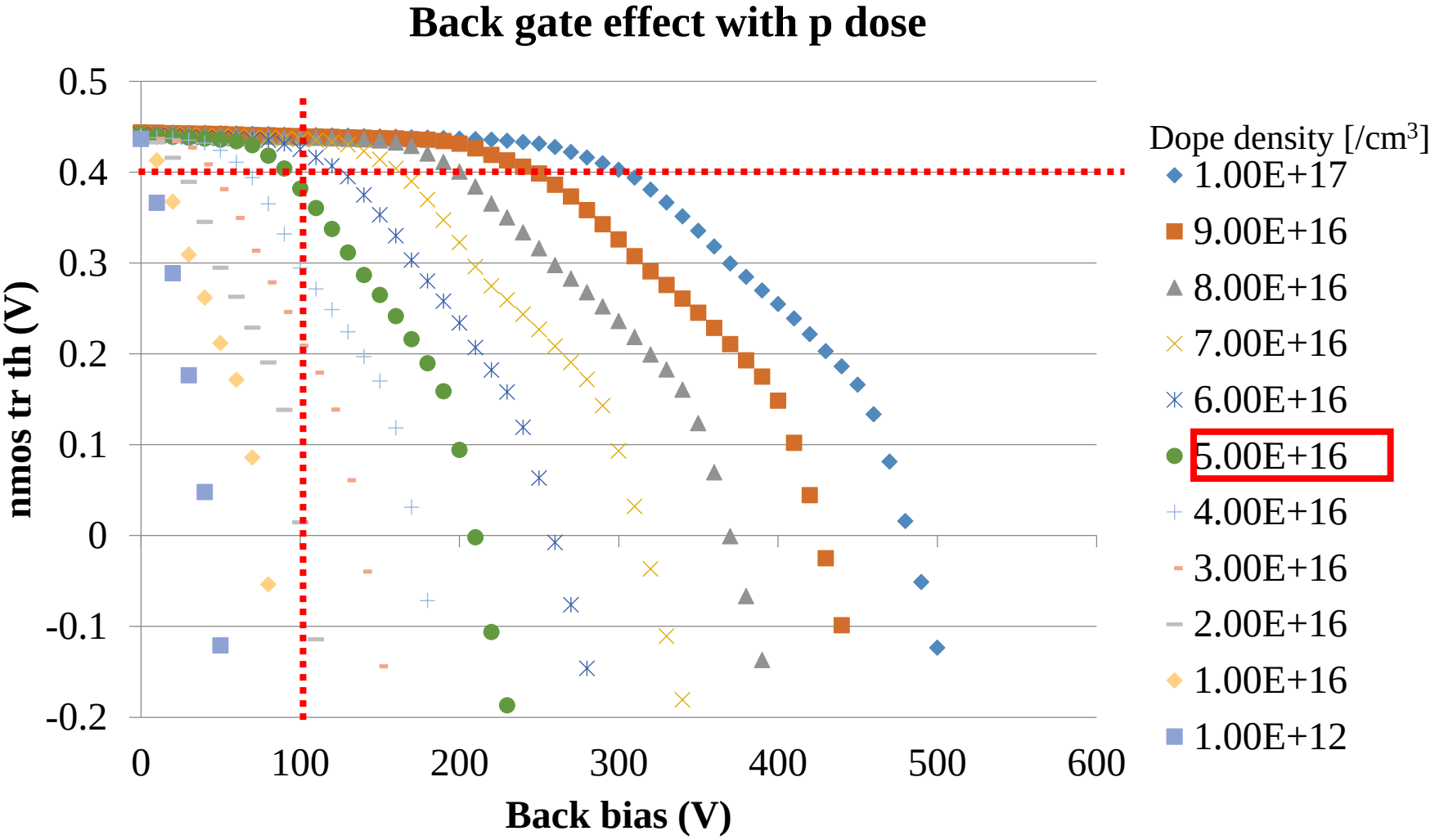
Substrate Voltages act as Back Gate, and change transistor threshold.

Geometry of TCAD simulation for BPW effectiveness study

Dope density [/cm^3]



Simulation result for BPW effectiveness study

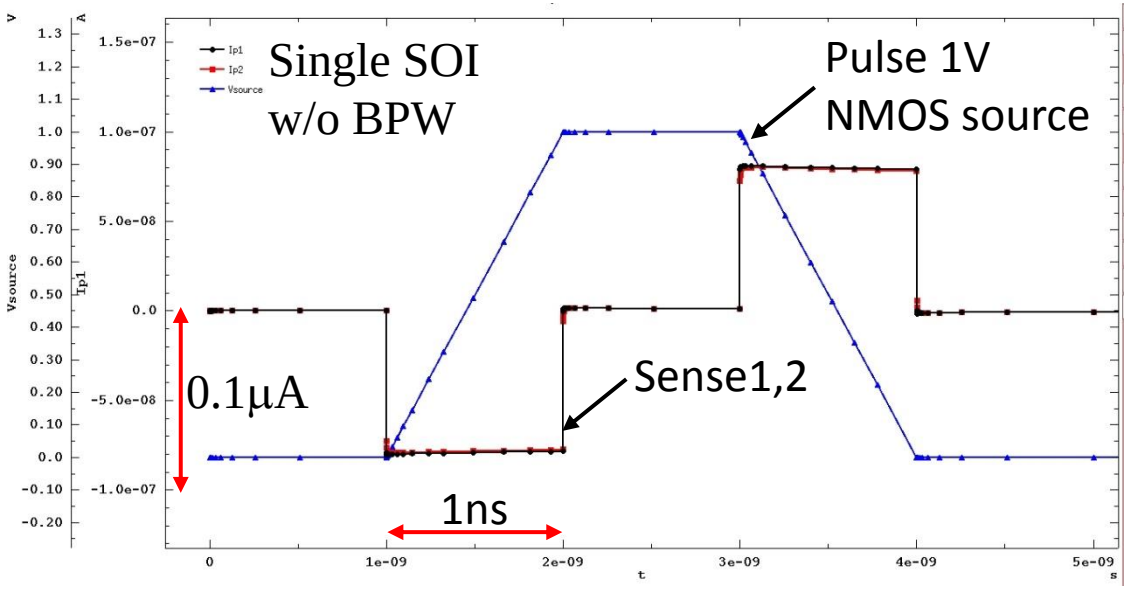


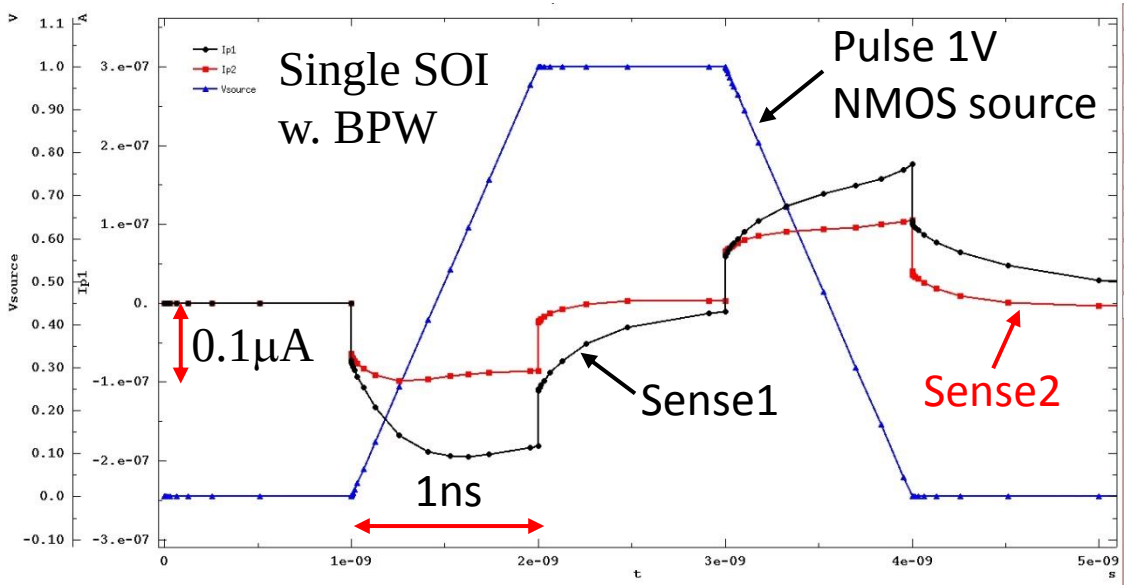
"Vth>0.4V" @ back bias > 100 V → p dose > 5e16

Increase of maximum voltage in which tr. works

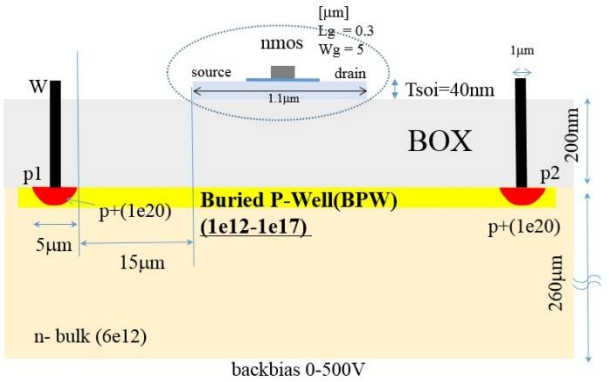
Transition analysis

Crosstalk study (TCAD Simulation)





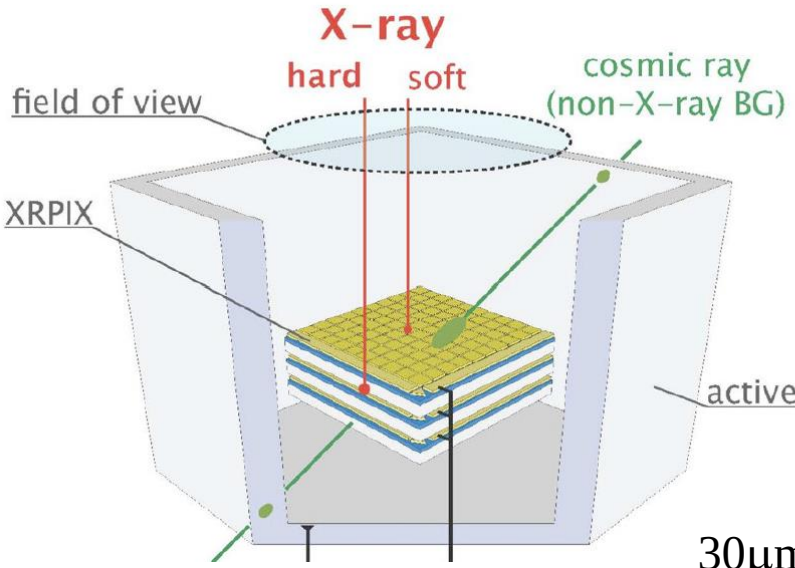
Blue: *Vsource*
Black: *Ip1*
Red: *Ip2*



Crosstalk increase by BPW

An example of crosstalk observation (XRPIX2/2b,3/3b)

TIPP2014
A. Takeda
(Kyoto Univ.)

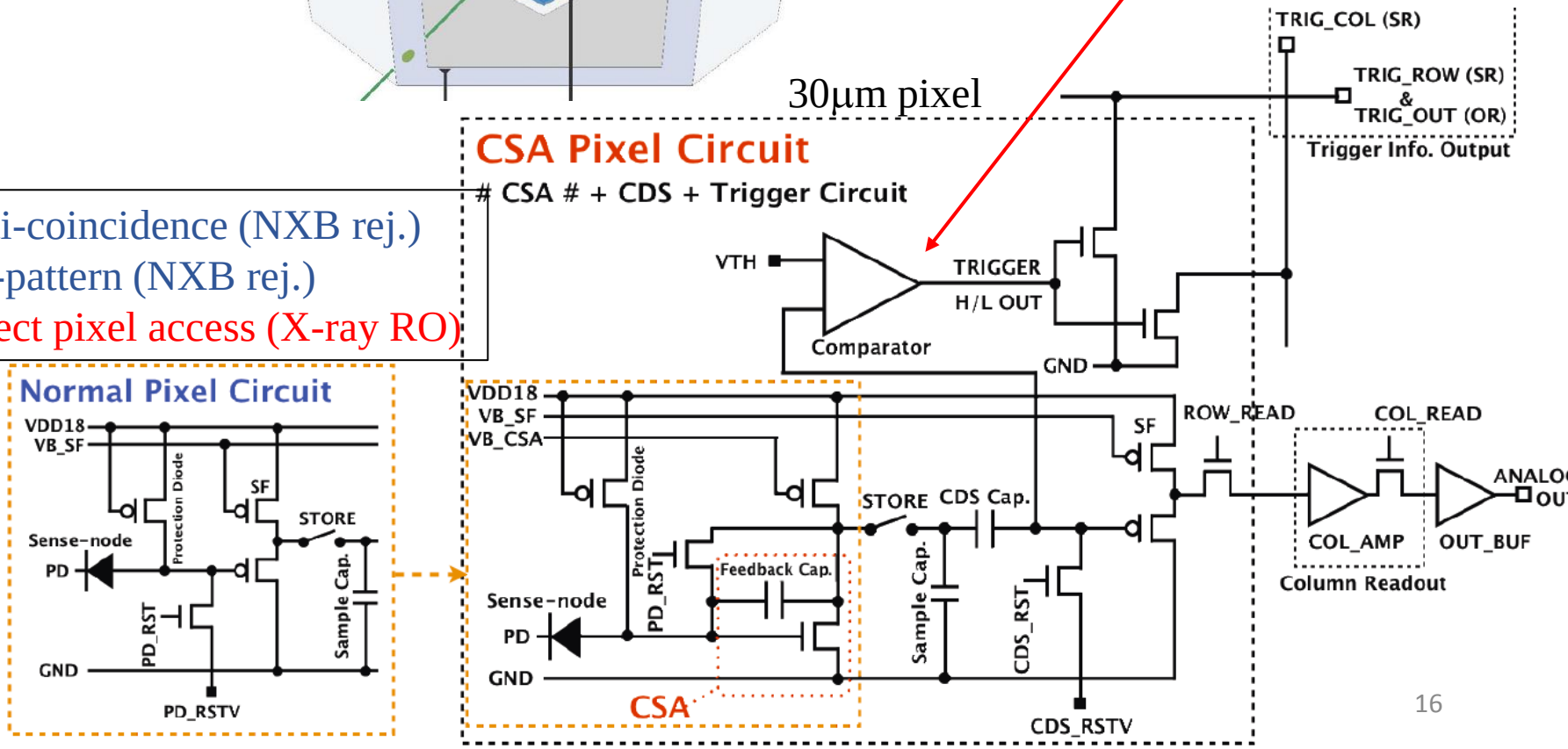


For X-ray astronomy
Event-driven R/O circuit

Comparator in pixel

30μm pixel

Anti-coincidence (NXB rej.)
Hit-pattern (NXB rej.)
Direct pixel access (X-ray RO)

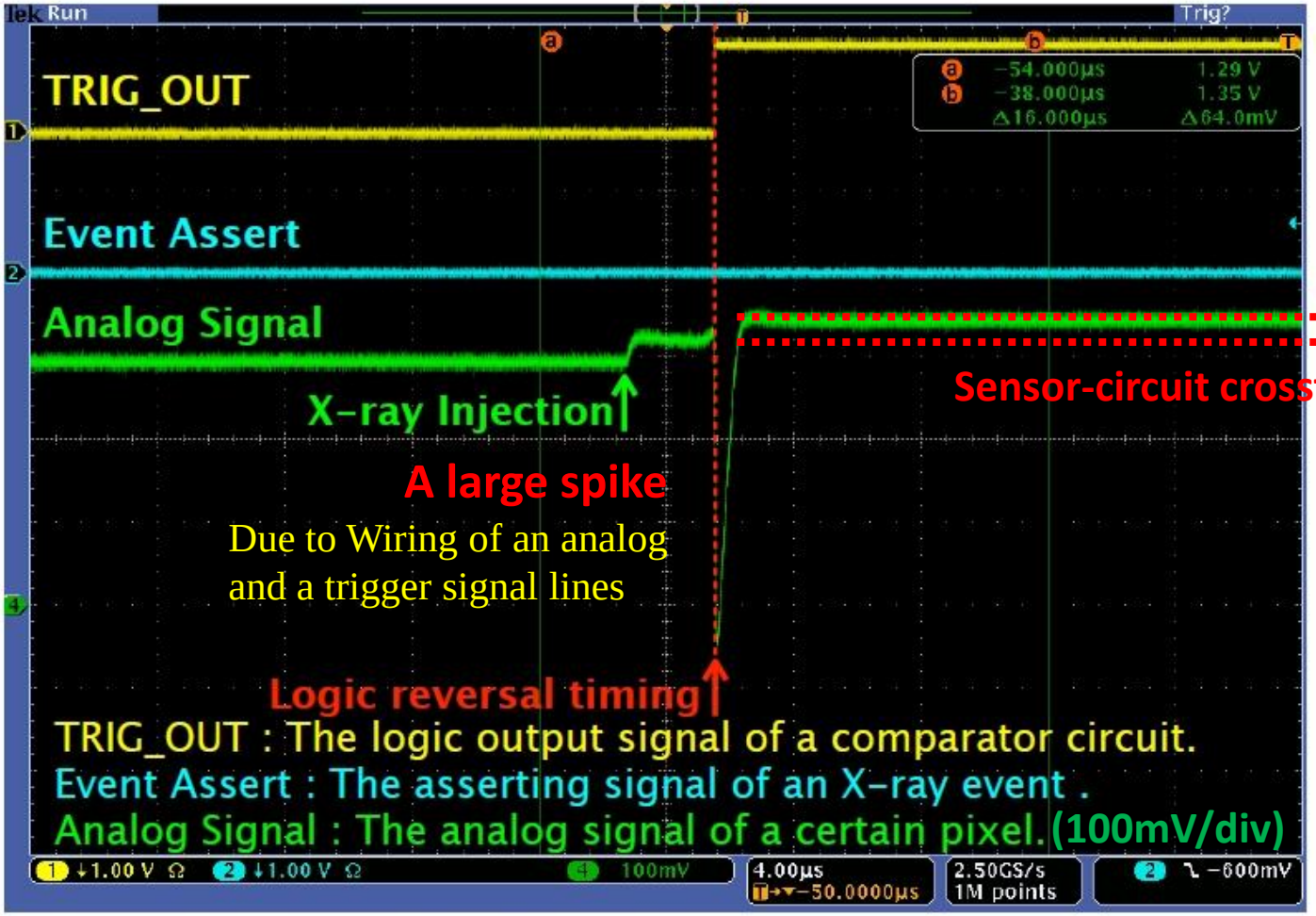


An example of crosstalk

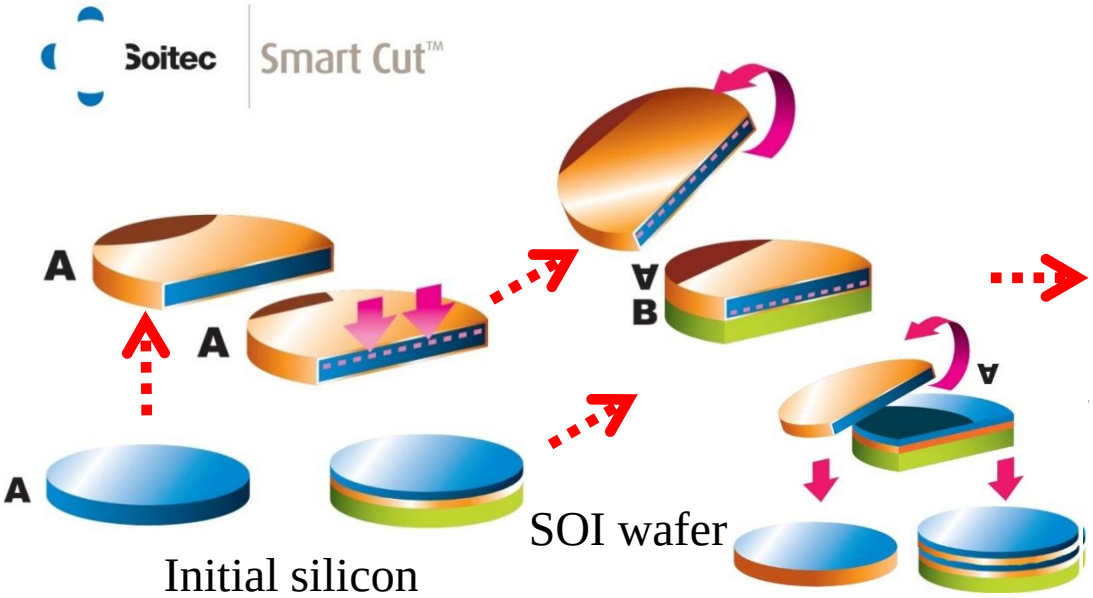
A. Takeda,PIXEL2014

XRPIX2/2b (Kyoto Univ.)

– The waveform of an oscilloscope when X-rays enter (^{109}Cd : 22.2 keV).

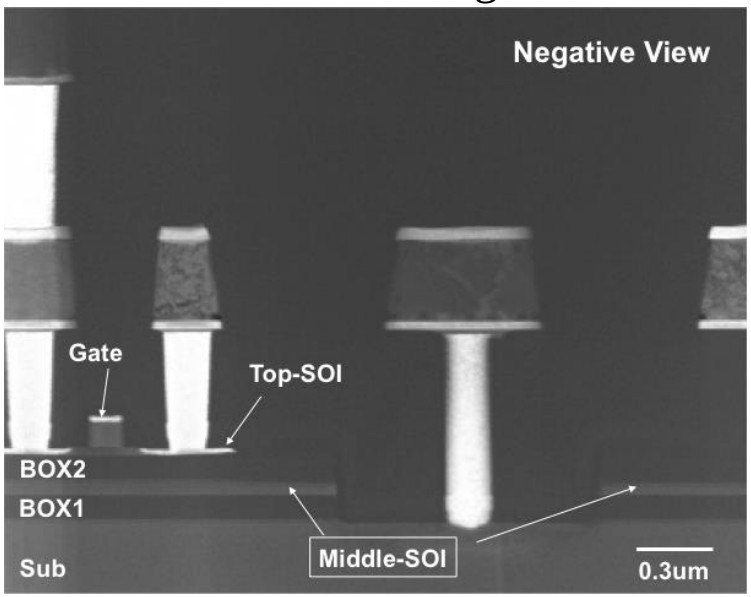


Double SOI pixel sensor



* Substrate: NCZ or PCZ wafer

STEM image

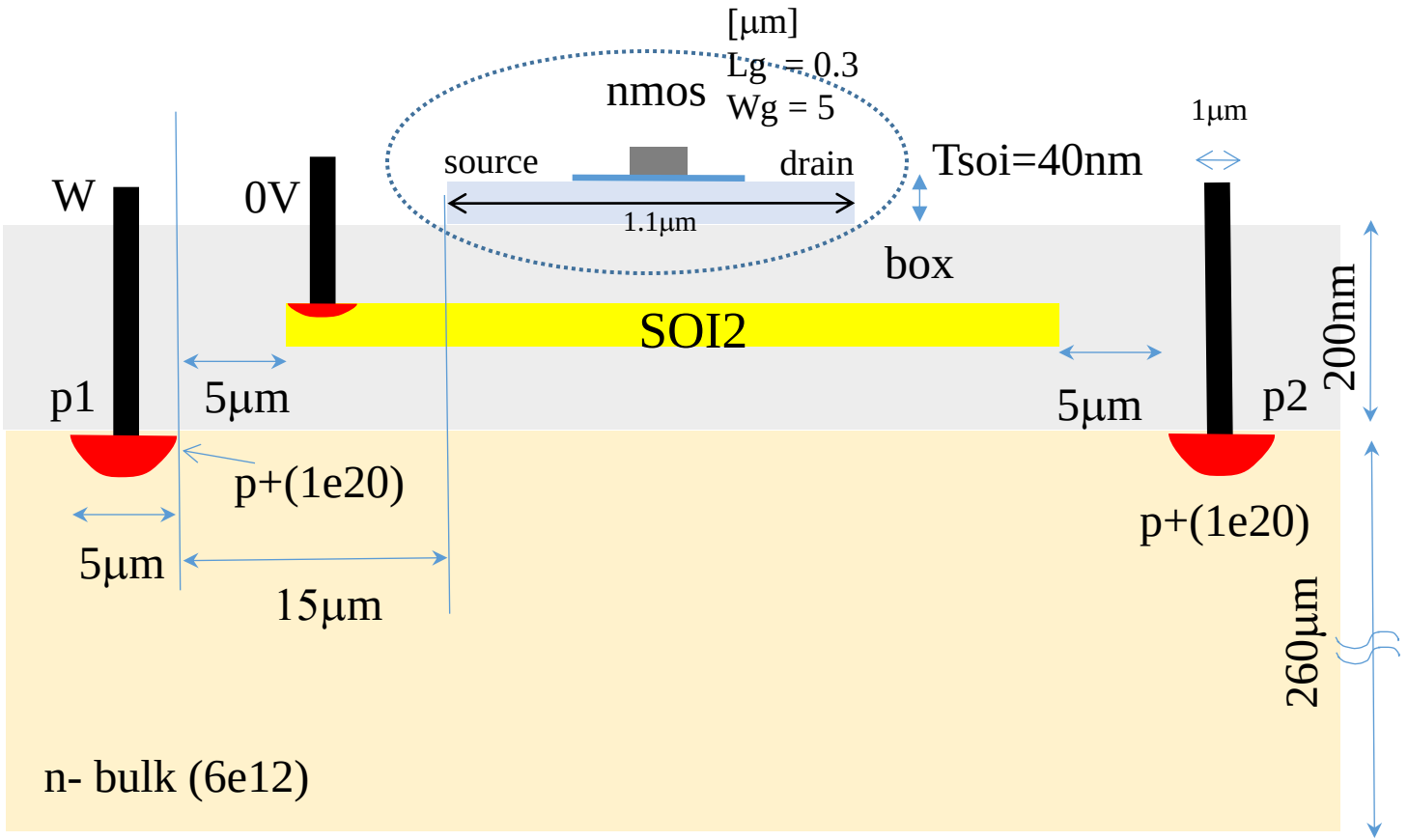


Additional shield layer

Shield the back gate effect
Compensate effect of box charge
Shield the sensor to circuit crosstalk

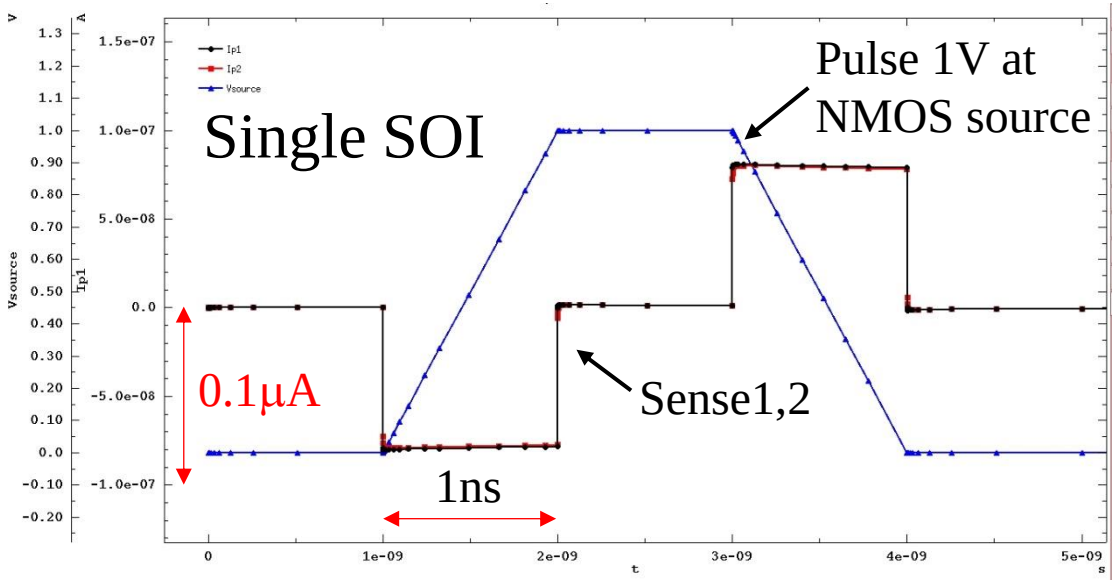
Geometry of TCAD simulation
For double SOI effectiveness study

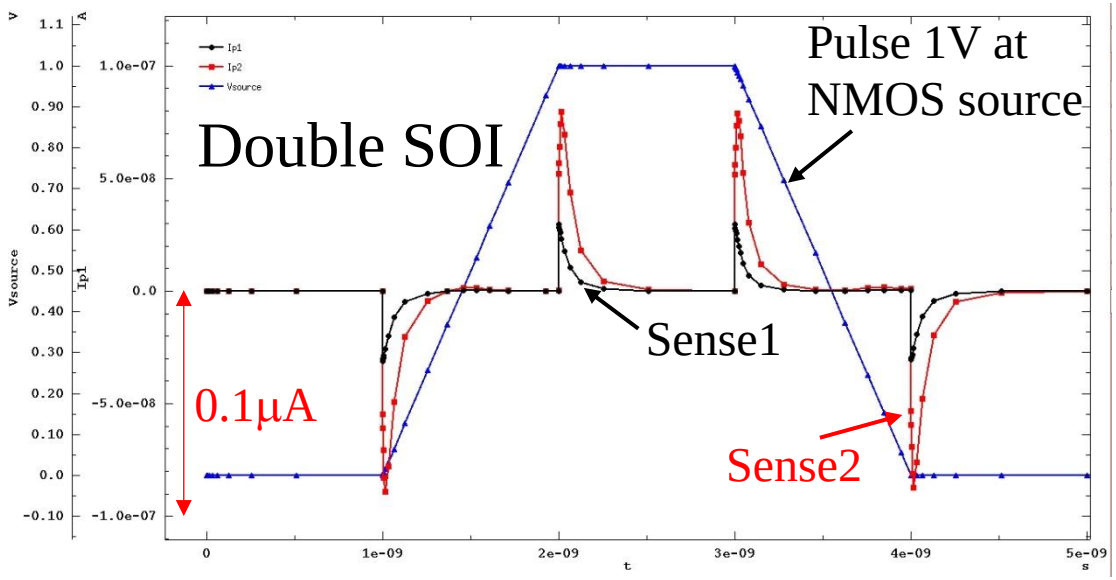
Dope density [/cm^3]



Transition analysis

Crosstalk (TCAD Simulation)





Blue: *Vsource*

Black: *Ip1*

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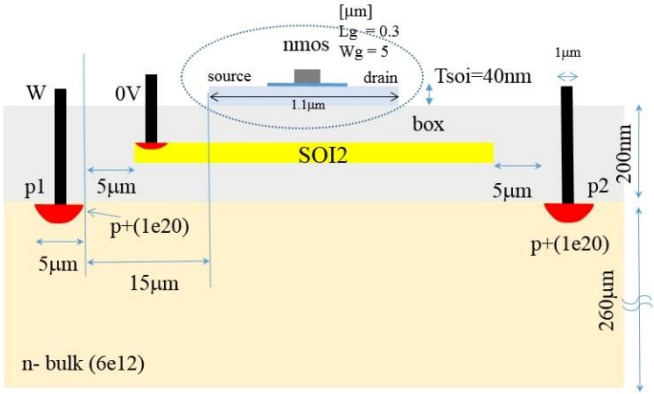


Crosstalk can be suppressed in double SOI sensor

Development of double SOI pixel sensors

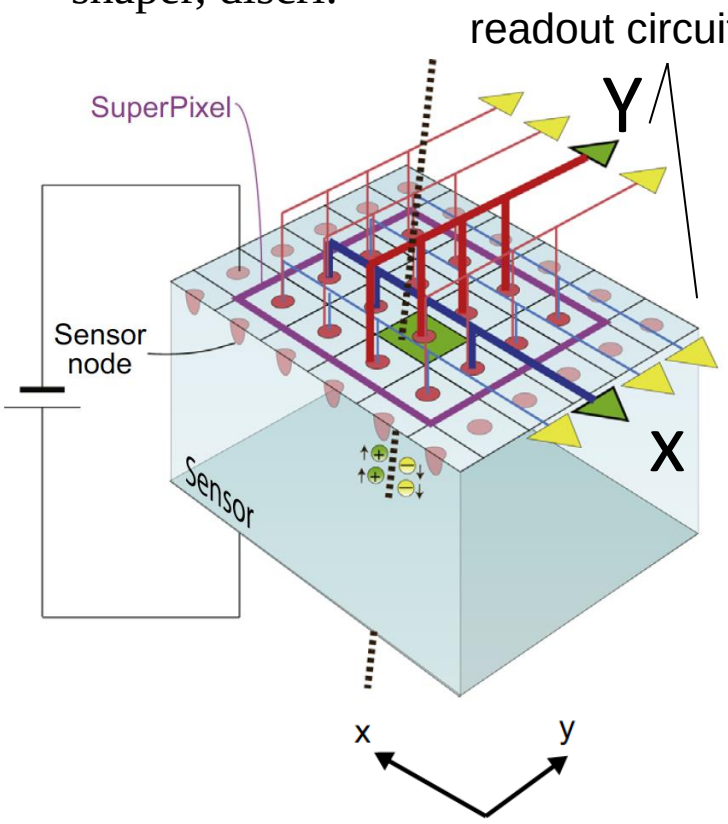
2012 The first prototype → breakdown study
2013 The second prototype → pixel sensor, rad. hard study
(TIPP2014, VERTEX2014, IEEE-NSS 2014)
2014 The third prototype
→ Still under fabrication! → chips will be delivered in October

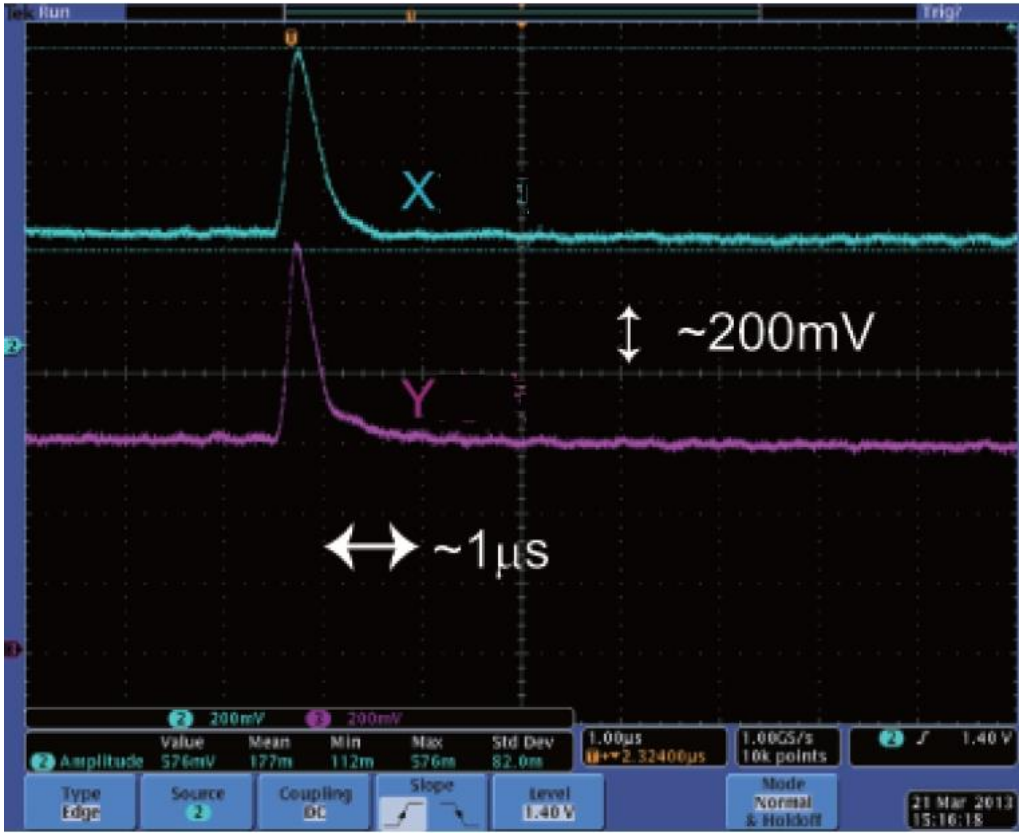
Shaper output of beta-ray signal (PIXOR)

Double SOI (d-SOI) : The second prototype

Tohoku Univ.

"Superpixel" includes pre-amp., shaper, discri.





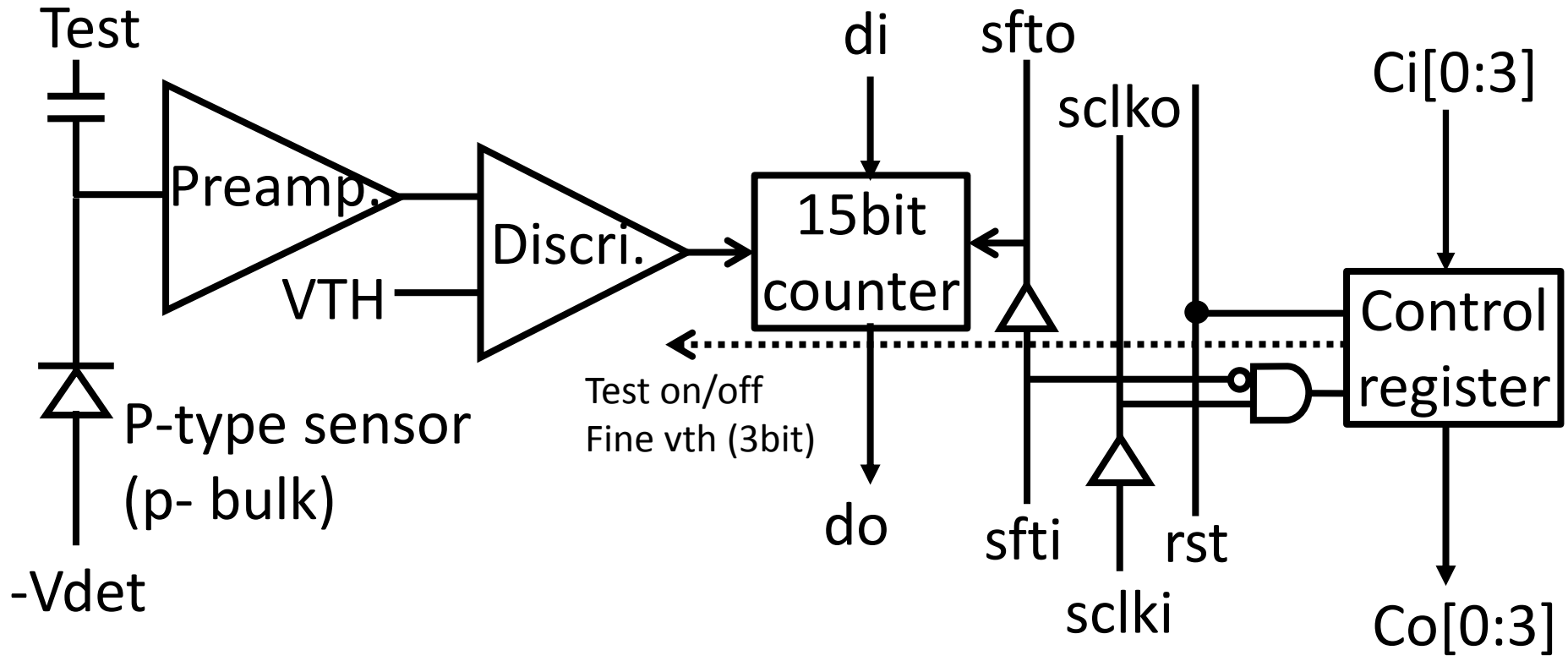
Sr-90 beta-ray

Y. Ono et al., NIMA 731 (2013) 266-269
N. Shinoda, Master thesis, March, 2013

beta-ray signals were observed successfully from Pre-amp.&shaper cir. with d-SOI
Discriminator output is not confirmed yet.

Future plan; Counting-type pixel (double SOI)

Under development



Future plan; Counting-type pixel (double SOI)

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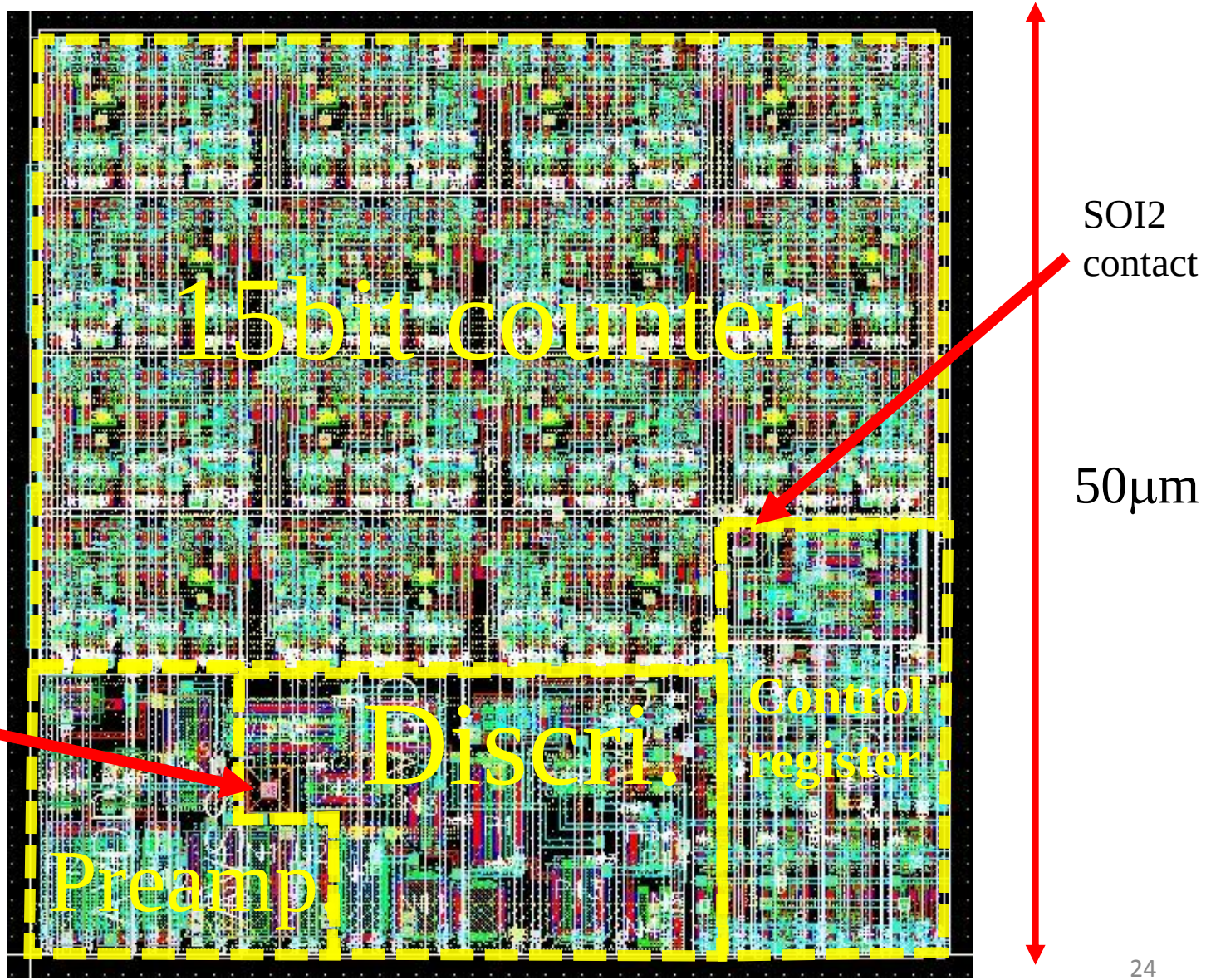


Summary

Several SOI pixel sensors have successfully been fabricated

3 issues; the back-gate effect, radiation hardness, sensor-circuit crosstalk
1. The back-gate effect
Integration-type pixel sensors works thanks to BPW process

2. Sensor-circuit crosstalk
can be suppressed by applying double SOI

3. Radiation hardness
(is not mentioned in this talk)

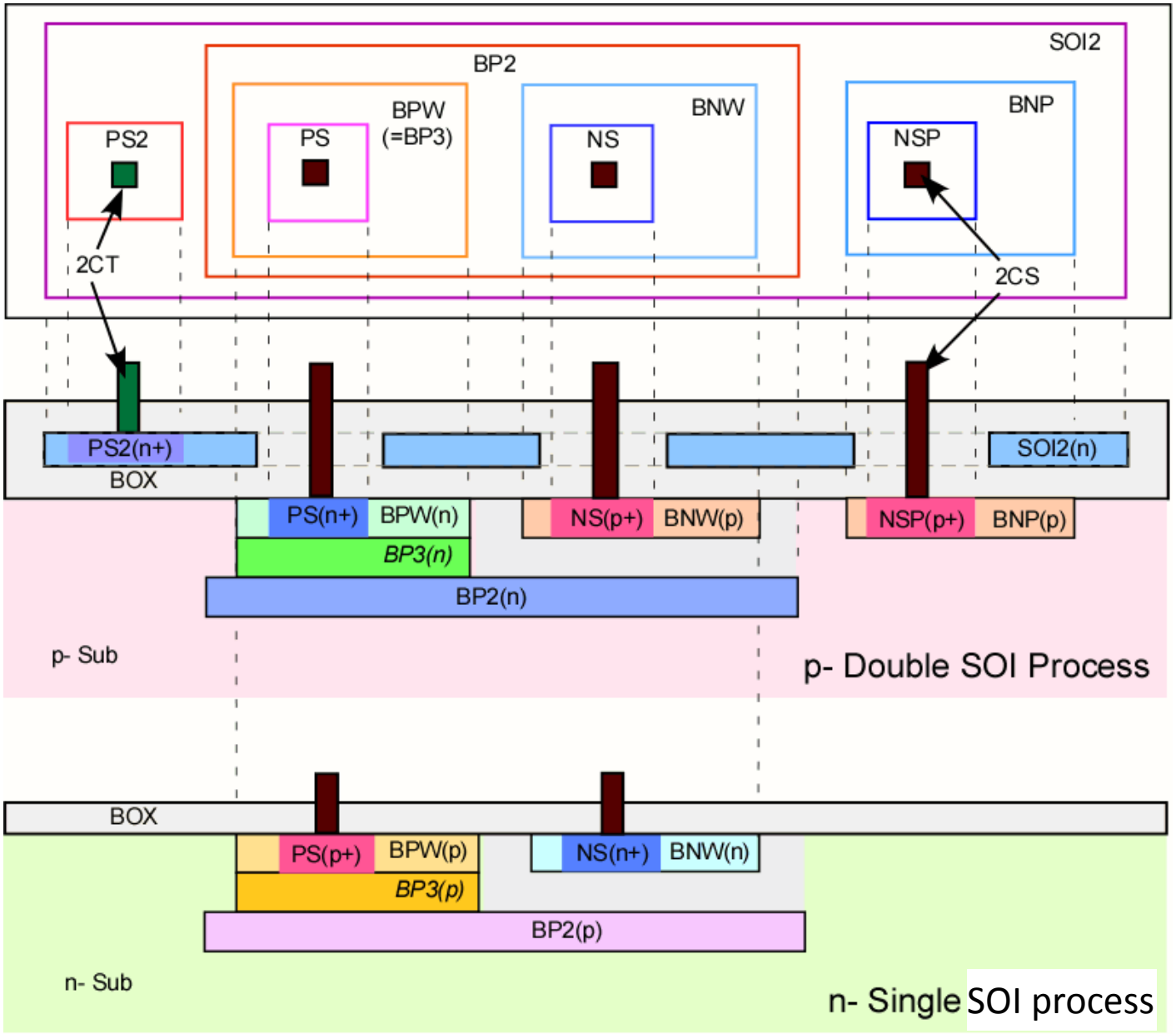
SPRiT (SOI Portable Radiation imaging Terminal)

Double SOI pixel sensors:
The 1st trial 2012
The 2nd trial 2013
The 3rd trial 2014 Chips will be delivered in October.
optimize pixel design with p-type DSOI sensors

http://rd.kek.jp/project/soi/

Supplement

Various Implantation Options in Sensor part

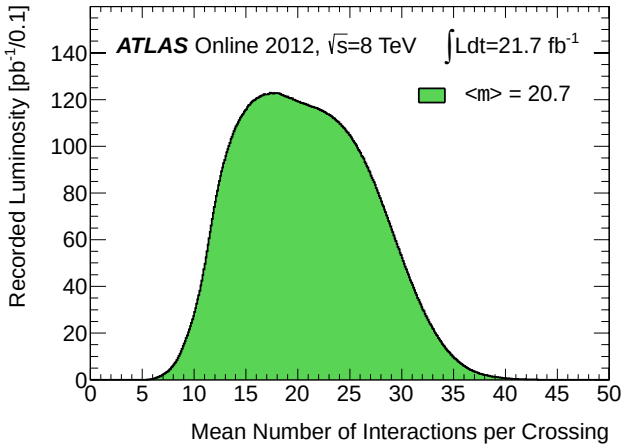


CPIX14
Y.Arai

Requirements to the Pixel Detectors

Hadron colliders:

- High total integrated dose and neutron flux
  LHC ATLAS inner Pixel detector:
  ~160 kGy and 10^{15} n_{eq}/cm^2 (x10 for HL-LHC)
- Immunity to Single Event Effects
- Very high event pile-up



Linear colliders:

- High granularity
- Complex readout scheme

➔SOI pixel detector fulfill these requirements.

M. Yamada, PIXEL2014

ATLAS Luminosity Public Results:
https://twiki.cern.ch/twiki/bin/view/AtlasPublic/LuminosityPublicResults

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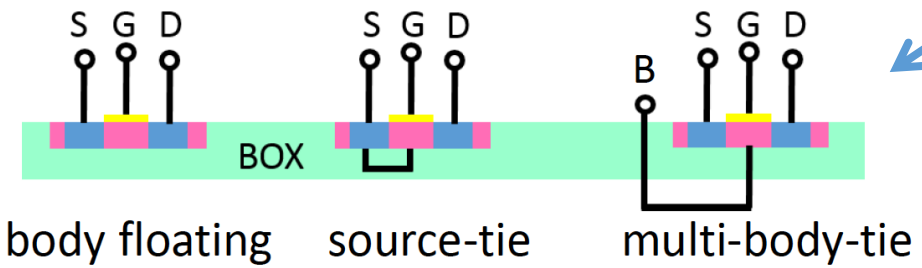
Cancelling the TID effects

Compensation of TID effect

Threshold of transistor shifts negatively due to positive potential from BOX .
➔Applied negative potential to SOI2 (VSOI2).

Test samples (NMOS and PMOS)

- several *L* and *W* of Tr
- low, normal and high threshold V
- Three kinds of body connections



Several types of transistors are used for readout circuit.
We evaluated the radiation damage of transistors processed on double SOI.

Irradiation: ^{60}Co γ-ray from 3 kGy up to 2 MGy

at Takasaki Advanced Radiation Research Institute, JAEA
(`http://www.taka.jaea.go.jp/index_e.html`)

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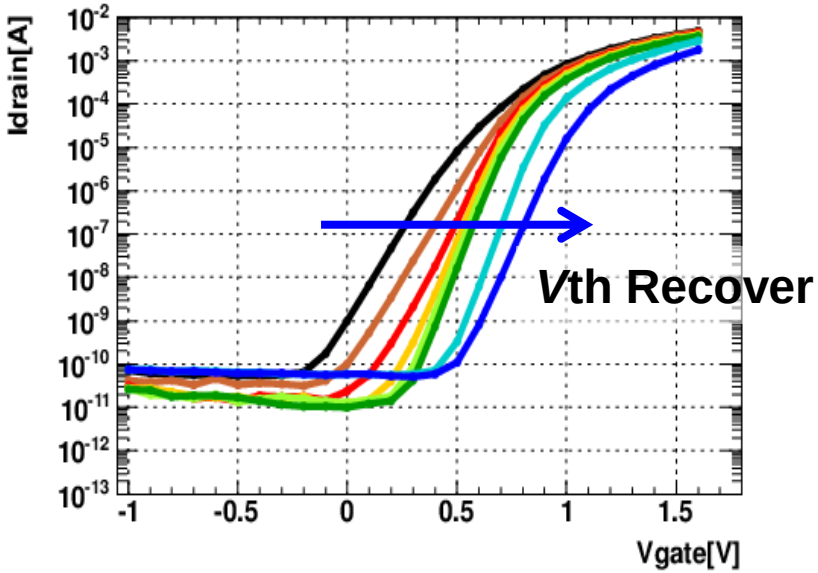
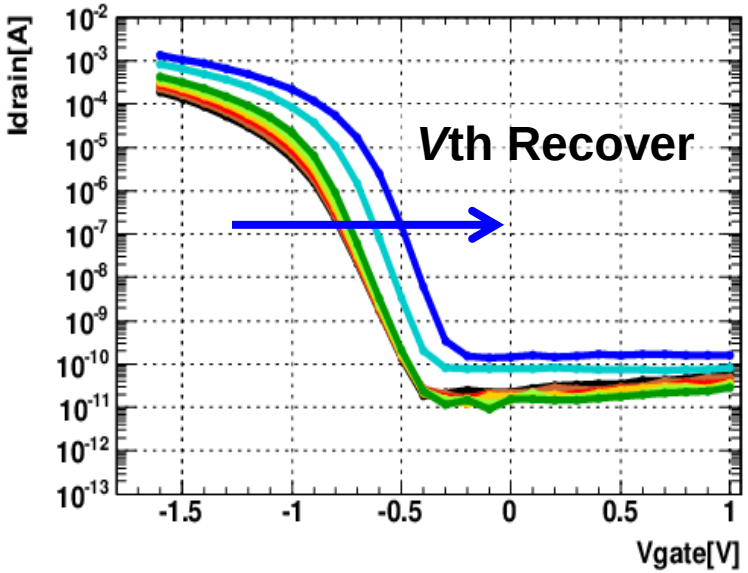
I_D-V_G after Irradiation with VSOI2

I_D-V_G curves with VSOI2 to cancel positive potential from BOX after irradiation of **200 kGy**.

NMOS Body-tie



PMOS Body-tie



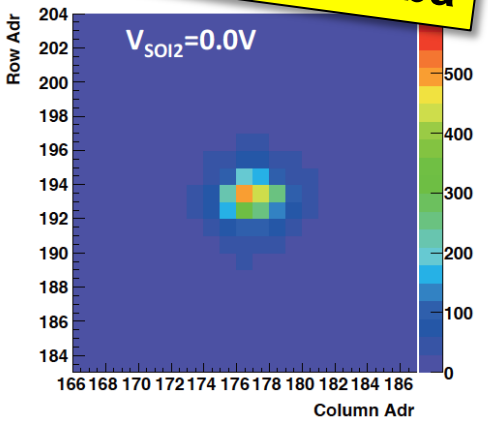
● VSOI2=0V ● VSOI2=-1V ● VSOI2=-2V
● VSOI2=-3V
● VSOI2=-4V ● VSOI2=-5V ● VSOI2=-10V ● VSOI2=-15V

We observed recovery of I_D-V_G curve after irradiation with VSOI2.

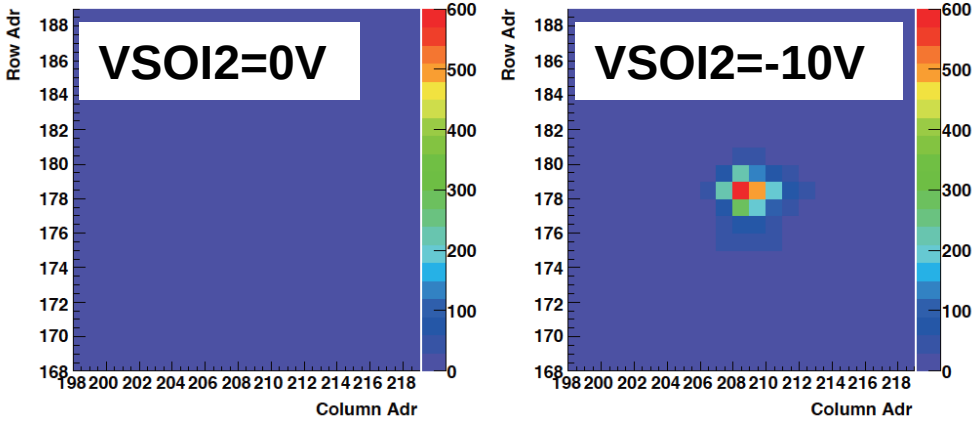
Double SOI

Pre-irrad

Univ. Tsukuba

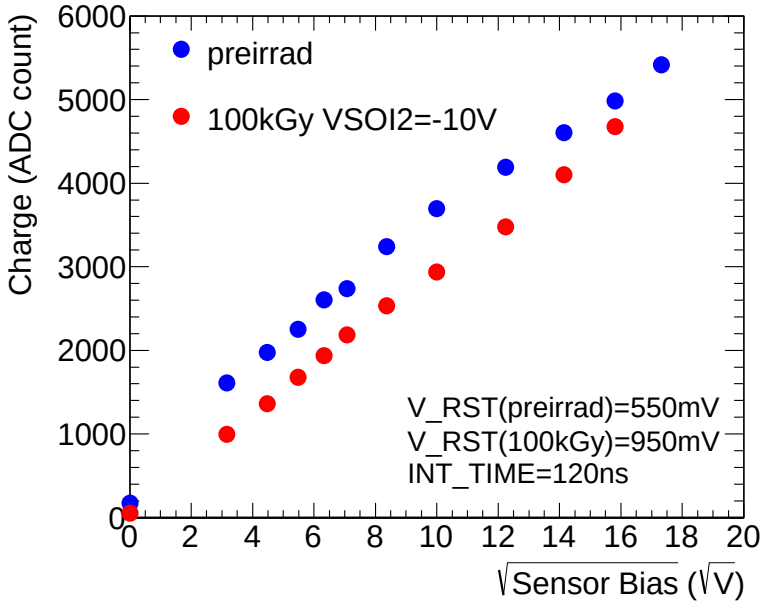


Response to infrared laser of 1064 nm wavelength and 10 n pulse duration.



The pixel images after 100 kGy could not obtain but recovered with VSOI2=-10V.

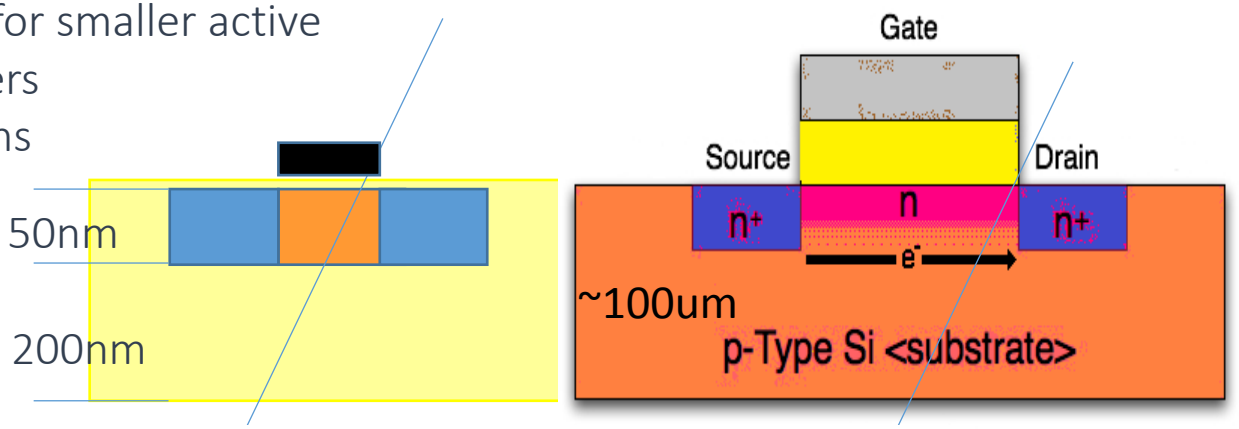
The average ADC count as function of the square root of the bias voltage for sensor.
➔Obtained similar linearity and sensitivity to pre-irradiation with VSOI2=-10 V .



S. Honda et al., TIPP12014, 2-6 June 2014, Amsterdam

TID: Target Radiation Levels

SOI is immunity from SEEs for smaller active area, enclosed in oxide layers
⇨ ideal for space applications



TID: Total Ionization Damage is rather complicated …

Wide dose range of applications:

LHC pixel ~ 500 kGy, $10^{15} n_{eq}/cm^2$@ATLAS (*x*10 for HL-LHC)
Belle-II ~ 10 kGy/y, $2x10^{12} n_{eq}/cm^2$ /y
ILC (e.g., ILD @ *r*=15 mm) ~ 1 kGy/y, ~$10^{11} n_{eq}/cm^2$ /y
X-ray imaging: kGy/y ～MGy/y
…

Radiation damage studies done so far:

proton irradiation to 10^{16} n_{eq}/cm^2
^{60}Co γ irradiation to 5 MGy
for DOUBLE-SOI: ^{60}Co γ irradiation to 2MGy

Tohoku Univ.

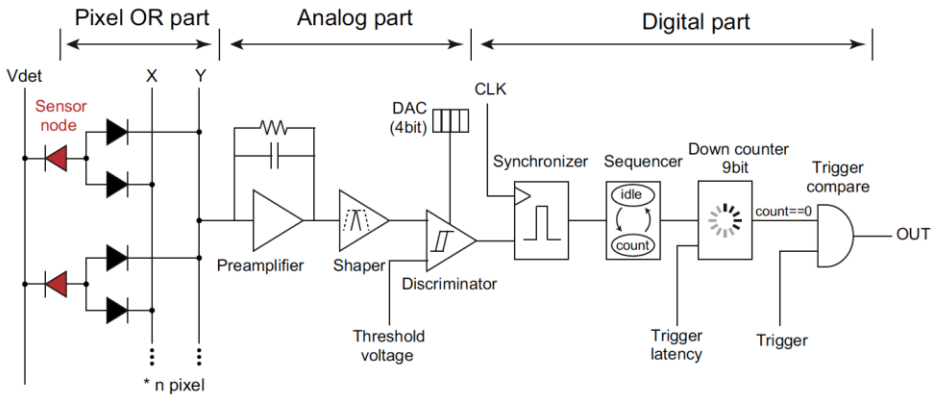
PIXOR

Digital part

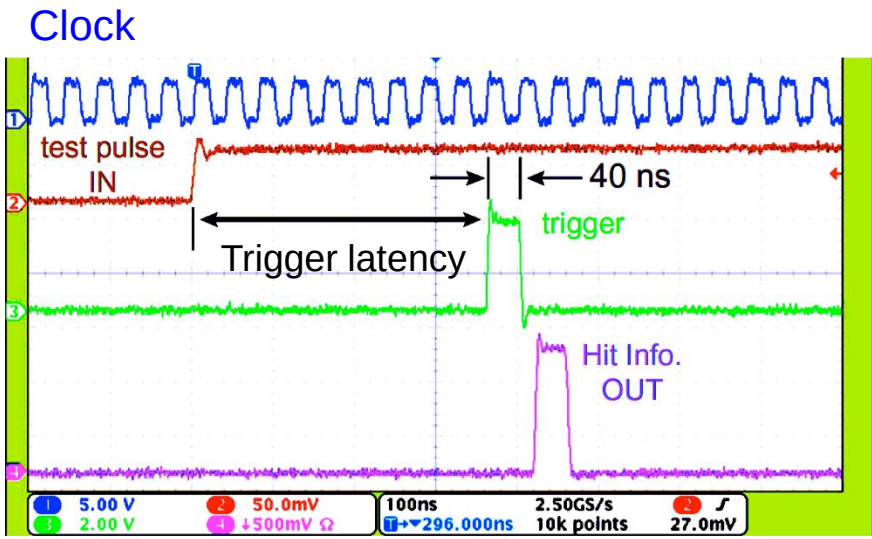
It manages holding of binary data from discriminator and timing comparison of hit and trigger.

Generally a trigger decision takes several micro seconds from the actual event time in high energy experiment (trigger latency).

Evaluated the overall circuit of digital part with a test-pulse.



Digital circuit could store the hit information of the signal during the trigger latency and sent a binary hit information as expected.



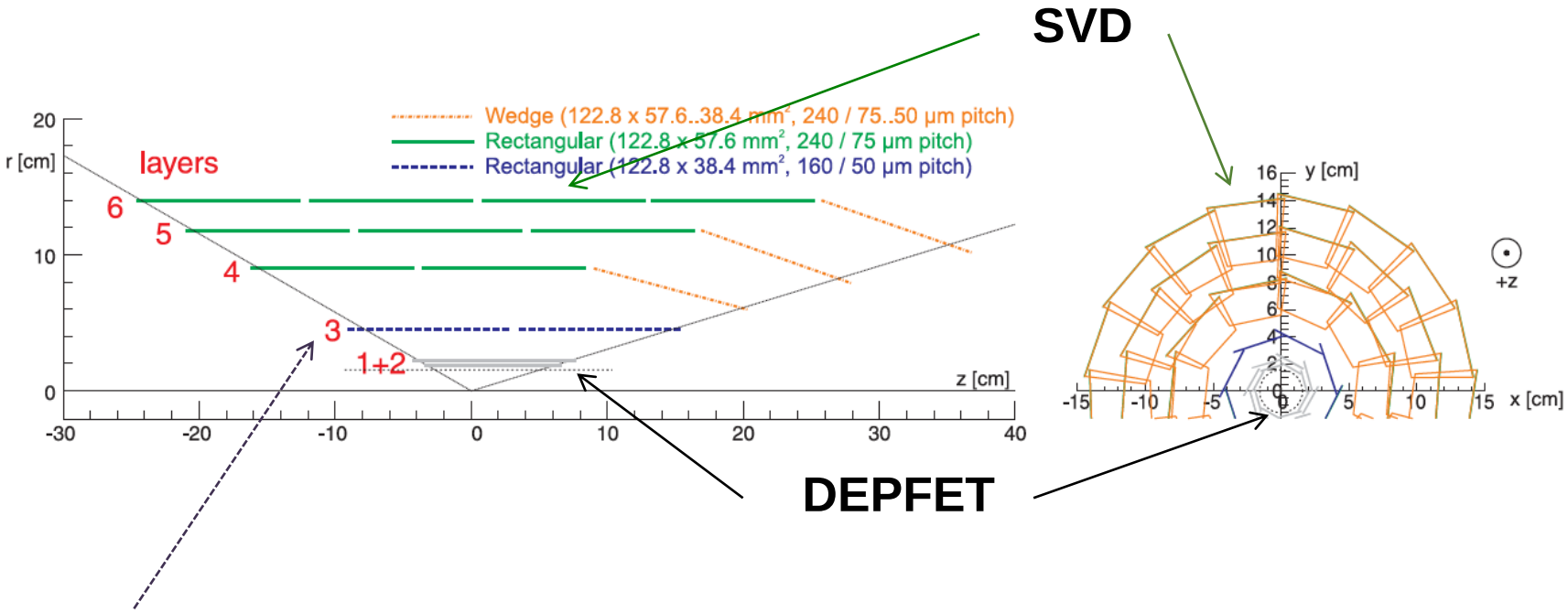
Y. Ono et al., NIMA 731 (2013) 266-269
N. Shinoda, Master thesis, March, 2013

PIXOR

Vertex Detector of Belle II

Two layers of pixel detector **DEPFET**

Four layers of silicon strip detector **SVD**



We are aiming PIXOR is installed as 1st layer of SVD for Belle II upgrade.

M.Friedl et al., “The Silicon Vertex Detector of Belle II”, VERTEX2011, 19-24 June 2011, Rust, Lake Neusiedel, Austria