The Clock Distribution System for the ATLAS Liquid Argon Calorimeter Phase-I Upgrade Demonstrator

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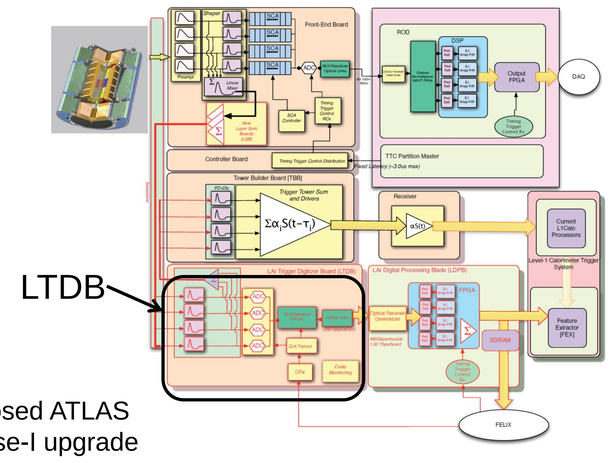
Introduction

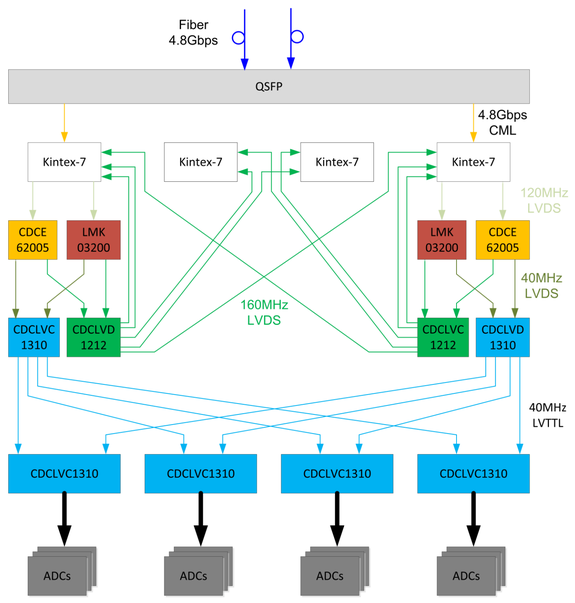
- The trigger electronics of the ATLAS liquid argon calorimeter (LAr) is being developed for the LHC Phase-I trigger upgrade [1].
- A Liquid-argon Trigger Digitizer Board (LTDB) will be developed for the ATLAS liquid Argon Colorimeter Phase-I trigger upgrade.
- In order to demonstrate the full function of the LTDB, which is based on ASICs such as GBTX and GBT SCA, a prototype board called the Demonstrator is being developed based on Commercial-Off-The-Shelf (COTS) components.
- Each Demonstrator includes 40 octal-channel Analog/Digital converters (ADCs) and 4 FPGAs.
- Each ADC needs a 40-MHz LVTTL clock.
- Each FPGA has 16 embedded multi-gigabit-transceivers and needs 2 clocks at 160 MHz.
- It is critical to distribute high-quality clocks to all ADCs and FPGAs.



The architecture of the proposed ATLAS LAr trigger electronics in Phase-I upgrade

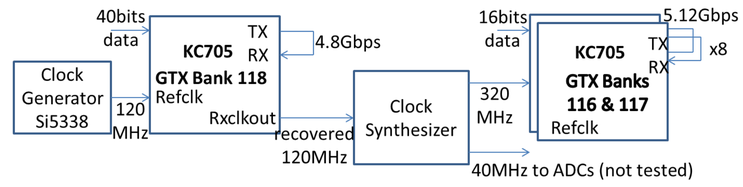
Design and Verification

- The clock source comes from a GLIB board located on the back-end counting room via optical fibers.
- Two channels of QSFP optical receivers convert optical signals to electronic signals and send electrical signals to two Kintex-7 FPGAs.
- Each FPGA runs the GBT firmware and recovers two 120-MHz clocks from the 4.8-Gbps data.
- The two recovered 120-MHz clocks are sent into two frequency synthesizers/jitter cleaners LMK03200 and CDCE62005, respectively, each of which cleans jitter and generates a 40-MHz LVDS clock and a 160-MHz LVDS clock.
- Five 10-output low-jitter clock buffers CDCLVC1310 convert the 40MHz LVDS clocks to 40 LVTTL clocks to drive 40 ADCs ADS5272.
- A 12-output low-jitter LVDS clock buffer CDCLVD1212 fans out the 160-MHz LVDS clock and drives 4 Kintex-7 FPGAs. Each of the two FPGAs on the left most and the right most need one extra clock for slow control.
- In order to improve the reliability, optical fibers, optical receivers, FPGAs, jitter cleaners, and clock buffers are redundantly. Each clock buffer has two inputs and can be remotely configured to select one clock source.



The block diagram of the clock distribution system

- All components, including the optical transceiver, the FPGA, the clock frequency synthesizers/jitter cleaners, the clock buffers, have been tested independently.
- The jitter of the recovered clock after the jitter cleaner was verified to meet the requirements of ADCs and FPGAs.
- The clock distribution scheme to the FPGA has been verified with real data transmission firmware.



The block diagram of the clock distribution system

The jitter measurement summary

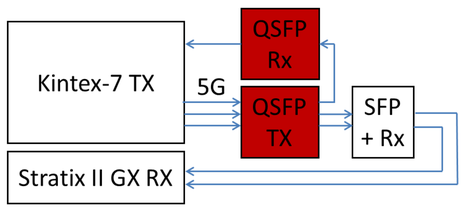
Clock jitter		Random (RMS, ps)	Deterministic (pk-pk, ps)
Before cleaner		5.9	81.2
After cleaner	CDCE62005	5.1	6.5
	LMK03200	1.4	12.9

Radiation Tolerance Qualification

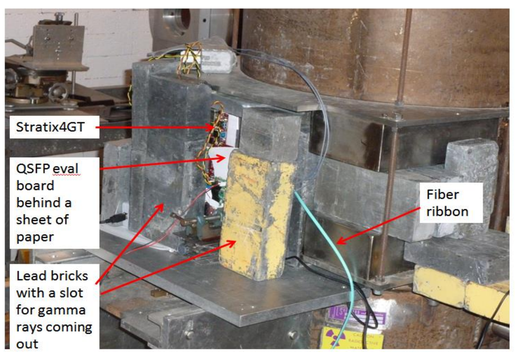
- The Demonstrator will operate at low luminosity for one to three years (2015-2017, 100 fb^{-1}).
- All components have been tested in a neutron (max 800 MeV) or 200-MeV proton beam for SEE and in X-rays or ^{60}Co gamma rays for TID.
- The test results show that all components chosen meet the radiation tolerance requirements for the Demonstrator.

The estimated radiation level at the ATLAS LAr (including safety factors) in three-year operation

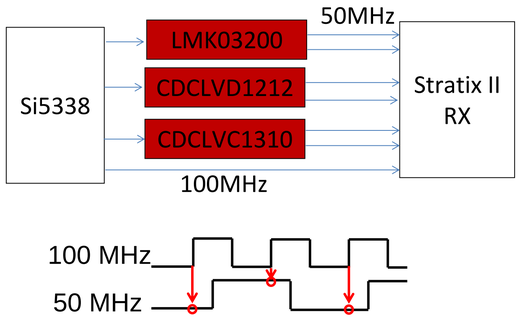
TID	9.0 krad(SiO2)
NIEL	1.6E12 (1-MeV equ. neutron)/cm^2
SEE	2.3E11 (>20 MeV hadron)/cm^2



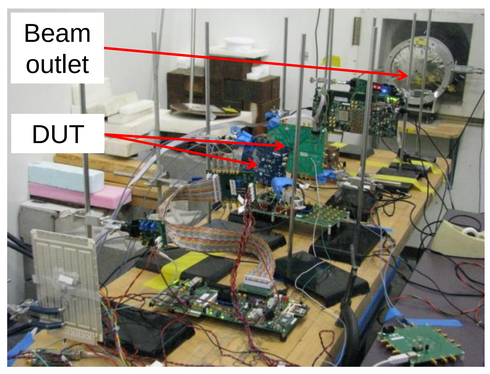
The SEE test setup of QSFP



The picture of the TID test setup of QSFP



The SEE test setup of clock buffers and jitter cleaner



The picture of the SEE test setup of clock buffers

The SEE test result summary

Device	Rad type	Non-SEFI SEU		SEFI	
		σ (cm^2)	Est. err rate (1/yr)	σ (cm^2)	Est. err rate (1/yr)
AFBR-79EIDZ RX	Proton	<1.3E-11	<1.0	<1.3E-11	<1.0
	Neutron	<2.3E-11	<1.8	<2.3E-11	<2.0
LMK03200	Neutron	<2.5E-11	<1.9	6.1E-10	46
CDCLVD1212	Neutron	2.3E-11	1.7	<2.3E-11	<1.7
CDCLVC1310	Neutron	<8.0E-12	<0.61	<8.0E-12	<0.61
XC7K325T RX	Neutron	2.2E-10	16	2.0E-10	16

The TID test result summary

Device	Rad	Dose Rate (krad/hr)	TID (krad)	Degradation	Max Icc change
AFBR-79EIDZ	X-ray	5.1	8.1	No	N/A
LMK03200	X-ray	3.0	14.9	No	< 1%
CDCLVC1310	X-ray	38	1230	No	15%
CDCLVD1212	^{60}Co γ	N/A	1130	No	50%

Conclusion

- A COTS-based clock distribution system has been developed for the ATLAS LAr LTDB Demonstrator.
- The performance of the clock distribution system has been evaluated.
- The components used in the clock distribution system have been qualified to meet radiation tolerance requirements of the Demonstrator.

Acknowledgments

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References

[1] ATLAS Collaboration, *ATLAS liquid argon calorimeter Phase-I upgrade technical design report*, CERN-LHCC-2013-017 and ATLAS-TDR-022, September 20, 2013.
[2] Martin Dentan, "ATLAS policy on radiation tolerant electronics," *ATLAS Project Document No. ATC-TE-QA-0001 (Rev 2)*, 21 July 2000.
[3] Philippe Farthouat, "Radiation Tolerant Electronics New Safety Factors," ATLAS upgrade Week, Nov. 6, 2013, CERN, Geneva, Switzerland.

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