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The Clock Distribution System for the ATLAS Liquid Argon Calorimeter Phase-I Upgrade Demonstrator

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A prototype Liquid-argon Trigger Digitizer Board (LTDB), called LTDB Demonstrator, has been proposed to demonstrate the functions of the ATLAS Liquid Argon Calorimeter Phase-I trigger electronics upgrade. Forty Analog/Digital converters and four FPGAs with embedded multi-gigabit-transceivers on each Demonstrator need high quality clocks. A clock distribution system based on commercial components is being developed for the Demonstrator. The design of the clock distribution system is presented. The performance of the clock distribution system has been evaluated. The components used in the clock distribution system have been qualified to meet radiation tolerance requirements of the Demonstrator.

Summary

A Liquid-argon Trigger Digitizer Board (LTDB) will be developed for the ATLAS liquid Argon Colorimeter Phase-I trigger upgrade. In order to demonstrate the full function of the LTDB, which is based on ASICs such as GBTX, a prototype board called the Demonstrator is being developed based on Commercial-Off-The-Shelf (COTS) components. Each Demonstrator includes 40 octal-channel Analog/Digital converters (ADCs) and 4 FPGAs. Each ADC needs a 40-MHz LVTTL clock. Each FPGA has 16 embedded multi-gigabit-transceivers and needs 2 clocks at 160 MHz. It is critical to distribute high-quality clocks to all ADCs and FPGAs.

We present a clock distribution system for the LTDB Demonstrator. The clock source of the Demonstrator comes from a GLIB board located on the back-end counting room via optical fibers. A four-channel QSFP optical receiver converts the optical signal to the electronic signal and sends the electrical signal to a Kintex-7 FPGAs. The FPGA runs the GBT firmware and recovers a 160-MHz clock from the 4.8-Gbps data. The recovered 160-MHz clock is sent into a frequency synthesizer and jitter cleaner LMK03200. LMK03200 is a zero-delay clock conditioner which cleans jitter. LMK03200 is also a frequency synthesizer which generates a 40-MHz LVDS clocks and a 160-MHz LVDS clock. Five 10-output low-jitter clock buffers CDCLVC1310 convert the 40MHz LVDS signal to 40 LVTTL clocks to drive 40 ADCs ADS5272. An 12-output low-jitter LVDS clock buffer CDCLVD1212 fans out the 160-MHz LVDS clock and drives 4 Kintex-7 FPGAs. In order to improve the reliability, two FPGAs and two jitter cleaners are redundantly used to recover the 160-MHz clocks from two optical fibers. The clock buffers have two inputs which can be remotely configured to select one clock source.

The performance of the clock distribution system has been evaluated. All components, including the optical transceiver, the FPGA, the clock frequency synthesizer and jitter cleaner, the clock buffers, have been tested independently. The clock frequency synthesizer and jitter cleaner has been tested to generate 40-MHz and 160-MHz clocks. The jitter of the recovered clock after the jitter cleaner was verified to meet the requirements of ADCs and FPGAs. The clock distribution scheme to the FPGA has been verified with real data transmission firmware.

The clock distribution system has been qualified to meet radiation tolerance requirements. The Demonstrator will operate at low luminosity for one to three years (2015-2017), so the radiation level for the Demonstrator is lower than that for the LDTB. However, since the Demonstrator is based on COTS components, the radiation tolerance of all components has to be evaluated. The components, including optical transceivers, clock buffers, jitter cleaner & clock synthesizers, and the FPGA, were irradiated with a neutron or proton beam and with

X-rays or gamma rays. The test results show that all components meet the radiation tolerance requirements for the Demonstrator.

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