First operation of the Level-0 Trigger of the NA62 Liquid Krypton Electromagnetic Calorimeter

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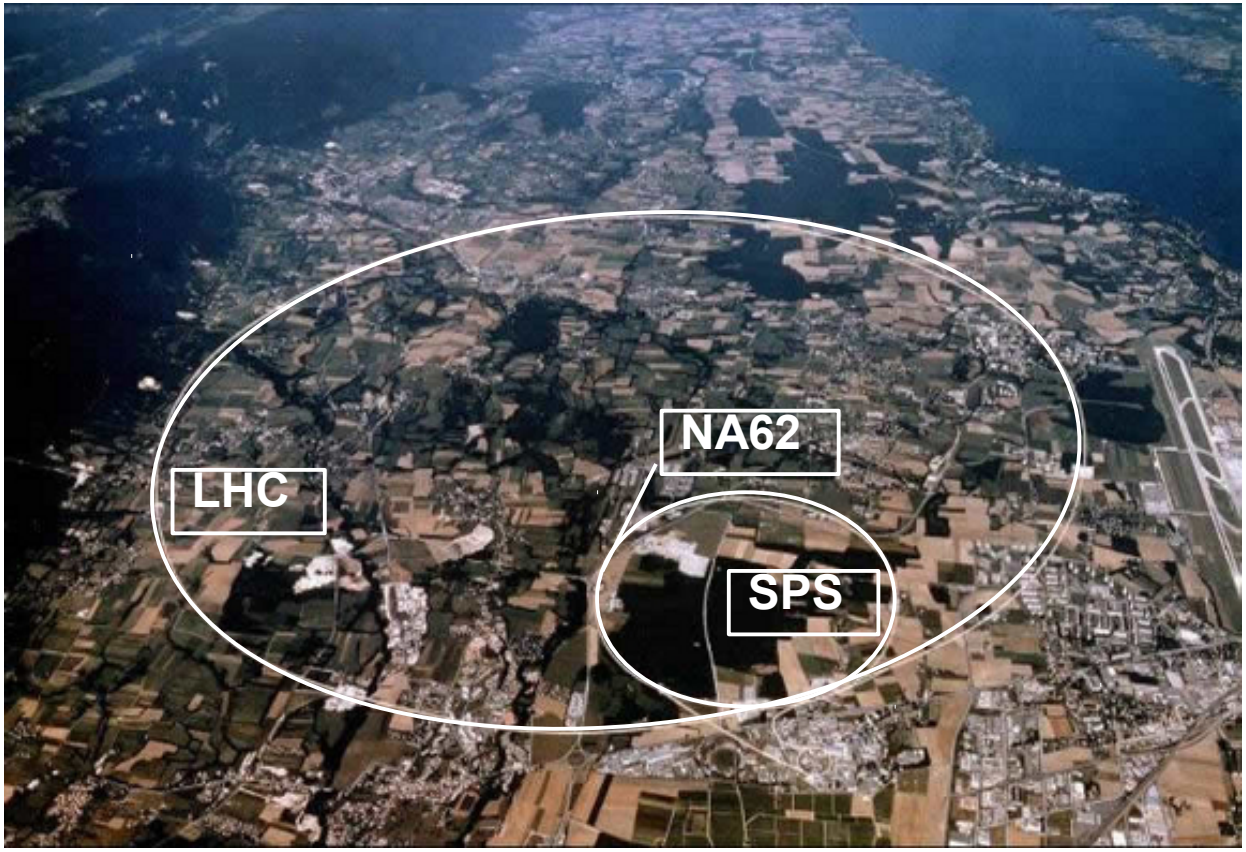
for the NA62 LKr L0 Trigger Working Group

TWEPP 2014 – Aix en Provence

The NA62 experiment at CERN SPS



Physics Physics Physics

2009–2012 | 2013–2014 | 2015 | 2016 | 2017 | 2018–2019

LHC LS1

LHC LS2

October 2014
1st Physics Test Run
(2 months : low intensity)

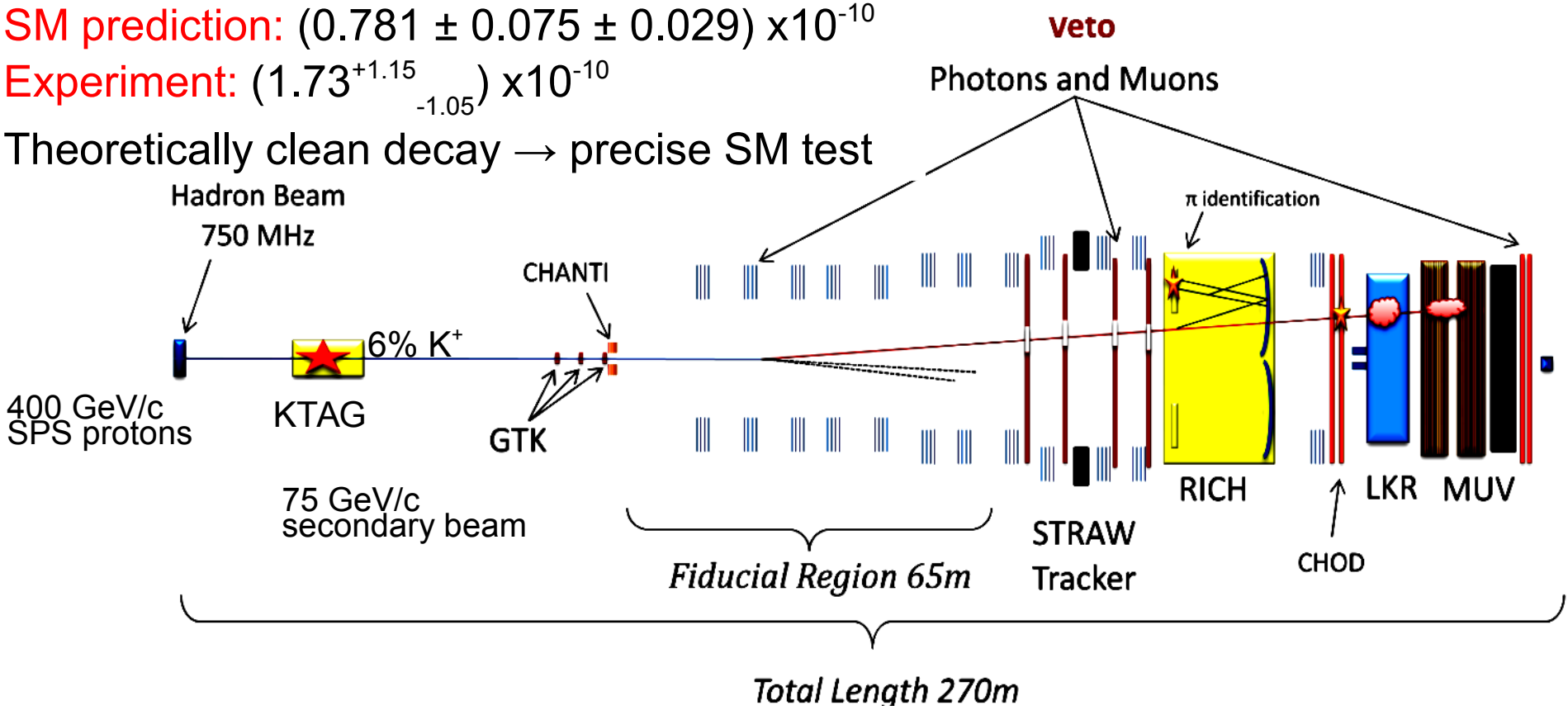
The NA62 experiment at CERN SPS

Goal: precise measurement of BR($K^+ \to \pi^+ \nu \bar{\nu}$)

SM prediction: $(0.781 \pm 0.075 \pm 0.029) \times 10^{-10}$

Experiment: $(1.73^{+1.15}_{-1.05}) \times 10^{-10}$

Theoretically clean decay → precise SM test



Main backgrounds:

$K^+ \to \mu^+ \nu \bar{\nu}$ (~ 63 %)

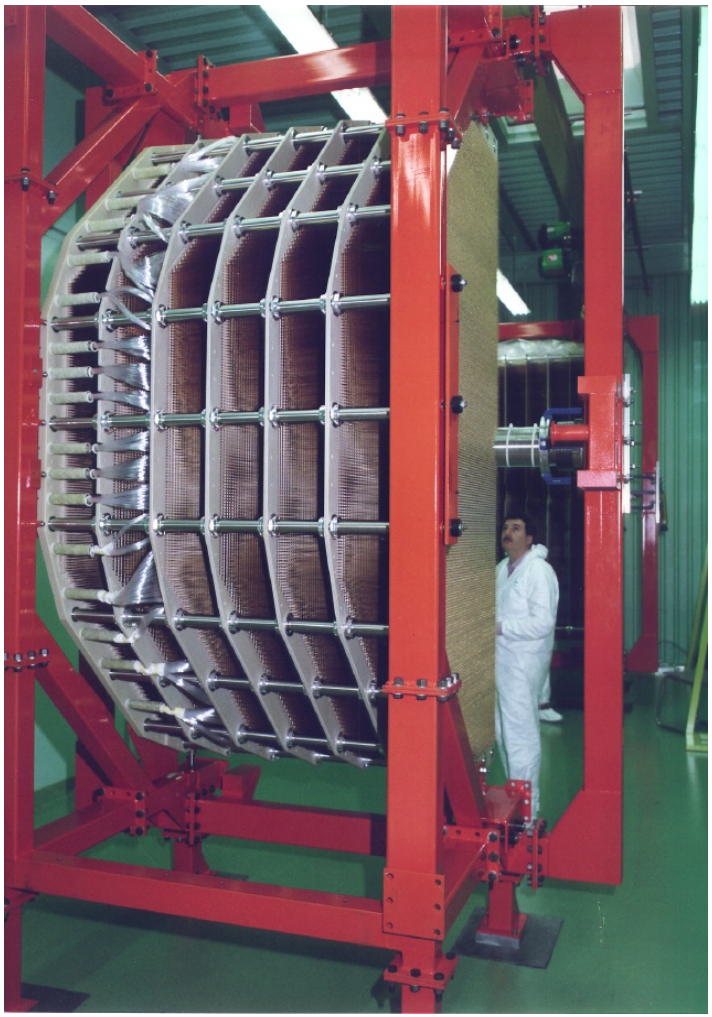
$K^+ \to \pi^+ \pi^0$ (~ 22 %) →

Hermeticity for photons up to 50 mrad.

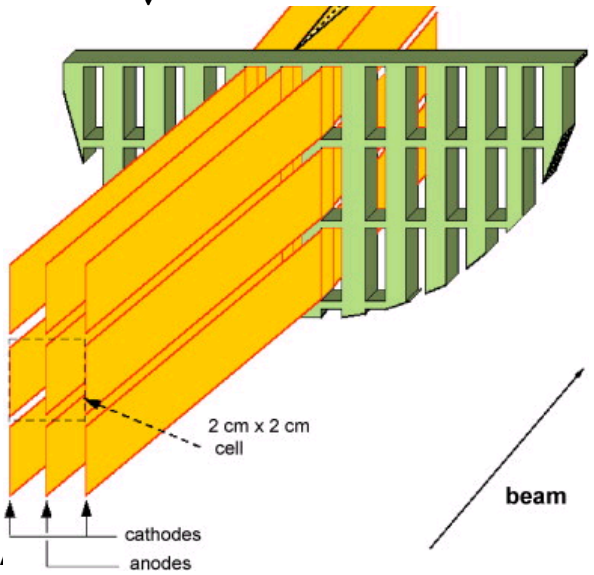
LKr (1-8.5 mrad) gets 80% of the photons.

The NA48 Liquid Krypton electromagnetic calorimeter

$K^+ \rightarrow \pi^+ \pi^0$ VETO

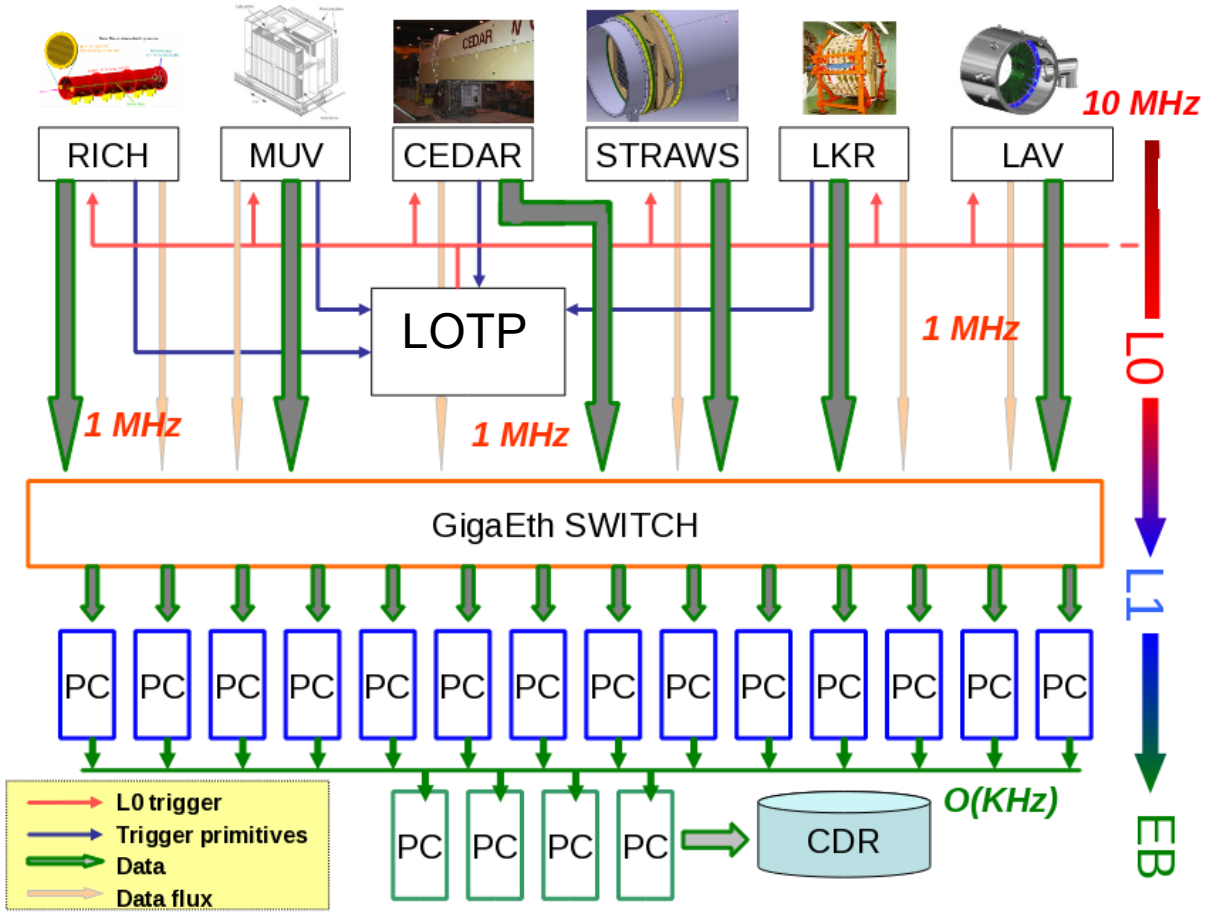


- 13248 channels.
- 27 X_0.
- Inefficiency: < 10^{-5} for E_γ > 10 GeV.
- σ_t = 800 ps (10 GeV photon).
- $$\frac{\sigma_E}{E} = \frac{3.2\%}{\sqrt{E}} \oplus \frac{9\%}{E} \oplus 0.42\% \quad \text{[E in GeV]}$$



The TDAQ System

12 sub-detectors, ~ 80000 channels, 25 GB/s raw data (LKr 22 GB/s)



L0 hardware trigger

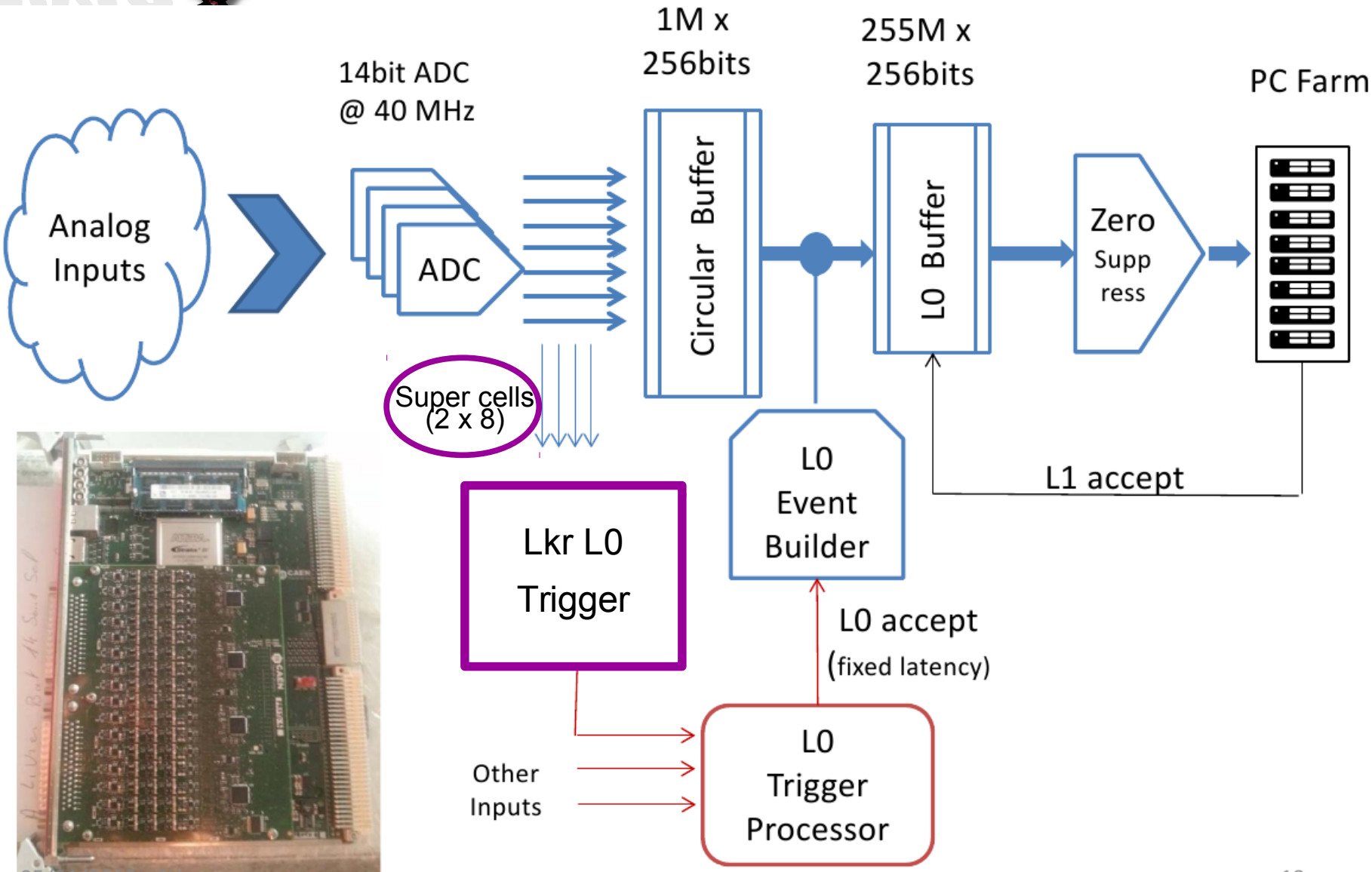
L0 = CHOD *RICH * $\overline{\text{LKR}}$ * $\overline{\text{LAV}}$ * $\overline{\text{MUV}}$

max output rate 1 MHz
max latency 1 ms

L1 software trigger
(sub-dector level)
max output rate 100 kHz
max total latency 1 s.

L2 software trigger
(event level)
max output rate ~15 kHz
max tot. latency = spill period (~ 10 s)

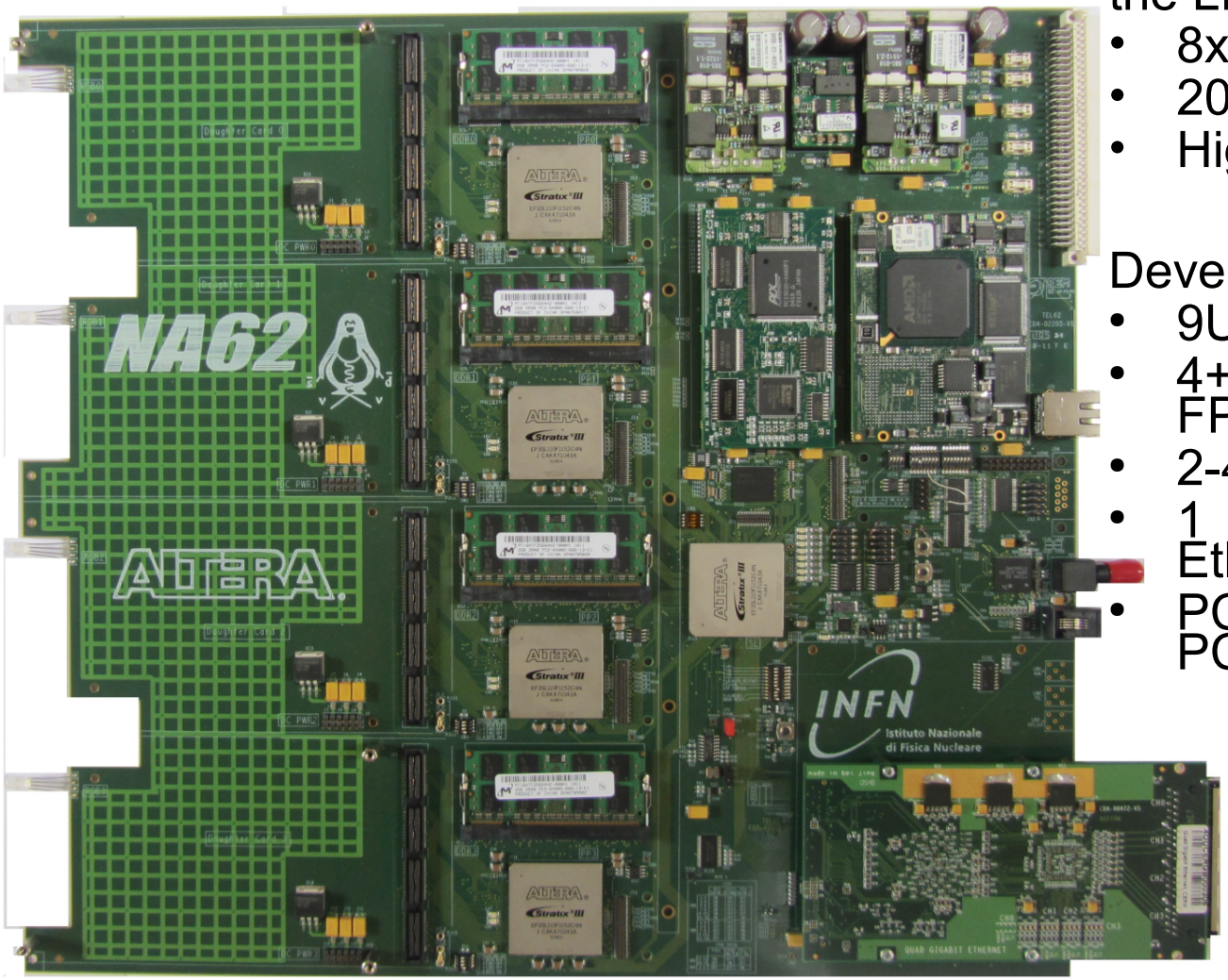
LKr CREAM Readout (414 boards)



(from F. Hahn)

The motherboard: TEL62

Trigger **EL**ectronics for NA**62**

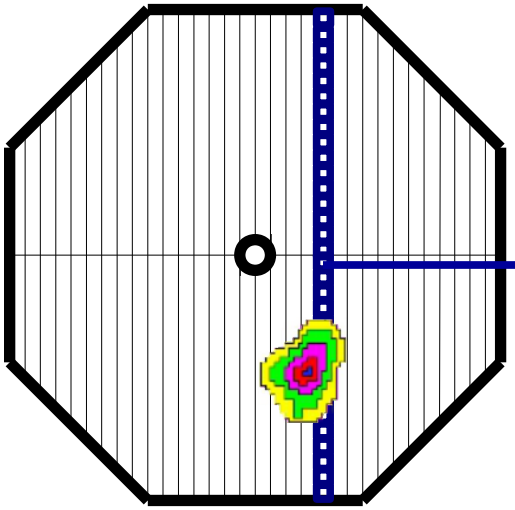


Update from TELL1, general purpose data acquisition board developed at EPFL for the LHCb experiment:

- 8x computational power
- 20x buffer memory
- Higher connectivity

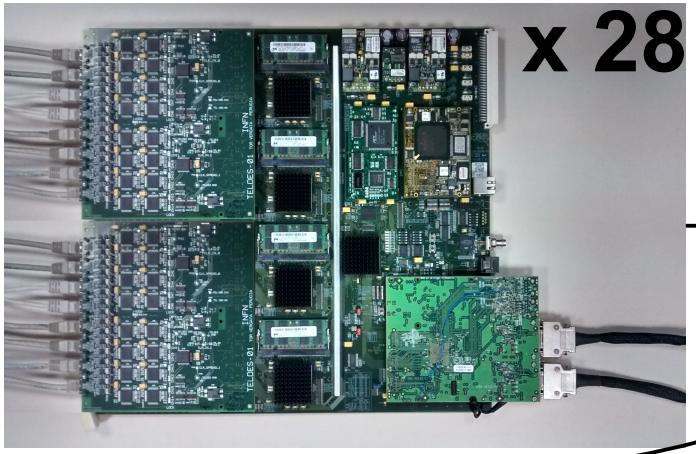
Developed ar INFN Pisa:

- 9U Eurocard size
- 4+1 Altera Stratix III FPGAs
- 2-4 input mezzanine cards
- 1 output mezzanine (e.g. Ethernet)
- PCI bridge to on-board PC.



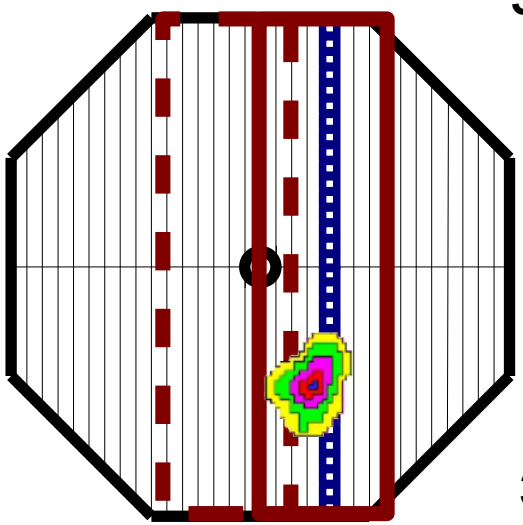
640 Mbps / ch
→ 20.5 Gbps
per TEL62

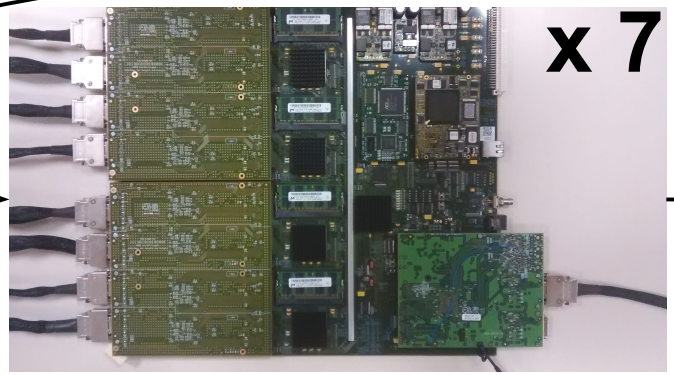
32 ch



FRONTEND LAYER

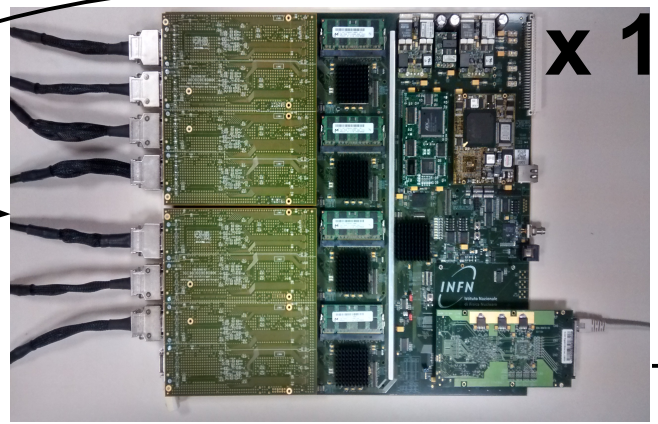
3.7 Gbps / ch





1st CONCENTRATOR LAYER

3.7 Gpbs / ch



2nd CONC. LAYER

L0 Trigger Processor

In the Test Run the system will be smaller:

6 FE (inner calorimeter) → 1 concentrator

LKr L0 Trigger: performance requirements in the worst case scenario

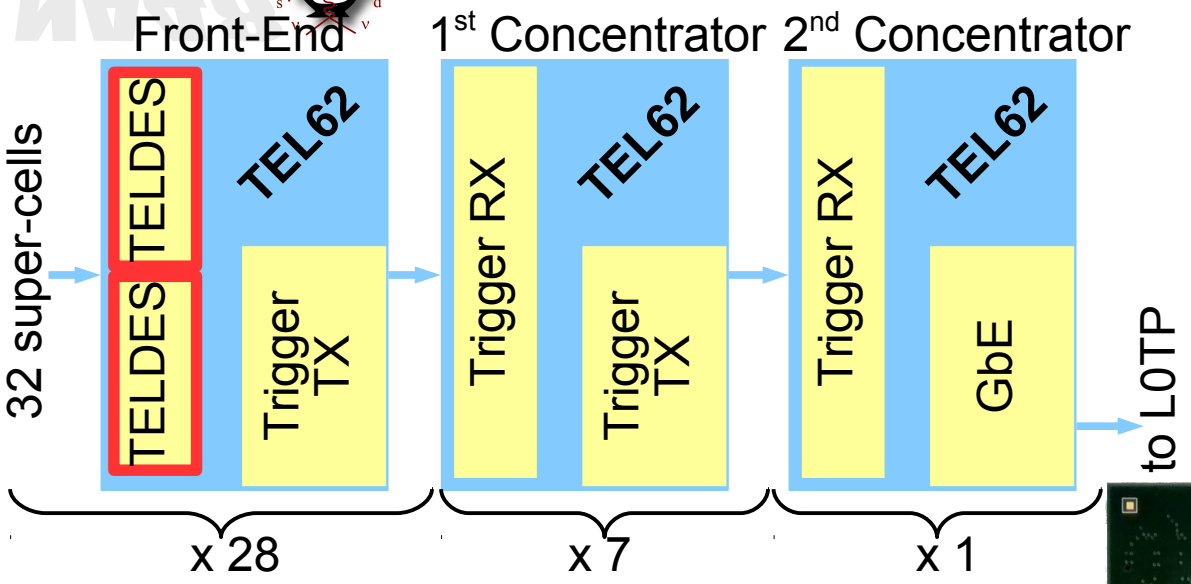
- From simulation:
  - max avg instantaneous hit rate = **30 MHz**
  - 3 times higher in calorimeter center → **90 MHz**
- Worst case:
  - each hit produces a cluster;
  - each cluster is large (256-cells).

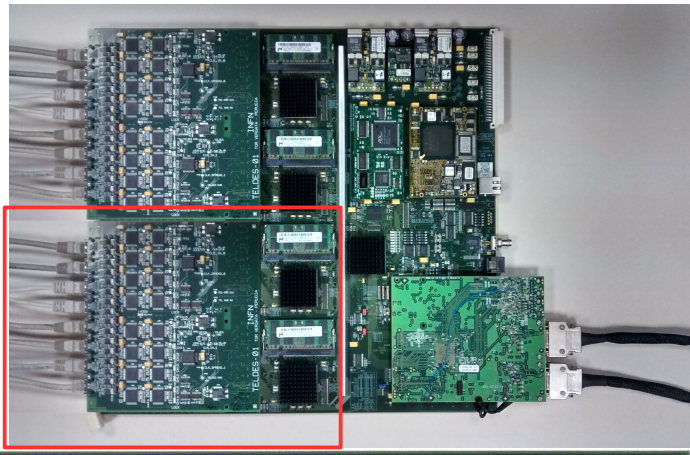
Max Peak Rate on each FE FPGA = **4.2 MHz**.

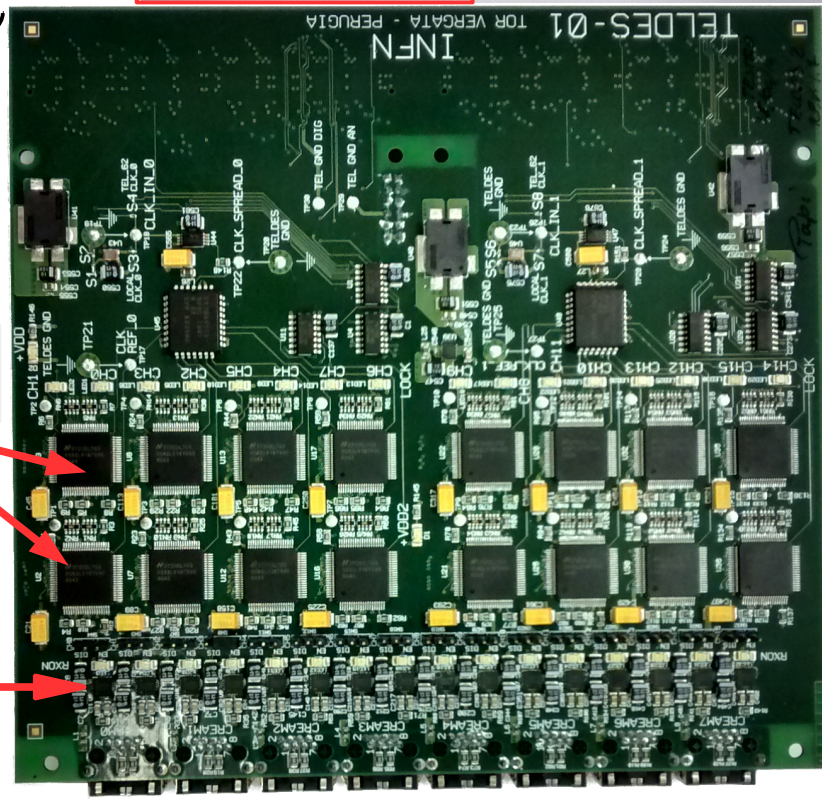
Worst-case bandwidth requirement FE → concentrator:

1.4 Gbps (**3.7 Gpbs available**)

TELDES: LKrL0 Input DESerializer







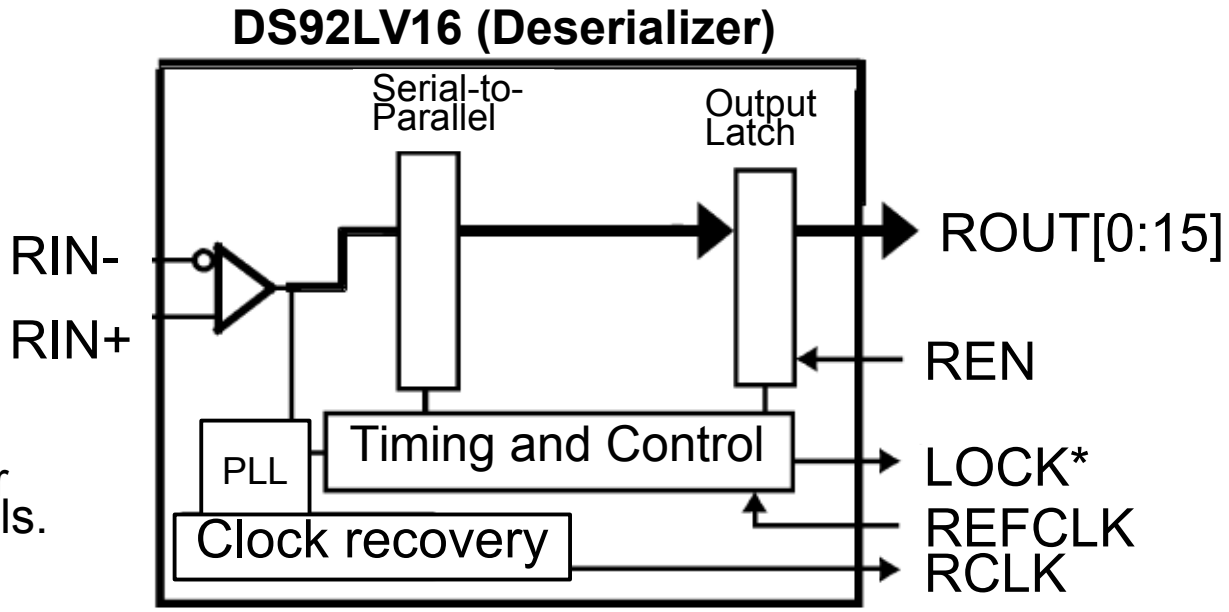
- Developed at INFN Perugia, deserializes data from Calorimeter Readout Modules.
- 2 TELDES boards per each Front-End TEL62:
  - 32 channels per TEL62;
  - 896 total.
- LVDS signals over Ethernet cables (640 Mbit/s per channel).

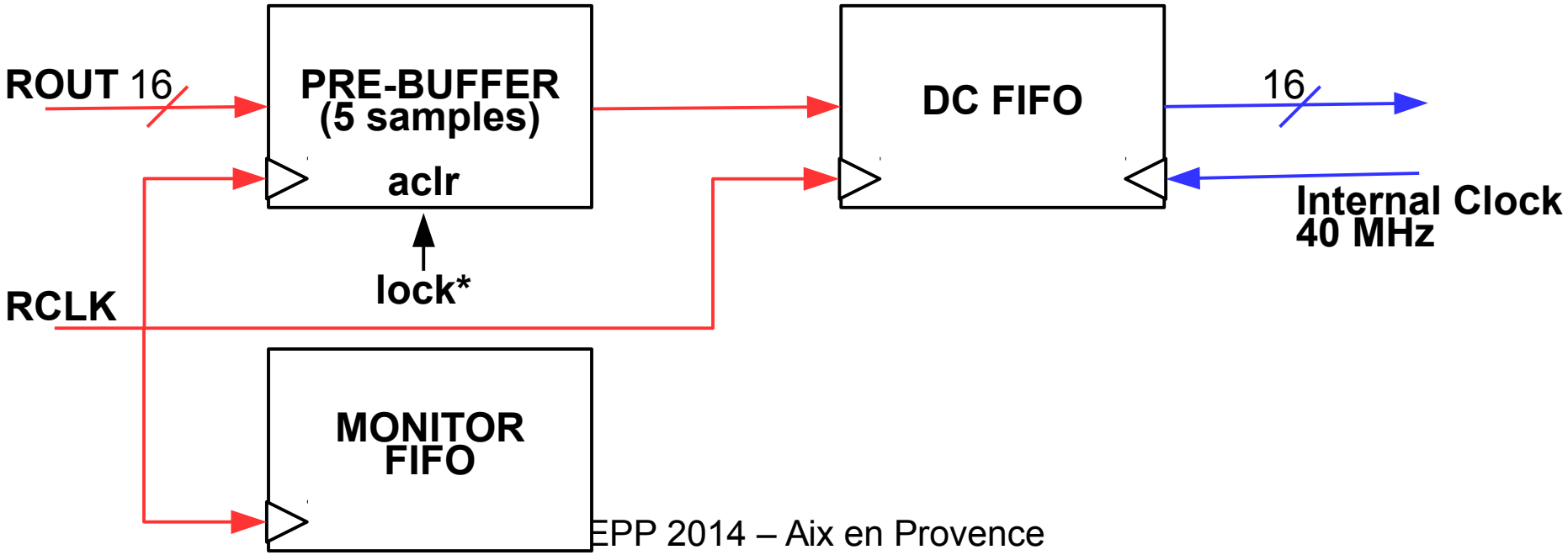
DS92LV16 deserializers

DS15EA101 equalizers

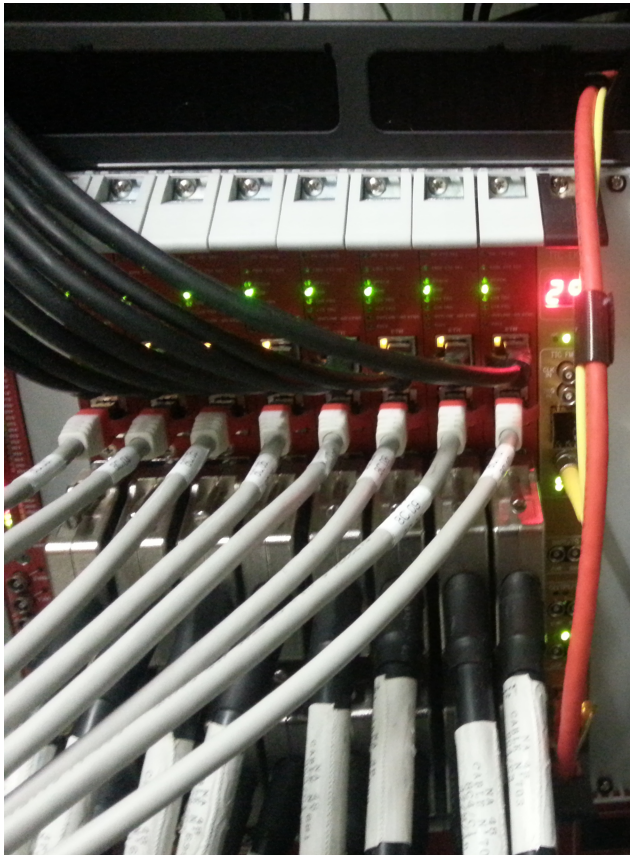
TELDES: Firmware

- 40 MHz 1:16 Derializer → 640 Mbps.
- Embedded clock (1 start + 1 stop bits).
- Deserializer recovers clock (RCLK) and data (ROUT).
- Firmware monitors deserializer lock, clock, equalizer rxon signals.

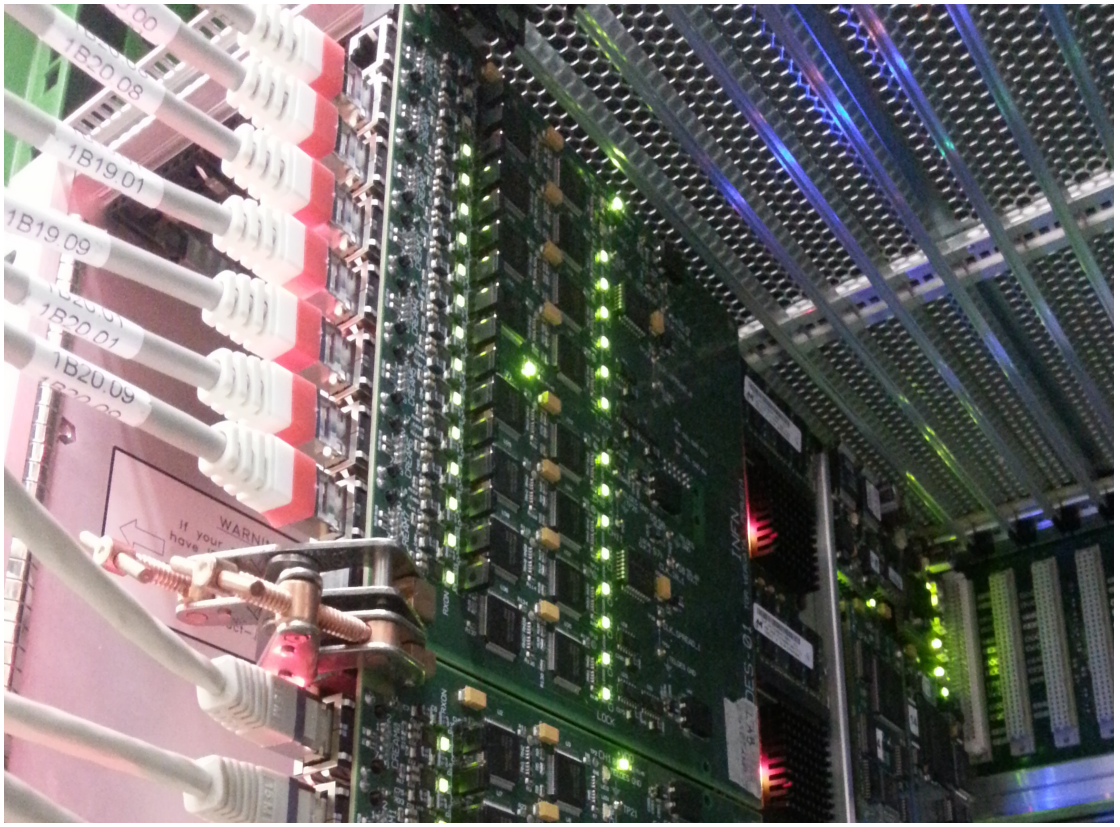




TELDES: testing



CREAM



TELDES on TEL62

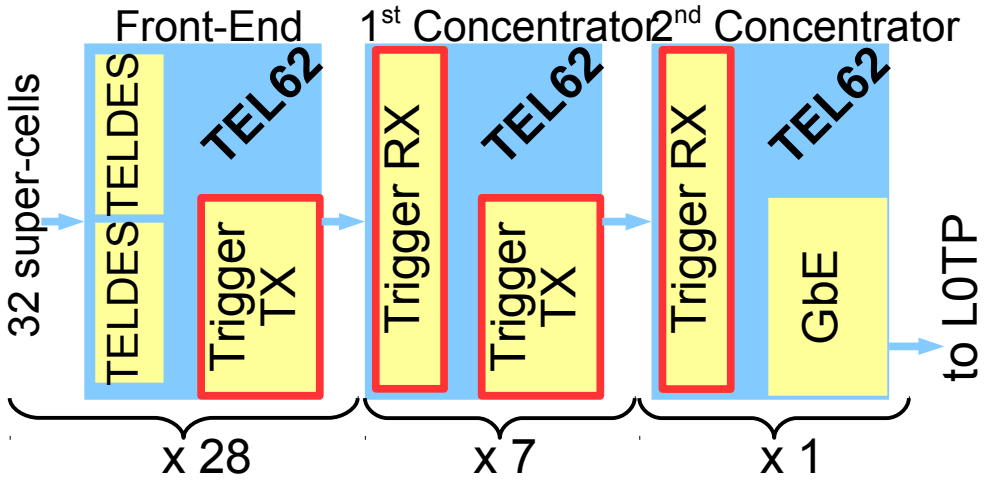
Data sent from CREAM to TEL62, checking signal lock and data values.

Unshielded cables easily pickup EMI noise → lock loss.

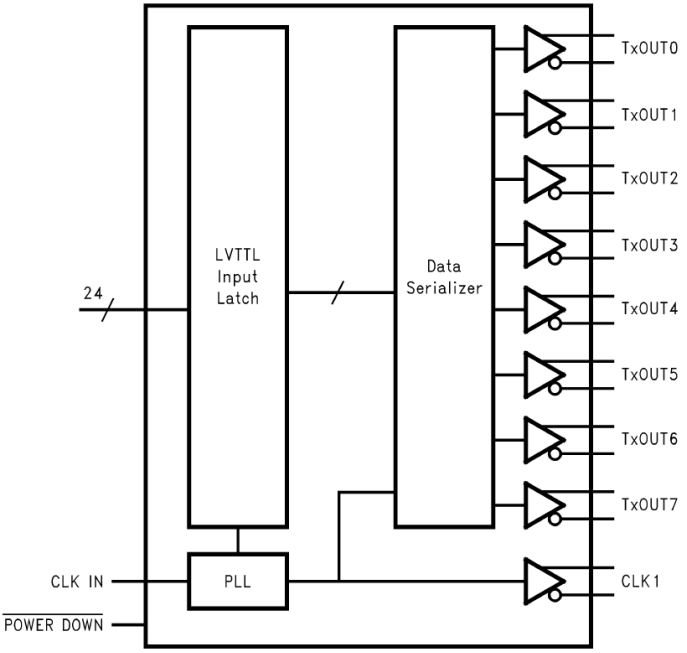
Good quality SFTP Cat. 6 cables are needed for a stable link.

Internal Transmission links

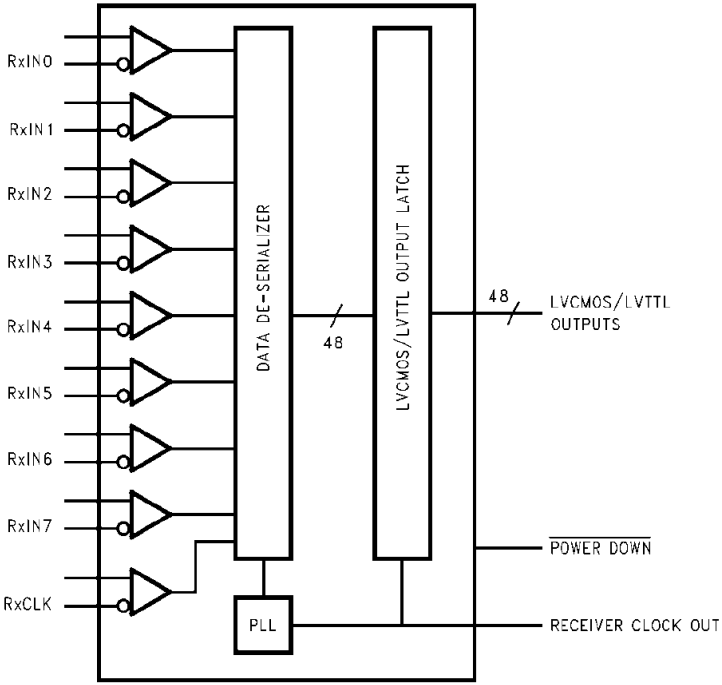
- 24 bit double edge inputs (48 bits per clock cycle).
- Serialization over 8 LVDS streams.
- Clock transmitted in parallel over a 9th LVDS link.
- 66 MHz to 133 MHz input clock → 3.2 to 6.4 Gbps.
- Optional DC balancing and pre-emphasis.



TI DS90CR485



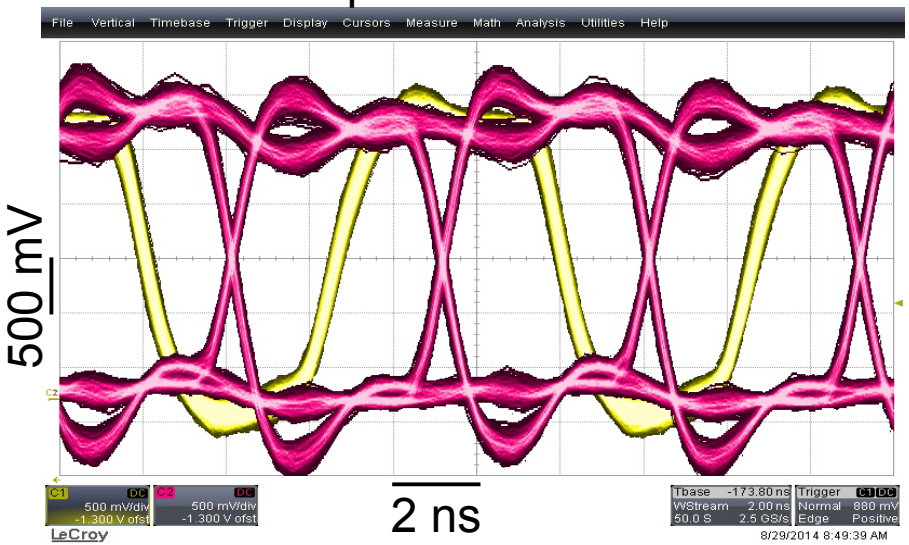
TI DS90CR486

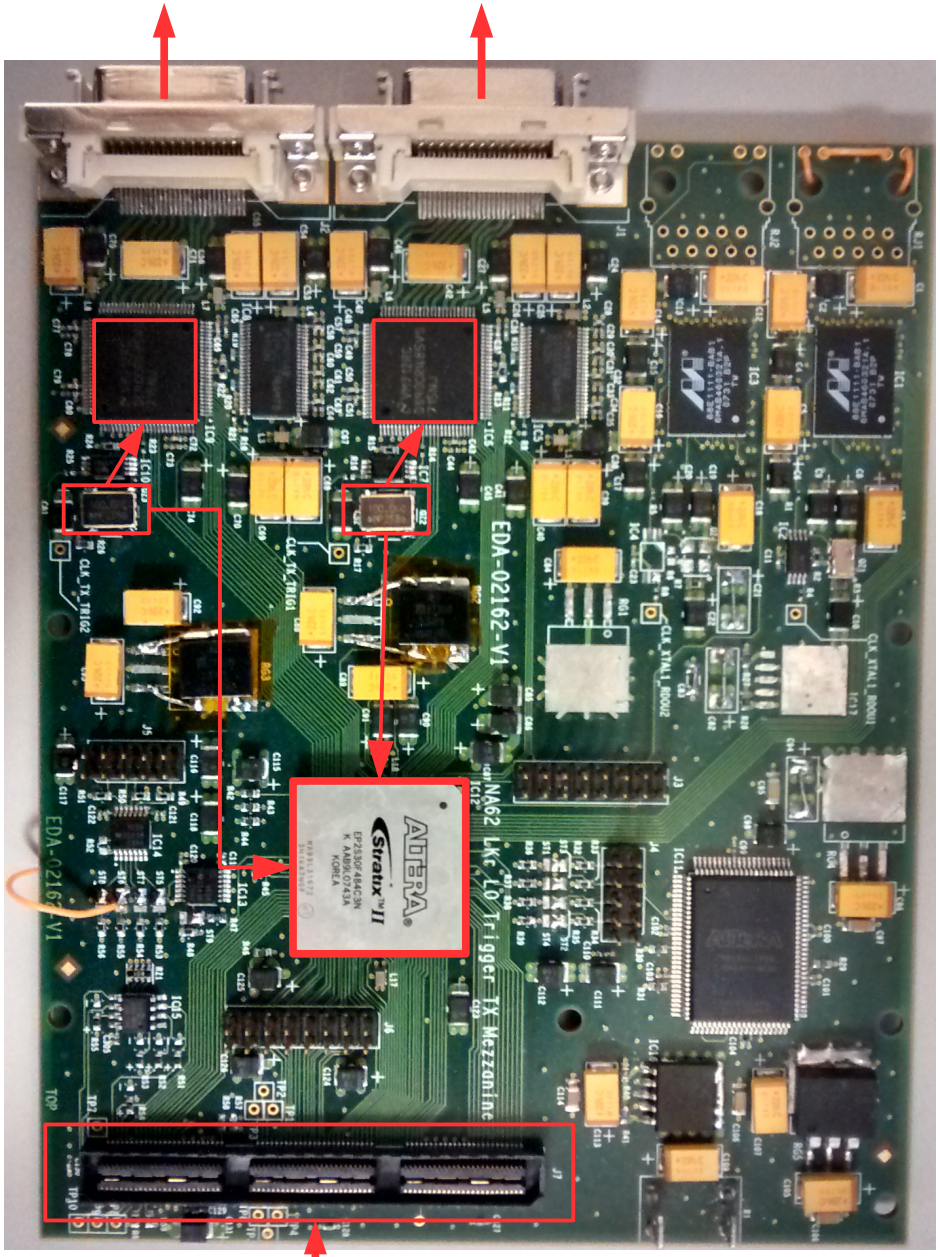


The Tx mezzanine

- 2 links, 2 DS90CR485.
- Stratix II for chip control, data buffering and DDR output.
- One external reference clock per each serializer:
  - Latches DDR data at serializer input.
  - Clocks transmission logic in the Stratix II.

Eye diagram at 100 MHz (PRBS23) at serializer input



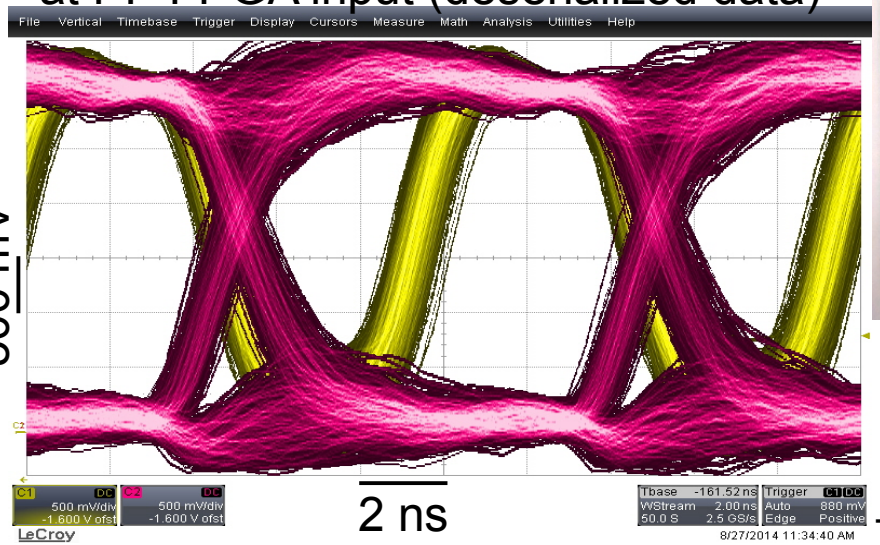


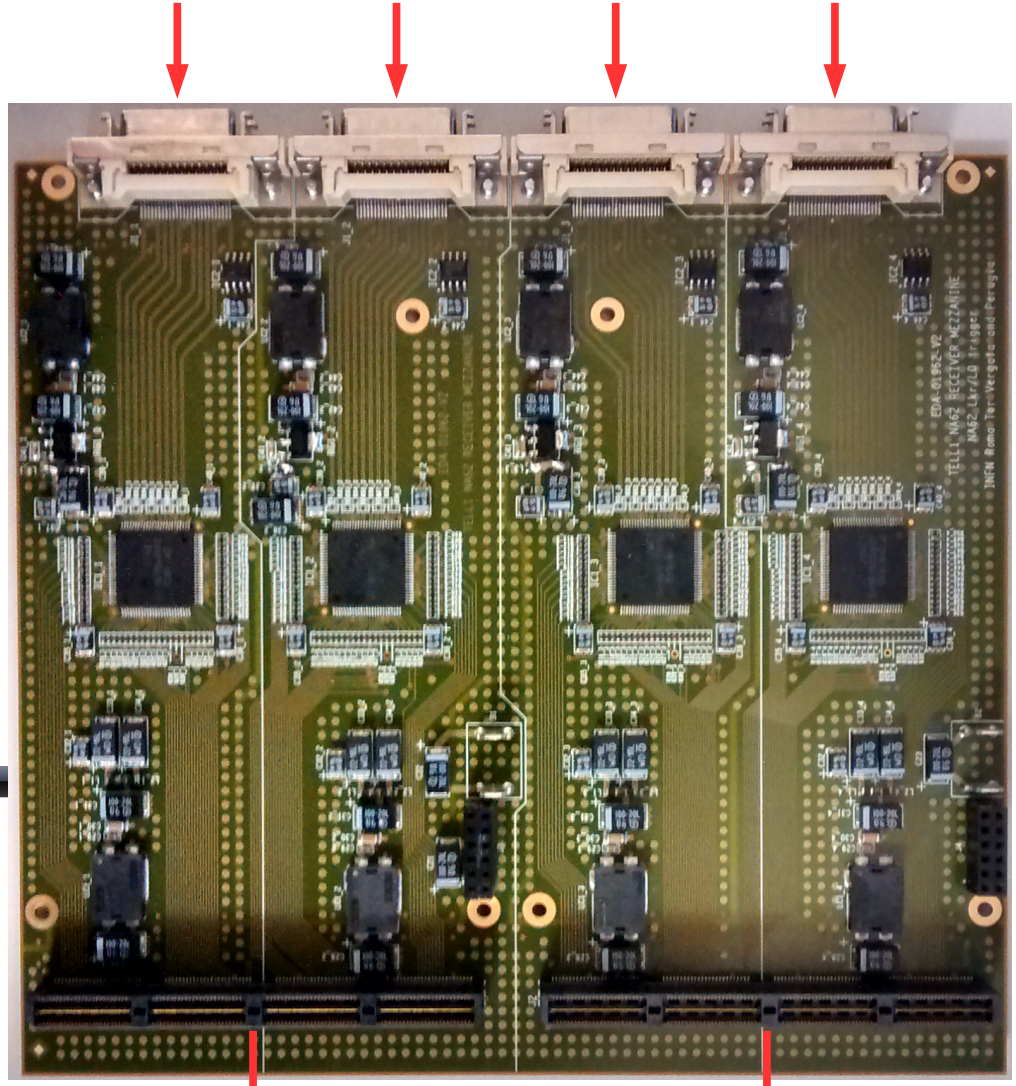
TEL62 data

The Rx mezzanine

- 4 links, 4 DS90CR486.
- Link quality (BER) dependent on:
  - Clock frequency.
  - Deskew quality (not constant).
  - Cable, connectors, soldering quality.
- Firmware:
  - Checks deskew.
  - Implements ECC.

Eye diagram at 100 MHz (PRBS23) at PP FPGA input (deserialized data)

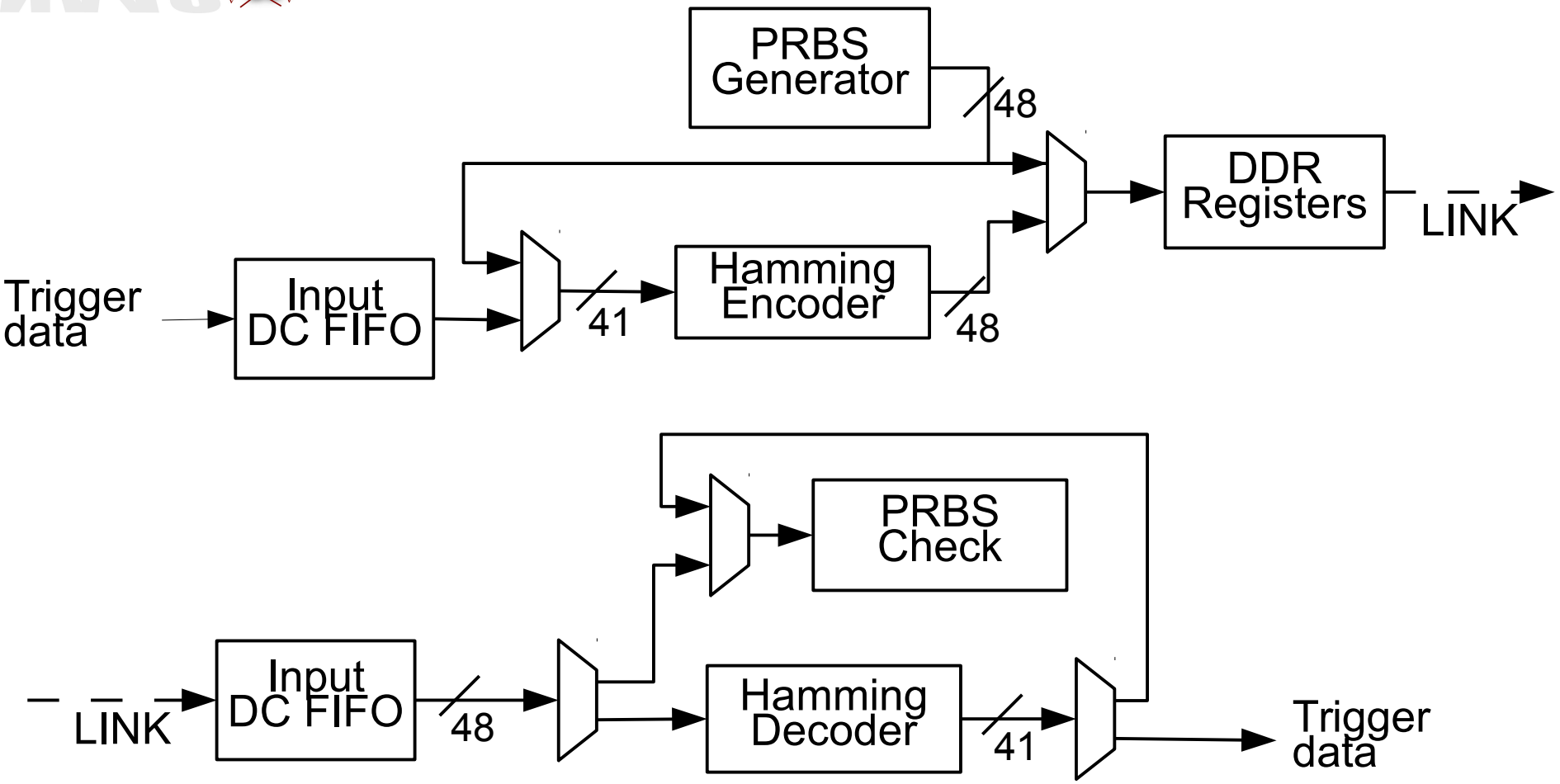




To PP0(2) FPGA

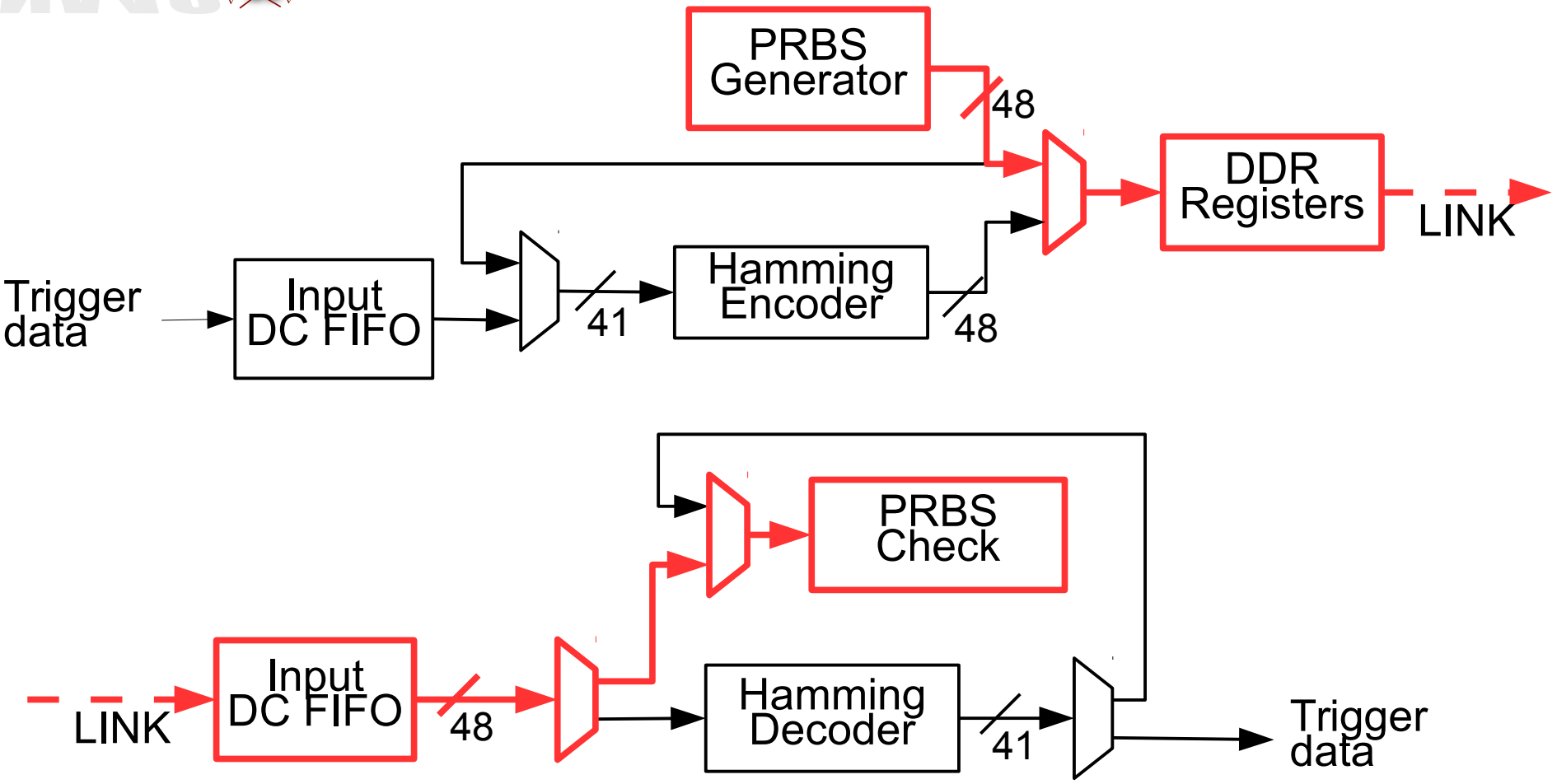
To PP1(3) FPGA

Internal Transmission: firmware



3 operational modes:
a) deskew – at power up / reset;
b) normal – for trigger;
c) Bit Error Rate Test – periodically.

Internal Transmission: firmware



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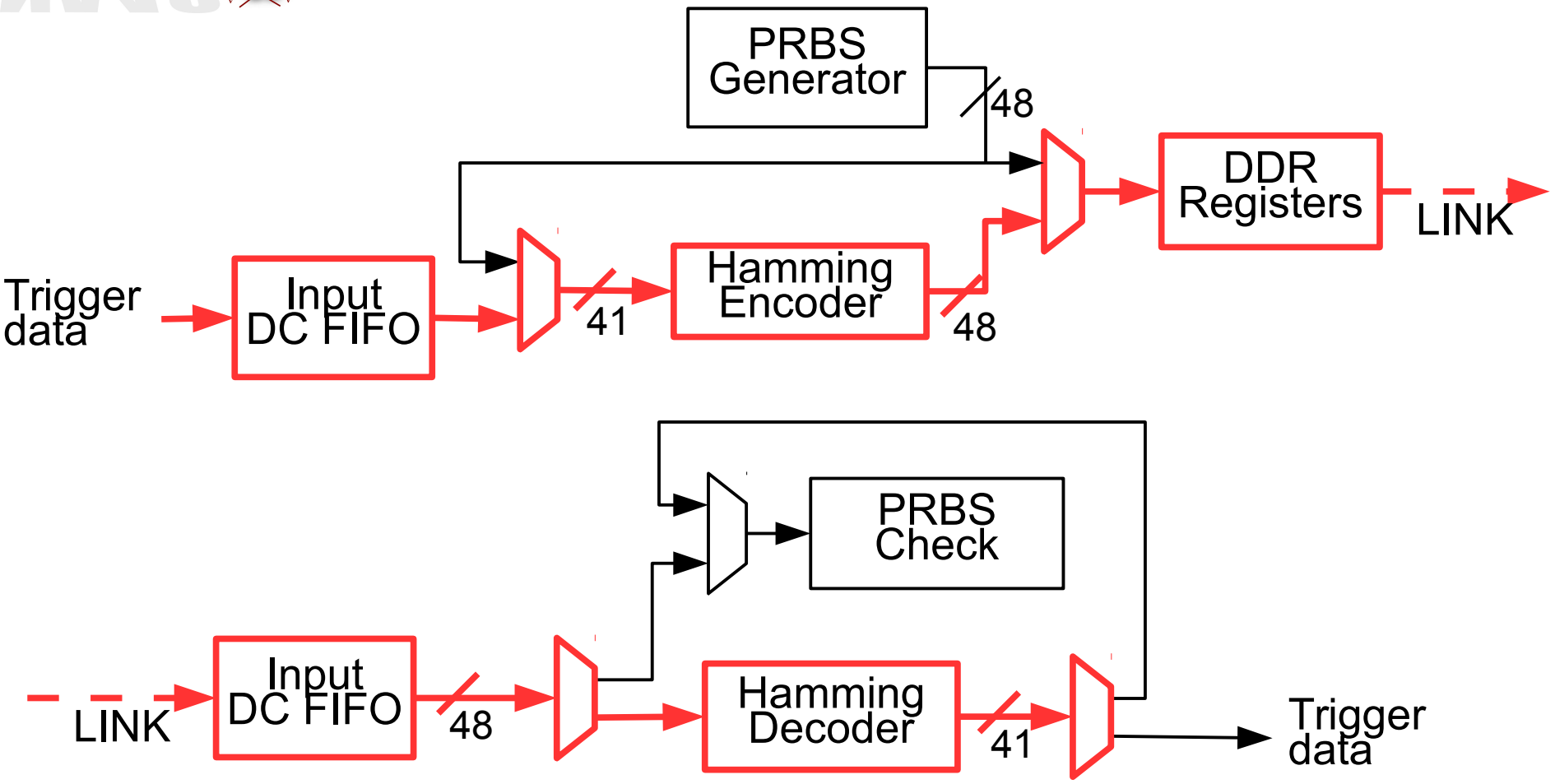

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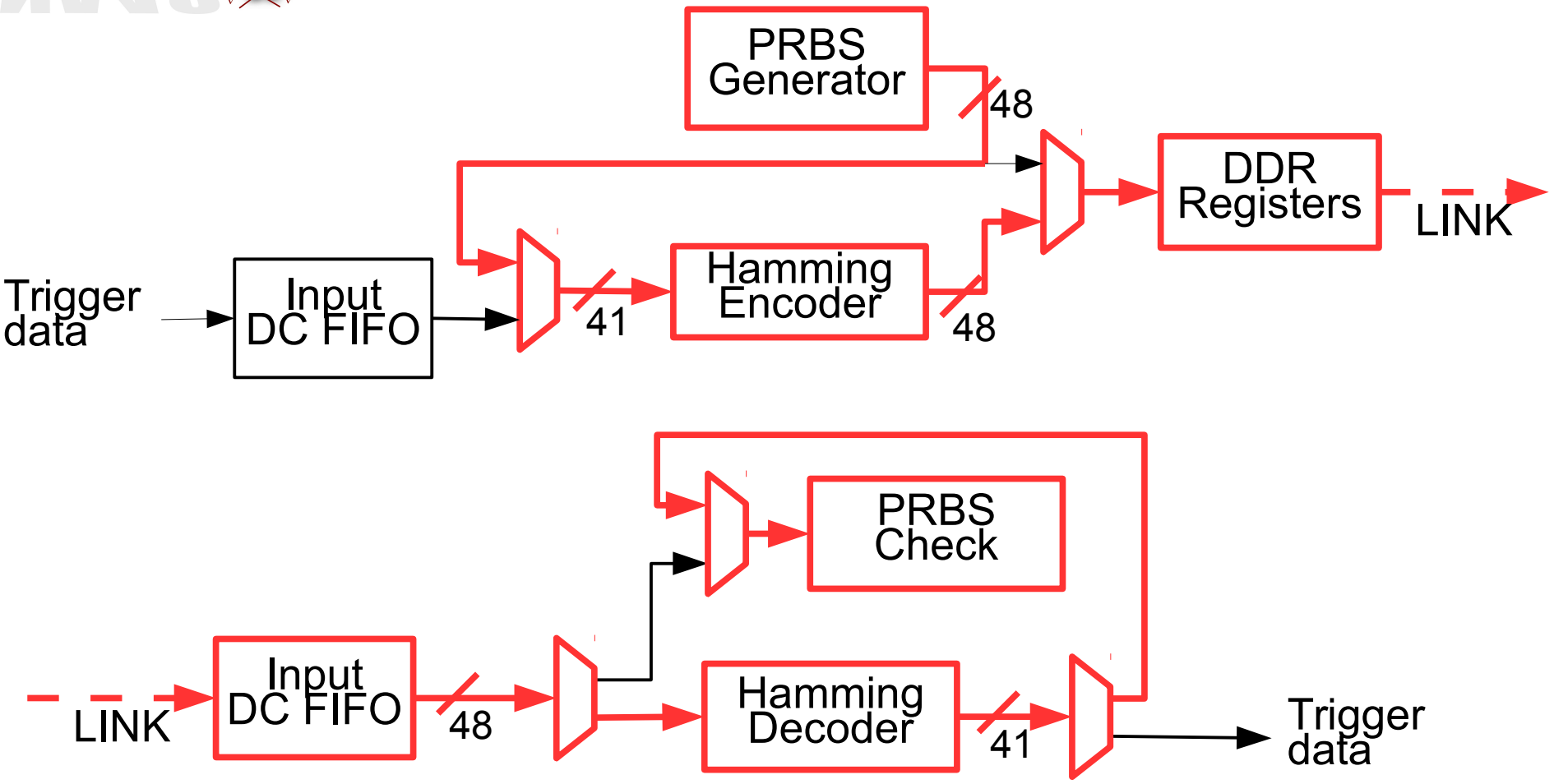
Internal Transmission: firmware



3 operational modes:

a) deskew – at power up / reset;

b) normal – for trigger;

c) Bit Error Rate Test – periodically.

Internal Transmission: BERT

Test result:

1) Up to 85 MHz:

BER < 10^{-15} (no error)

with <u>no error correction</u> from ECC.

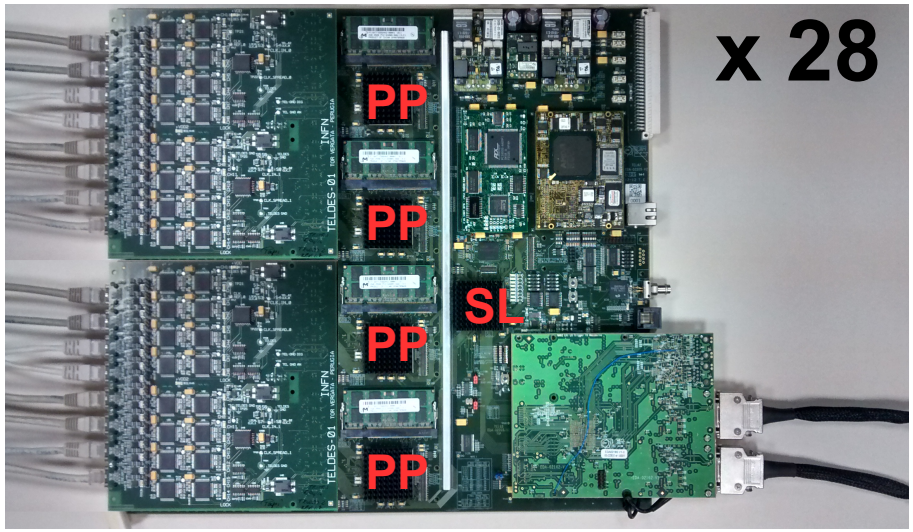
2) At 100 MHz:

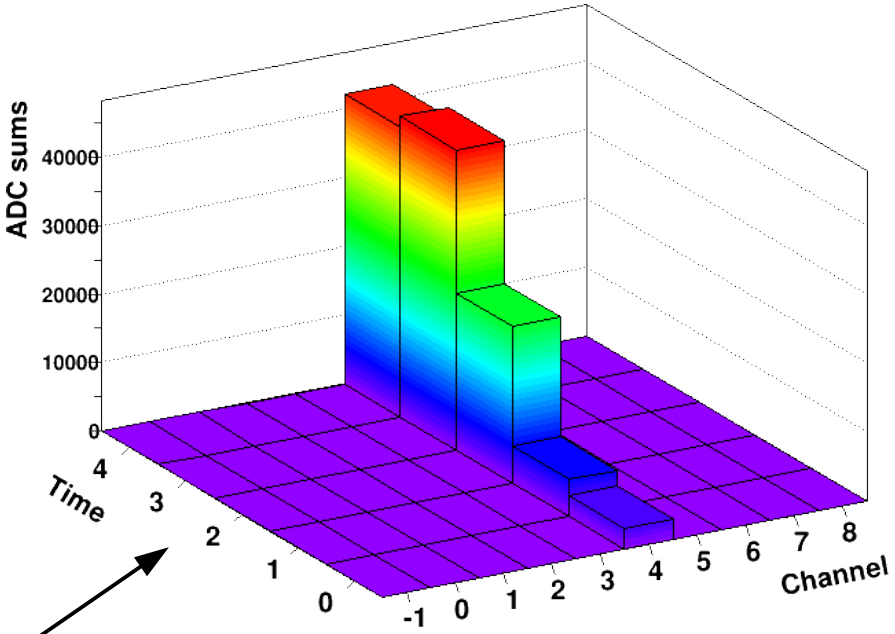
BER < 10^{-15} (no error)

with single error corrections (~ 10/s) and no double error detection.

The Test Run in October will start with 70 MHz.

Front-End layer: PP FPGA Firmware





Test Patterns

Super Cells (8 ch x 16 bit)

TELDES Interface

Peak Finder (space, time, threshold)

8 NIOS Cores (C code)

320 MHz
1.4 us latency

Peak Logic

Max Finder

Fine-time Estimation

Output to SL

40 MHz

4.2 MHz peak rate (worst)

160 MHz

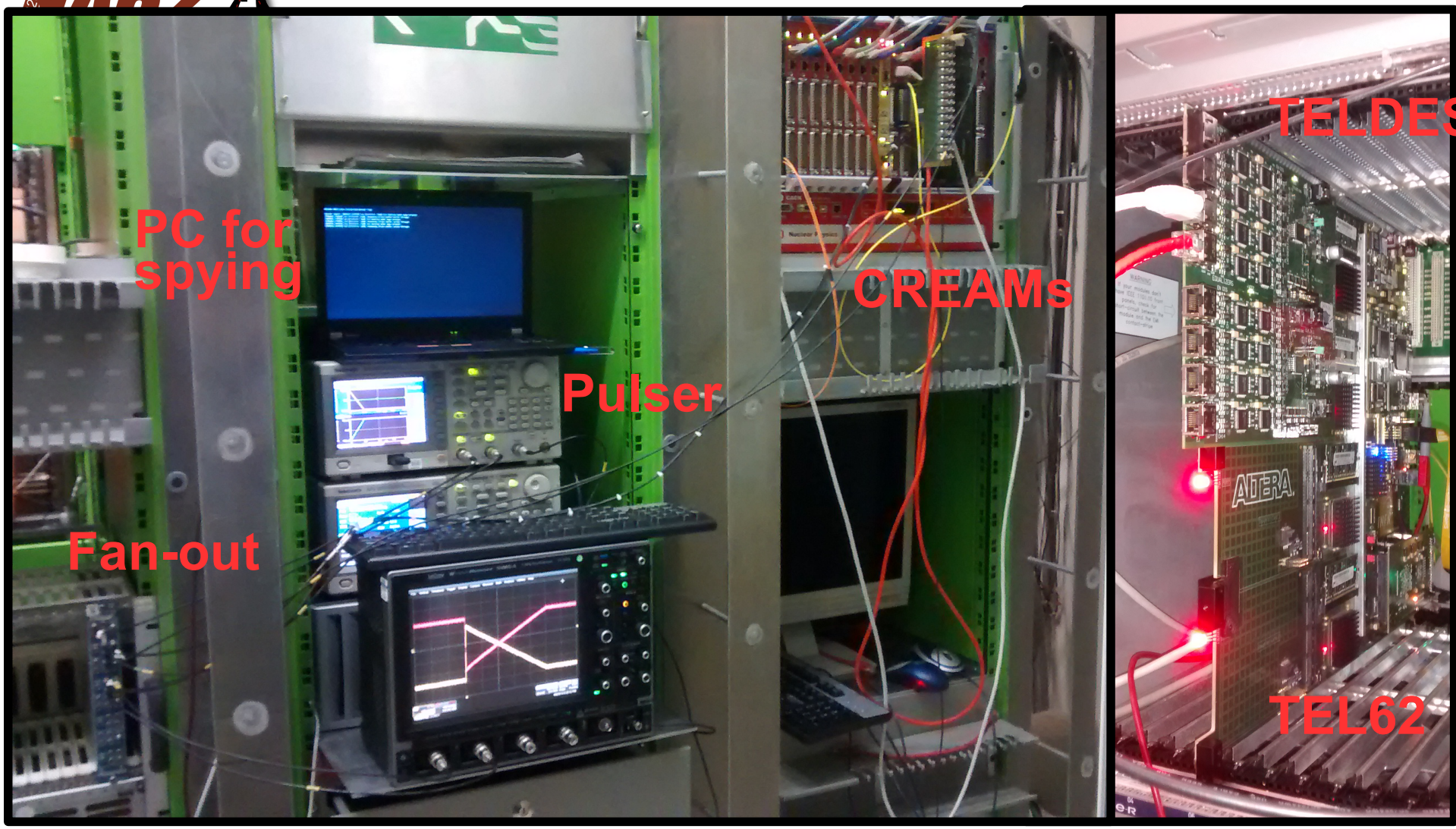
FPGA Resources Utilization (Front-End PP)

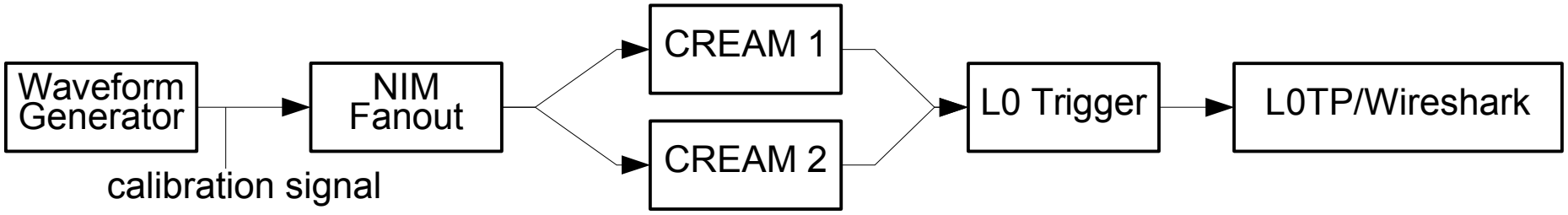
	0 NIOS	8 NIOS
Device	EP3SL200F1152C4	EP3SL200F1152C4
Timing Models	Final	Final
Logic utilization	22 %	42 %
Combinational ALUTs	15,313 / 159,120 (10 %)	41,085 / 159,120 (26 %)
Memory ALUTs	2,072 / 79,560 (3 %)	2,072 / 79,560 (3 %)
Dedicated logic registers	28,660 / 159,120 (18 %)	48,579 / 159,120 (31 %)
Total registers	28660	48579
Total pins	581 / 744 (78 %)	581 / 744 (78 %)
Total virtual pins	0	0
Total block memory bits	1,370,266 / 9,621,504 (14 %)	1,840,154 / 9,621,504 (19 %)
DSP block 18-bit elements	0 / 576 (0 %)	32 / 576 (6 %)
Total PLLs	2 / 8 (25 %)	2 / 8 (25 %)
Total DLLs	0 / 4 (0 %)	0 / 4 (0 %)

Per each NIOS core:

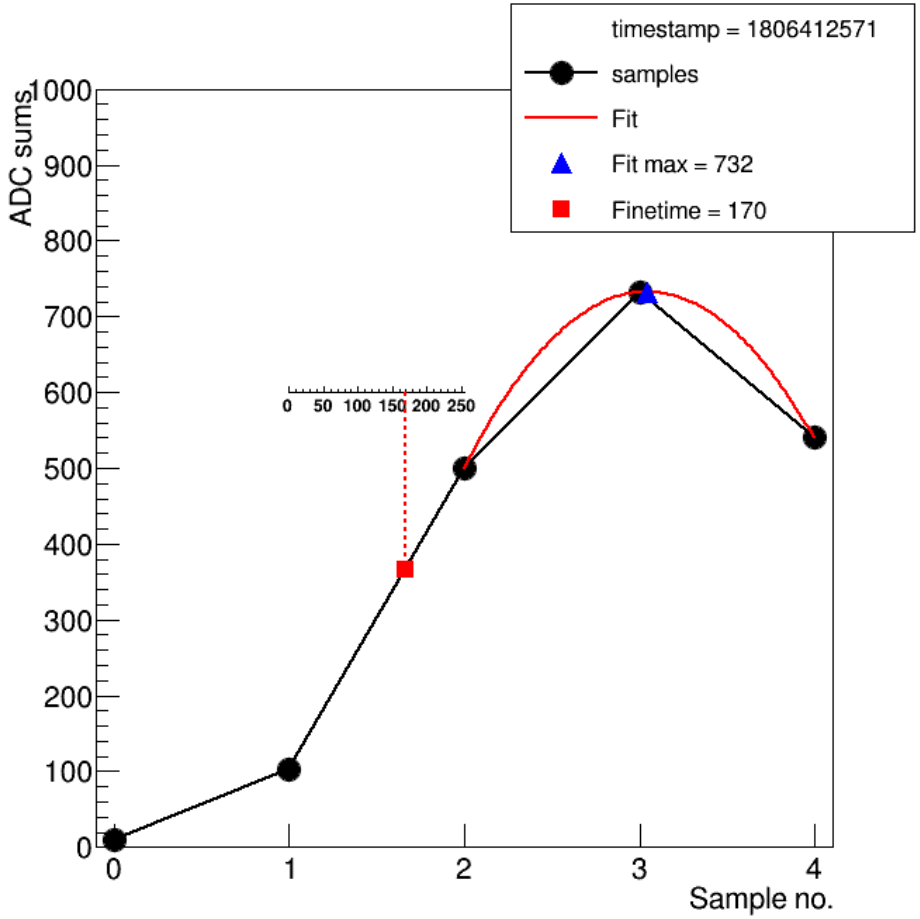
- 2.5 % logic
- 0.6 % block memory
- 4 DSP

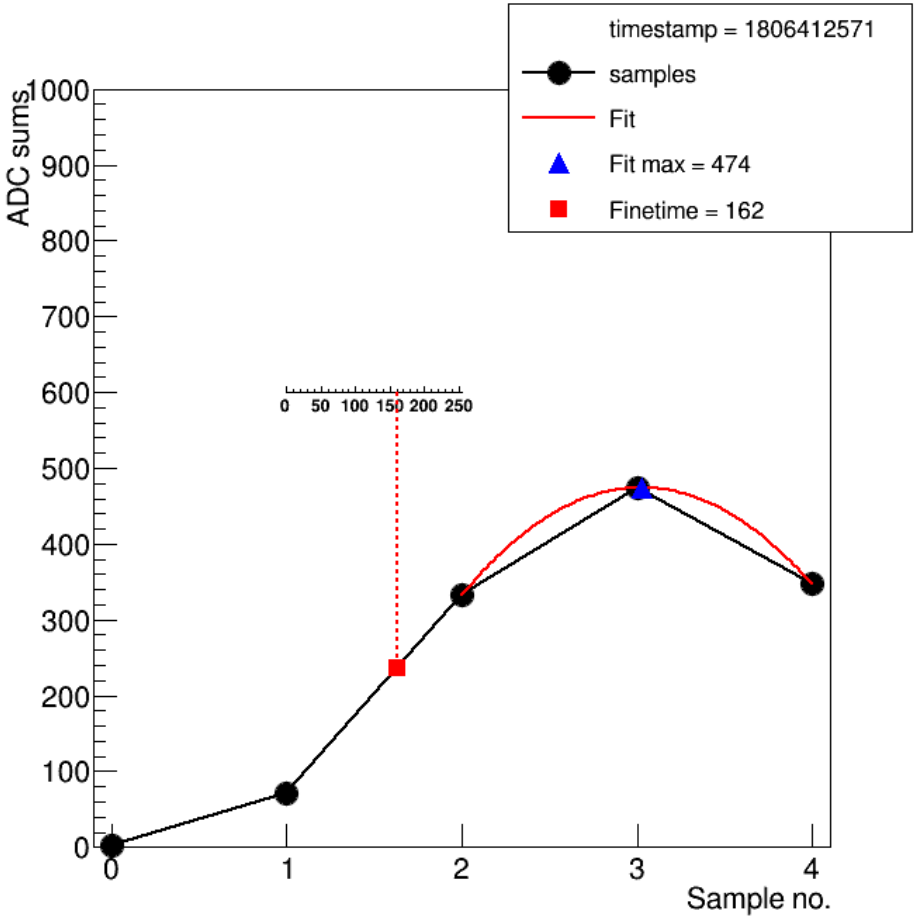
Setup


PC for spying
Pulser
Fan-out
CREAMs
TELDES
ALTERA
TEL62

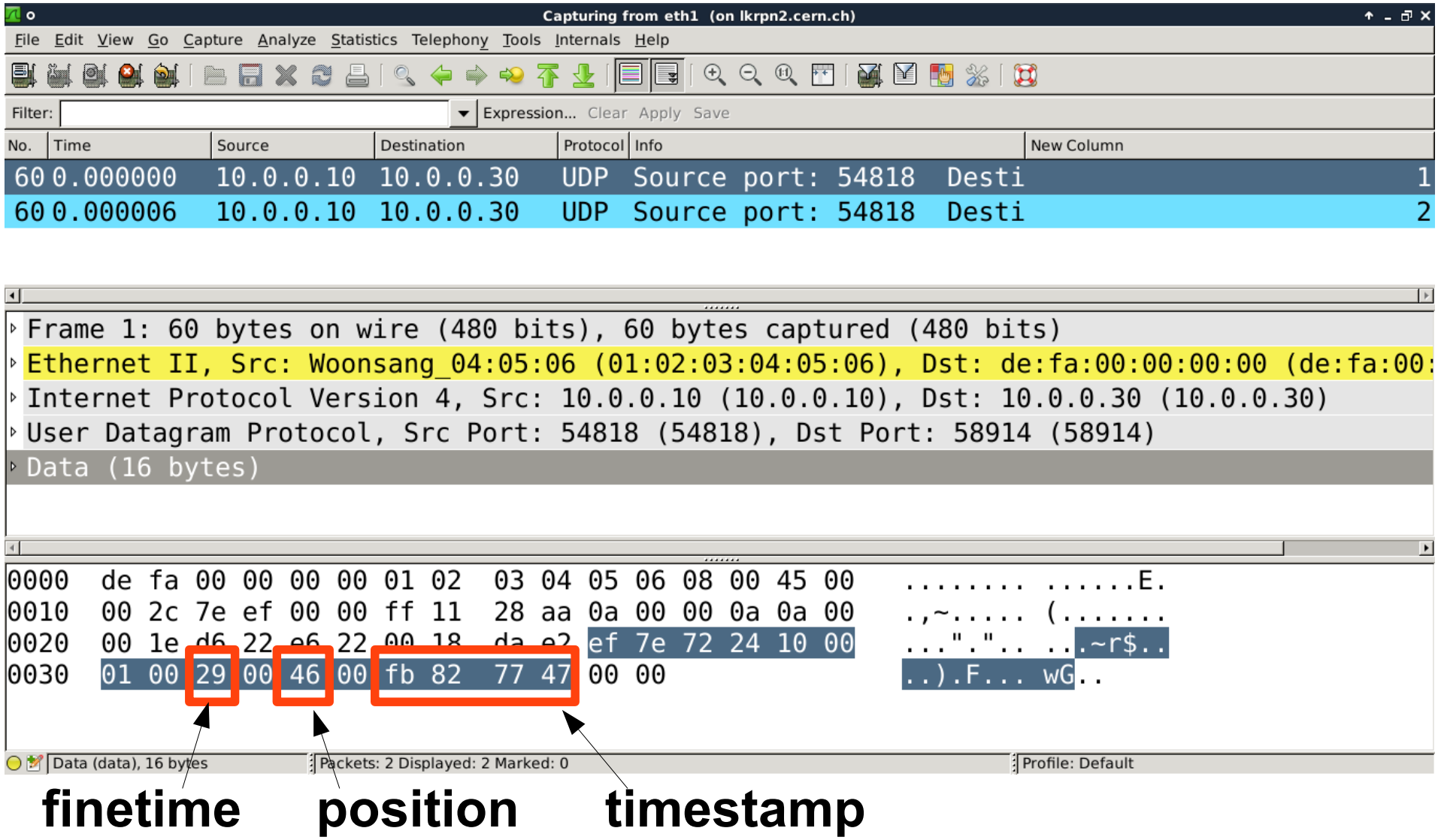

Waveform Generator
NIM Fanout
CREAM 1
CREAM 2
L0 Trigger
L0TP/Wireshark
calibration signal

Peak max and fine-time estimation



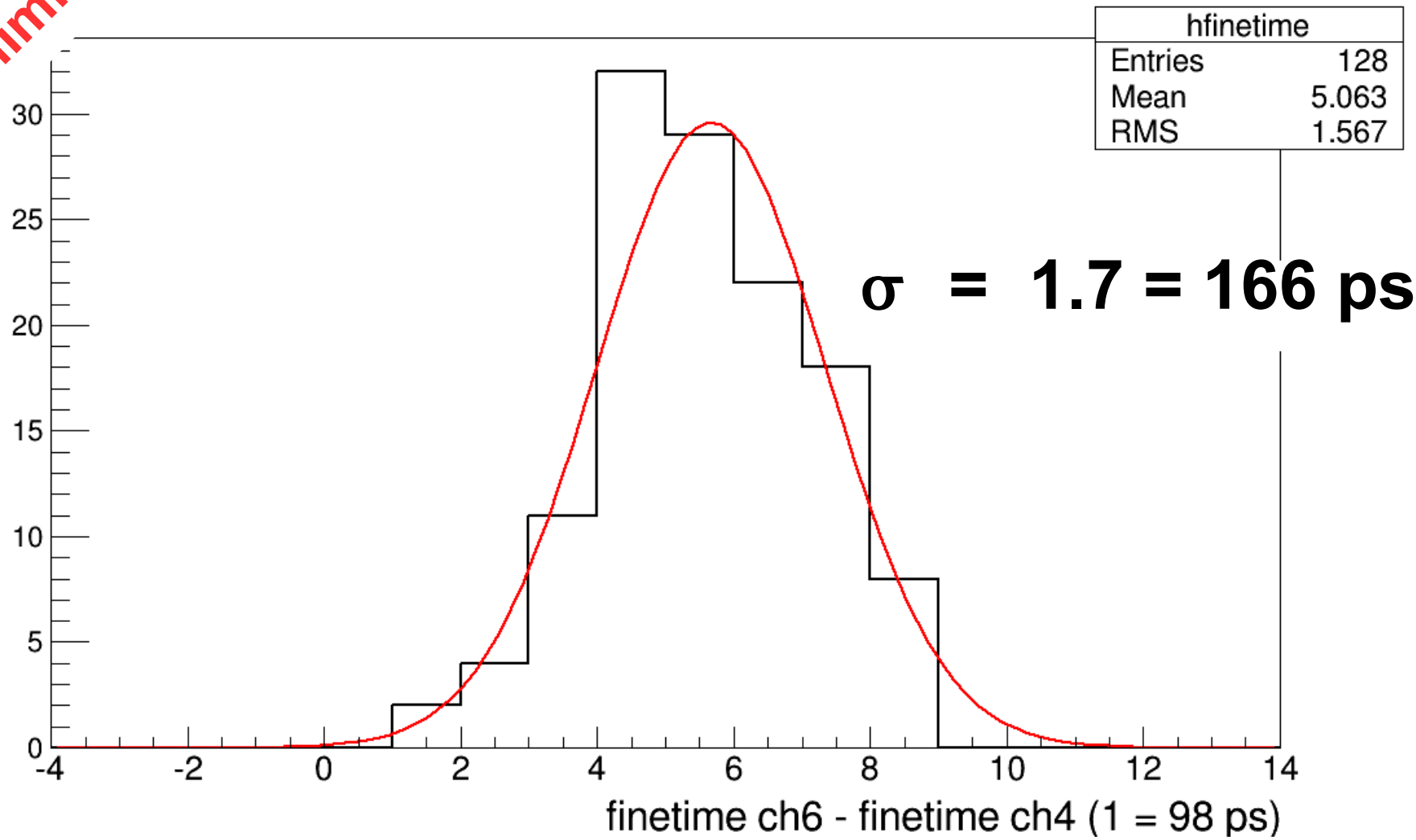


Test primitives (Wireshark capture)



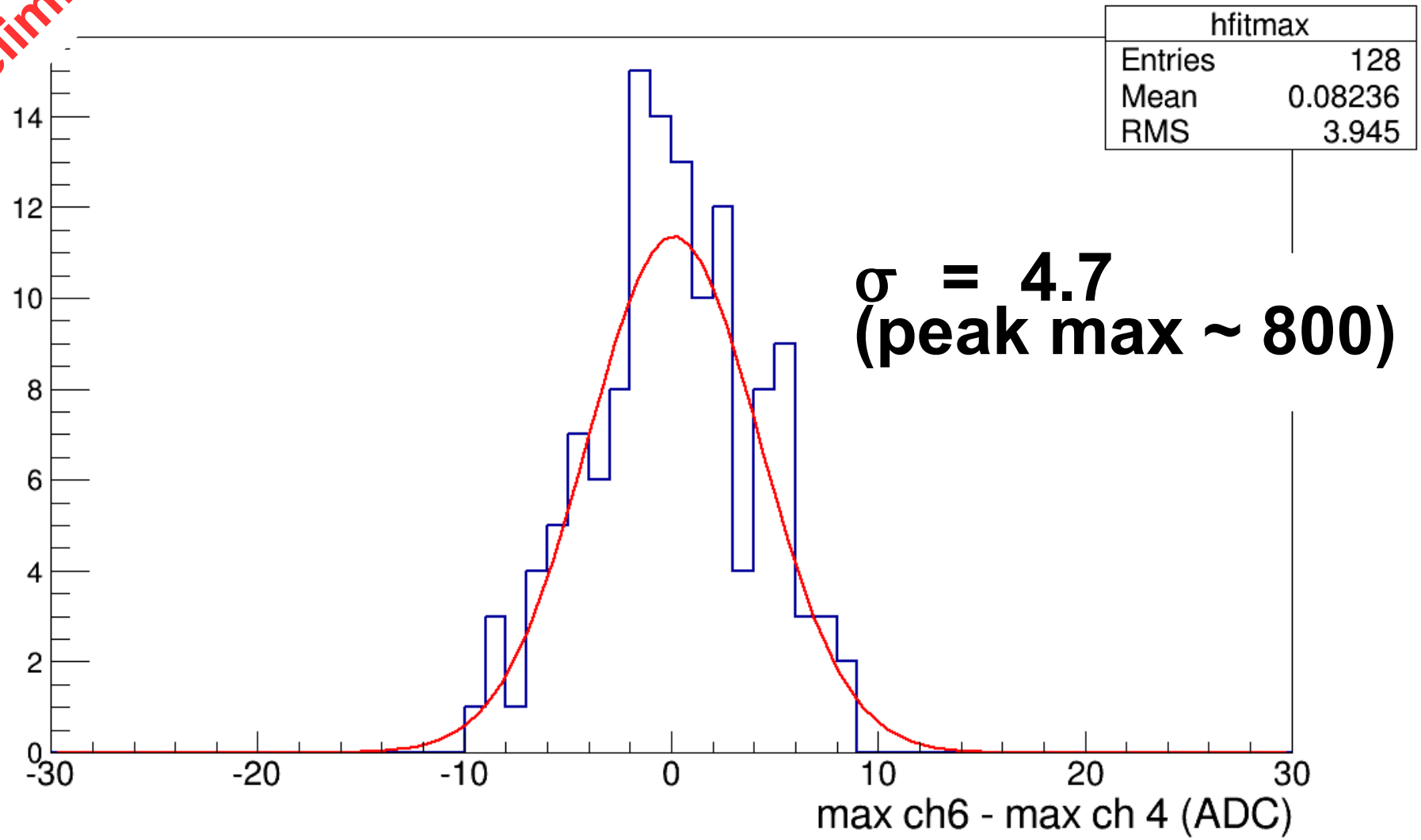
Finetime resolution

Preliminary

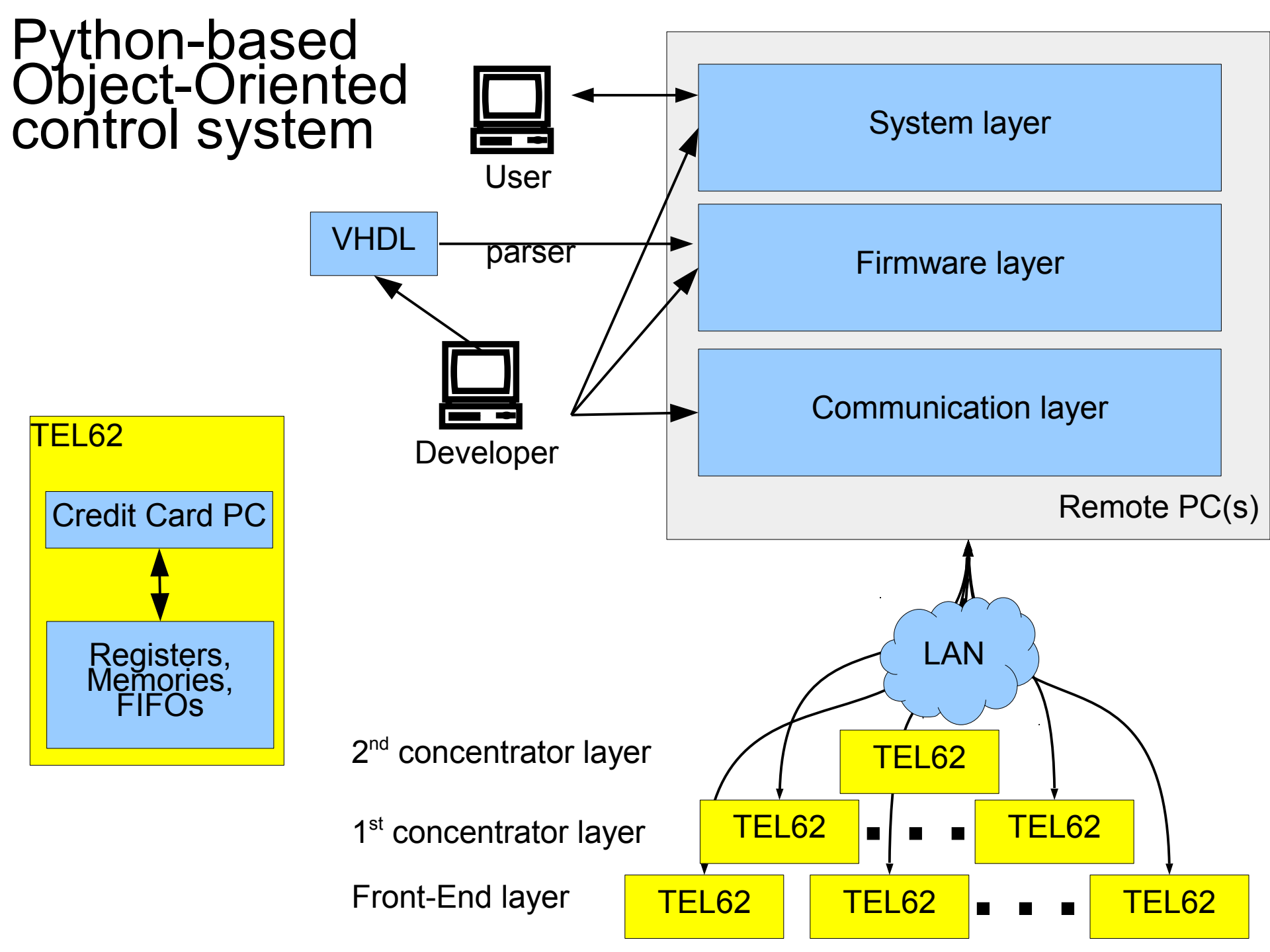


Energy Resolution (fit max)

Preliminary



Python-based Object-Oriented control system



Conclusions

- LKR L0 hardware tested and ready for commissioning.
- We have good preliminary estimations of finetime and energy resolution of the system.
- Test run goals:
  - commisioning and test of all detector components;
  - aiming at stable data taking.