Contribution ID: **125** Type: **Oral**

Development of Front-end Electronics for LumiCal Detector in CMOS 130 nm Technology

Wednesday 24 September 2014 14:00 (25 minutes)

The design and preliminary measurement results of a multichannel, variable gain front-end electronics for LumiCal detector at future Linear Collider are presented. The 8-channel prototype was designed and fabricated in a 130 nm CMOS technology. Each channel comprises a charge sensitive preamplifier and CR-RC shaper with pole-zero cancellation circuit. Measurement results confirm full functionality of the prototype and compliance with all requirements imposed by the detector specification. Power consumption of the front-end is around 1.5 mW per channel with 50 ns peaking time and noise ENC below 900 e^-.

Summary

In the very forward region of a future Linear Collider a special kind of calorimeter is foreseen - the Luminosity Calorimeter (LumiCal). The LumiCal will measure the luminosity with a precision of better than 0.001 at 500 GeV centre-of-mass energy and 0.003 at 1 TeV centre-of-mass energy. The sandwich type calorimeter consist of tungsten absorber disks of 3.5 mm thickness, corresponding to one radiation length, interspersed with sensor layers. Each sensor layer is segmented radially and azimuthally into pads. Due to the high occupancy originating from beamstrahlung and two-photon processes, the LumiCal needs a fast readout.

The variable gain, 8-channel front-end electronics was developed for the LumiCal. The ASIC was designed, simulated and fabricated in 130 nm CMOS technology. Each channel comprises a charge sensitive preamplifier and a CR-RC shaper with pole-zero cancellation circuit. The shaper peaking time of about 50 ns was chosen to fulfill the timings requirements. Two charge gain modes were implemented - the physics mode and the calibration mode. In the physics mode (low gain) the detector should be sensitive to electromagnetic showers resulting in a high energy deposition and the front-end should process signals up to about 6 pC per channel. In the calibration mode (high gain) it should detect signals from relativistic muons, i.e. should be able to register the minimum ionizing particles (MIPs). The proposed sensor geometry results in a wide range of capacitive load (5 pF - 35 pF) connected to a single front-end channel. Because of expected high occupancy per channel, the front-end should be fast enough to resolve signals from subsequent beam bunches separated in time of about 350 ns. Severe requirements on power dissipation of readout electronics may be strongly relaxed if the power is switched off between bunch trains, i.e. the power pulsing is applied. This is feasible since in the ILC experiment 200 ms pause is foreseen after each 1 ms length bunch train. The power pulsing was implemented in the designed prototype.

Measurements show that the ASIC is functional and fulfils the requirements. The measured charge gain in the calibration mode is around 4.23 mV/fC, with dynamic range up to 100 fC, and 0.1 mV/fC in the physics mode, with dynamic range up to 6 pC. The peaking time of around 52 ns was obtained in both modes. The designed front-end works with detector capacitance in the range of 0 to 50 pF. The measured noise ENC at 10 pF detector capacitance is below 900 e^- which gives the signal to noise ratio (SNR) above 20. The measured power consumption of the prototype is around 1.5 mW per channel at typical biasing. Using the power pulsing, with a duty factor of 1/200, the average power consumption is reduced to around 10 μW per channel. After power cycling the ASIC recovers completely within 1 us.

Authors: MORON, Jakub (AGH University of Science and Technology (PL)); SWIENTEK, Krzysztof Piotr (AGH University of Science and Technology (PL)); IDZIK, Marek (AGH University of Science and Technology (PL)); FIRLEJ, Miroslaw (AGH University of Science and Technology (PL)); FIUTOWSKI, Tomasz (AGH University of Science and Technology)

Presenter: MORON, Jakub (AGH University of Science and Technology (PL))

Session Classification: ASICs

Track Classification: ASICs