The VFAT3-Comm-Port : A complete communication port for front-end ASICs intended for use within the high luminosity radiation environments of the LHC.

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1. ABSTRACT:

Intended for use within the VFAT3 ASIC; the VFAT3 Comm-Port (V3CP) offers a single port for all communication to and from a front-end ASIC within the HL-LHC environment. This includes synchronization to the LHC clock, slow control communication for chip set-up, bias and monitoring, the execution of fast control commands and the readout of data. The poster presents the core design which could be considered generic and used as an IP block in other projects, describes the use encoding which allows robust communication reducing the risk of errors, possibly induced by Single Event Effects (SEE) and shows the specific implementation of the Comm-Port within the VFAT3 chip.

2. INTRODUCTION:

The CMS GEM upgrade plans to use the the GigaBit Transceiver (GBTX)[1] as the chip set for optical reception and transmission of all data in and out of the system. The GBTX then communicates with front-end chips via e-links[2].

The V3CP is designed to be compatible with the GBTX chip in that it receives and transmits, clock and data over three differential pairs running at 320Mbps. Figure 2.1 shows the VFAT3 chip connected to the GBTX via three e-links.

Four basic functions of VFAT3-Comm-Port (V3CP) can be distinguished :

- Reception of serial data via e-links.
- Synchronization of an internal 40MHz clock to the LHC machine clock.
- Execution of Fast Synchronous Control Commands (FSCCs).
- Transmission of data from a chip over e-links.

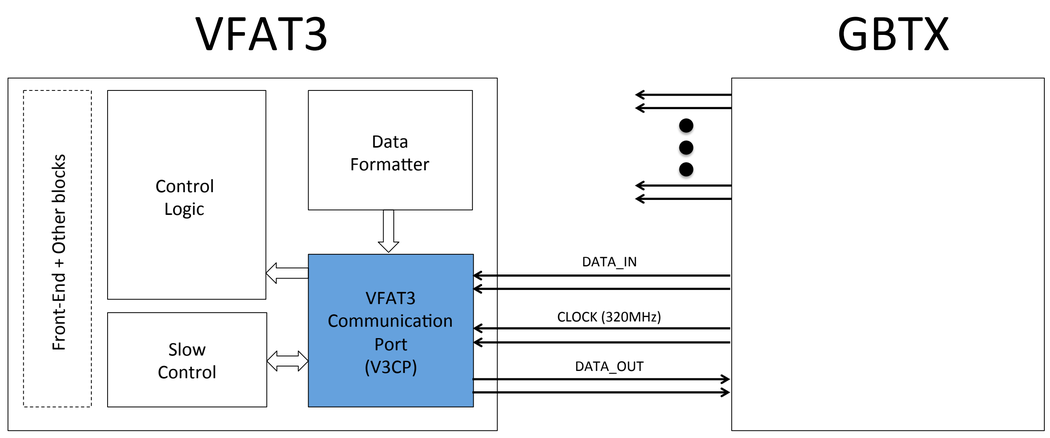

FIGURE 2.1: The connection between the VFAT3 chip and the GBT chip in the CMS GEM Data-acquisition system[3].

3. GENERIC ARCHITECTURE:

The input data to the V3CP is encoded using a 4-to-8bit encoding scheme. The coding provides 16 unique characters and two unique comma characters[4] (listed in Table 3.1) and is based on the theory developed by R. Hamming[5]. It provides Single Error Correction (SEC) and Double Error Detection (DED) provided that the phase of the internally generated clock is properly synchronized.

Name	4-bit word	8-bit representation	Disparity
A	0000	00000000	-4
B	0001	00001111	0
C	0010	00110011	0
D	0011	00111100	0
E	0100	01010101	0
F	0101	01011010	0
G	0110	01100110	0
H	0111	01101001	0
I	1000	10010110	0
J	1001	10011001	0
K	1010	10100101	0
L	1011	10101010	0
M	1100	11000011	0
N	1101	11001100	0
O	1110	11110000	0
P	1111	11111111	+4
CC-A		00010111	0
CC-B		11101000	0

TABLE 3.1: Set of characters transmitted down to the V3CP.

Such encoding does not only increase the robustness of input data to errors that can appear on the transmission lines but also increases their robustness against SEEs and SEUs after they are latched and processed inside a chip. The code has also a low-disparity.

The system operates on a fixed latency control path i.e. the data will arrive at at chip at a known time synchronous to the system clock. Therefore, the V3CP port needs to be synchronized. This is achieved by the sending of a robust synchronization pattern. The synchronization pattern is 24-bits long and is composed of three consecutive unique comma characters (CC-A). Synchronization can also be verified by sending an additional unique comma character (CC-B).

4. VFAT3 SPECIFIC ARCHITECTURE:

In the specific implementation for the VFAT3 the unique characters are treated as Fast Synchronous Control Commands (FSCCs). VFAT3 uses them for purposes such as the LV1A (Level one trigger), reset of chip's internal registers or initialization of internal counters. The complete set of FSCCs is listed in Table 4.1.

FSCC	Character	Function
EC0	B	Reset of the Event Counter (EC).
BC0	C	Reset of the BCZ Counter (BC).
CalPulse	D	Injection of the Calibration Pulse.
ReSync	E	Resets all VFAT3 state machines.
SCOnly	F	Force "Slow Control Only" Mode.
RunMode	G	Return from "Slow Control Only" Mode.
LV1A	H	First Level Trigger.
SC0	I	Sends "0" to the Slow Control.
SC1	J	Sends "1" to the Slow Control.
ReSC	K	Reset of Slow Control.
LV1A+EC0	L	First Level Trigger and reset of the EC.
LV1A+BC0	M	First Level Trigger and reset of the BC.
LV1A+ EC0+BC0	N	First Level Trigger and reset of the EC and the BC.
EC0 + BC0	O	Reset of the EC and the BC.

TABLE 4.1: List of the Fast Synchronous Control Commands (FSCCs).

Communication with the Slow Control is also embedded into the FSCCs. Such a solution allows the user to send and receive Slow Control commands with the effective bandwidth of 40Mbps, which is significantly faster than the standard communication scheme through I2C.

During the transmission of data from the chip, the V3CP produces headers to differentiate between different types of data, ie. tracking data, slow control data and fillers.

5. MICRO-ARCHITECTURE:

Figure 5.1 shows the block diagram of the V3CP and its connection to other VFAT3 internal blocks. The V3CP comprises five different blocks, namely: Receiver, Clock Divider, Transmitter, 8-to-4-bit decoder and Data Controller. The first four blocks are general VC3P components, whereas the latter one was specifically implemented for the use within the VFAT3 chip.

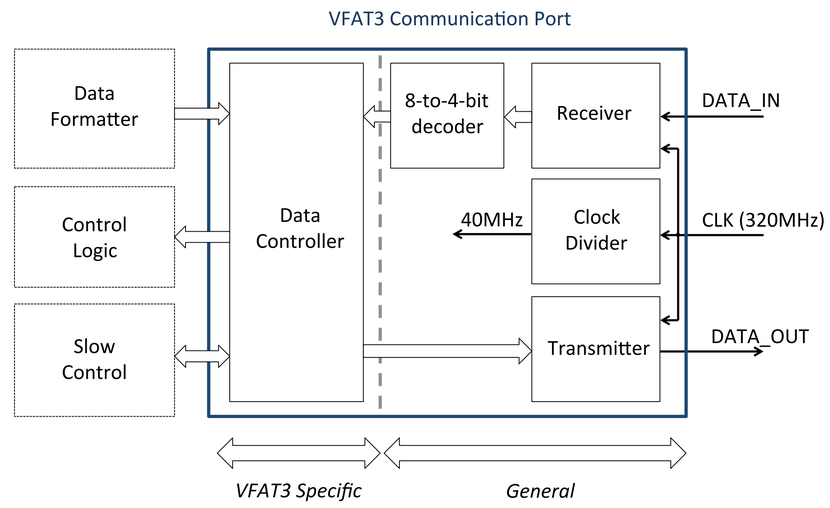

FIGURE 5.1: The micro-architecture of the V3CP and its connection to other VFAT3 internal blocks.

6. CONCLUSION:

The VFAT3-Comm-Port (V3CP) is a complete communication port, designed to provide a communication for readout of front-end ASICs, particularly VFAT3, working in demanding radiation environments and to be compatible with the GigaBit Transceiver (GBTX) chip. The port provides a communication protocol which enables an easy synchronization of a chip within a large system and adds robustness against SEEs and SEUs that can occur during transmission. Its specific implementation in the VFAT3 allows the communication with the Slow Control with an effective bandwidth of 40Mbps, which can decrease the time that is needed for the chip characterization, system setup and system calibration. For robustness against SEUs and SEEs, the V3CP logic was triplicated.

7. REFERENCES:

[1] K.Willey et al. "A Gigabit Transceiver for Data Transmission in the Future High Energy Physics Experiments", Physics Procedia 37(2012) p. 1561-1568.

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