Contribution ID: **58** Type: **Poster**

The VFAT3-Comm-Port : A Complete Communication Port for Front-end ASICs Intended for Use within the High Luminosity Radiation Environments of the LHC.

Wednesday 24 September 2014 17:26 (1 minute)

Intended for implementation within the VFAT3 ASIC; the VFAT3-Comm-Port offers a single port for clock, synchronization, fast and slow control commands as well as data and slow control readout. The paper initially describes the core design which could be offered for use as an IP block in other projects. It also discusses an encoding technique which provides unique comma characters and increases robustness to errors associated with Single-Event-Effects (SEEs) and Single-Event-Upsets (SEUs) during transmission. The second part describes the specific implementation of the Comm-Port within the VFAT3 chip.

Summary

VFAT3-Comm-Port (V3CP) is a communication port, designed to provide a communication for readout front-end ASICs working in the demanding radiation environments posed by modern high energy physics experiments, in particular the Large Hadron Collider at CERN.

The V3CP was designed to be compatible with the GigaBit Transceiver (GBTX) chip in that it receives and transmits, clock and data over three differential pairs (E-links) running at 320Mbps.

The V3CP has four basic functions. The first is the reception of serial data over E-links and their parallelization. The second is generation and synchronization of the internal 40MHz clock. The third is execution of Fast Synchronous Control Commands (FSCCs). The last is serialization and transmission of data from a chip over E-links.

The V3CP generates internal 40MHz clock. Synchronization of the generated clock is crucial for each chip in the system. This is achieved through the recognition of a robust synchronization pattern. The synchronization pattern is 24-bit long and is composed of three consecutive unique comma characters provided by a 4-to-8bit encoding. Clock's synchronization can also be verified by sending an another unique comma character.

Communication with the V3CP is unsymmetrical. The input data have to be encoded using 4-to-8bit encoding scheme. The coding is based on the theory developed by R. Hamming, it provides Single Error Correction (SEC) and Double Error Detection (DED) capabilities (provided that the internally generated clock is properly synchronized). Such encoding does not only increase the robustness of input data to errors that can appear on the transmission lines but also increases their robustness against SEEs and SEUs after they are latched and processed inside a chip. The code has also a low-disparity. Due to the encoding, V3CP's effective input bandwidth is reduced to 160Mbps. In order for the output bandwidth not to be decreased, no encoding on the output data is performed.

In specific implementation for VFAT3, the input data are threated as FSCCs. There are 16 FSCCs, and each FSCC carries 4-bit information. VFAT3 uses 9 of them for purposes like assertion of the Level-One-Trigger or reset of chip's internal registers. Communication with a Slow Control is also embedded into FSCCs. Such a solution allows the user to send and receive Slow Control commands with the effective bandwidth of 40Mbps, which is significantly faster than the standard communication scheme through I2C.

For robustness against SEUs and SEEs, the V3CP logic was triplicated.

Primary author: DABROWSKI, Mieczyslaw Maria (Warsaw University of Technology (PL))

Co-authors: Dr DE LENTDECKER, Gilles (Universite Libre de Bruxelles); DE ROBERTIS, Giuseppe (Universita e INFN (IT)); KLOUKINAS, Kostas (CERN); KUPIAINEN, Marko Tapio (Lappeenranta Univ. of Technology (FI)); ASPELL, Paul (CERN); BONACINI, Sandro (CERN); TUUVA, Tuure (Lappeenranta Univ. of Technology (FI))

Presenter: DABROWSKI, Mieczyslaw Maria (Warsaw University of Technology (PL))

Session Classification: Second Poster Session

Track Classification: ASICs