# Development of a low power 5.12Gbps Data Serializer and Wireline Transmitter circuit for the VeloPix chip

Vladimir Gromov

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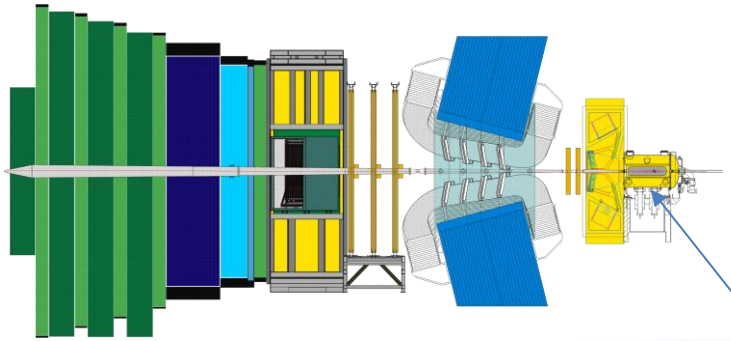
*TWEPP 2014, Aix-en-Provence, France.*

*September 25, 2014*

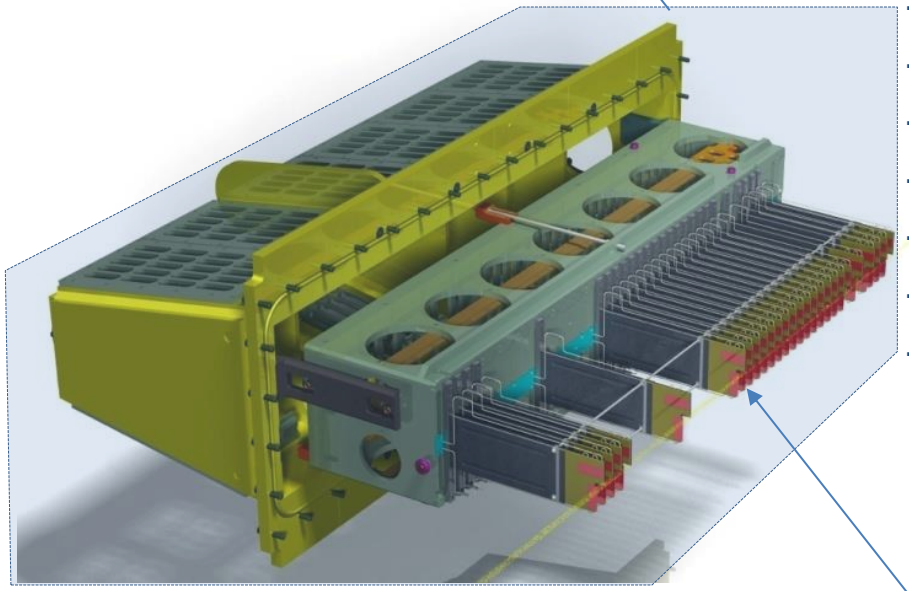
# Outline

- VeloPix pixel readout chip for VELO detector upgrade in LHCb experiment
- data serializer circuit : a shift-register-free topology
- the circuit design aspects and experimental results
- take-aways

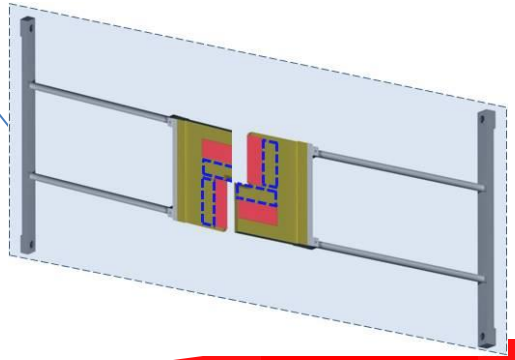
# Upgrade of VELO detector in LHCb



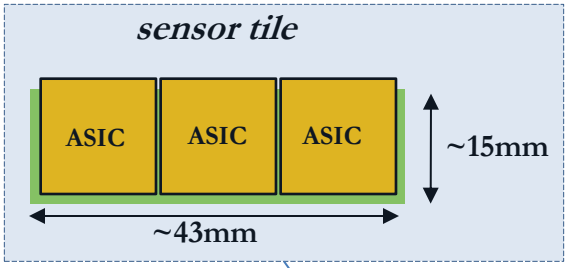
**LHCb upgrade:**
- long shutdown 2 (LS2) (2018)
- luminosity of 2 x $10^{33}cm^{-2}s^{-1}$ (5x present)

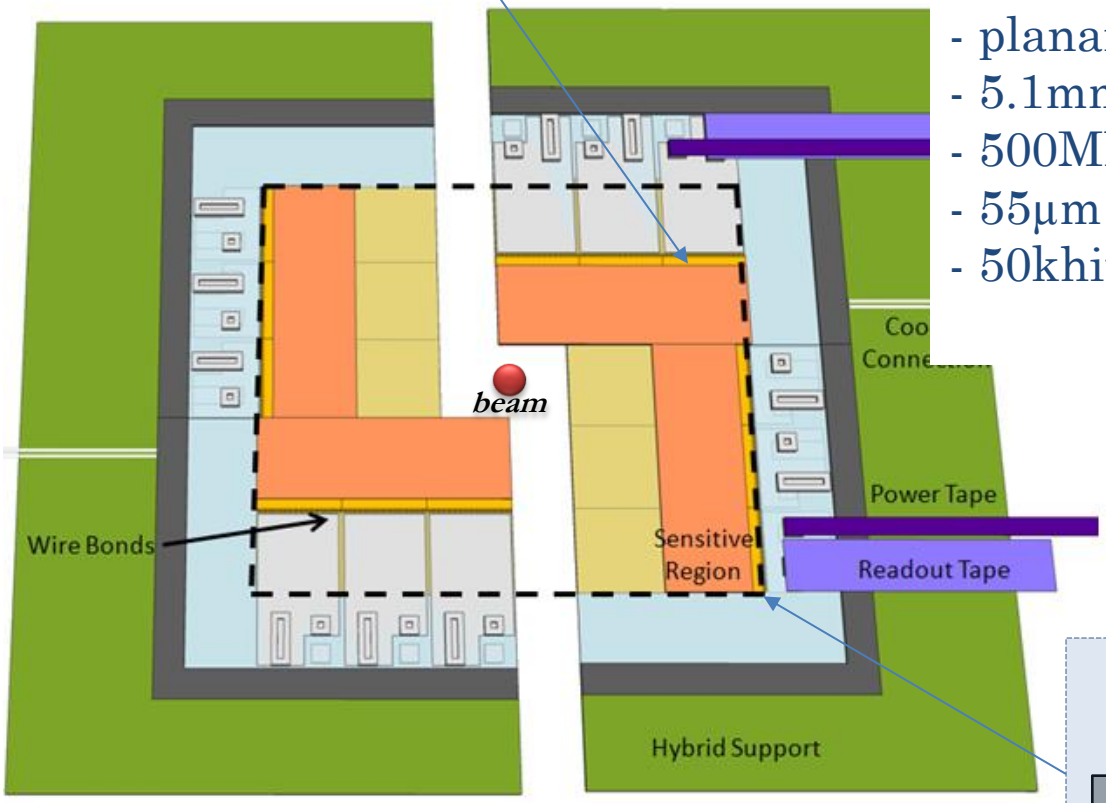


**VELO: hybrid pixel detector**
- trigger-less
- 26 stations (layers)
- total active area $1237cm^2$ (A3 size)
- vacuum compatible
- low material budget
- lowest possible power electronics
- radiation hard



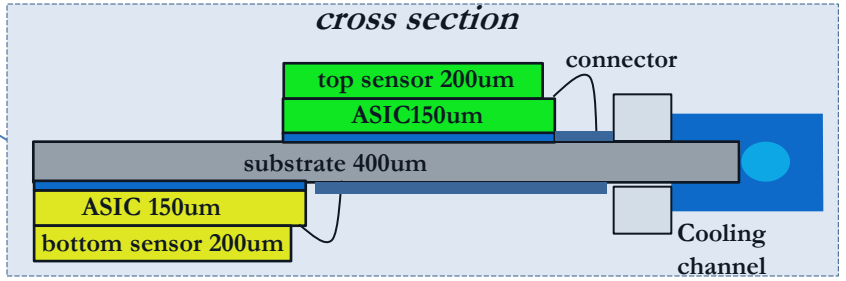
# VELO detector: station layout



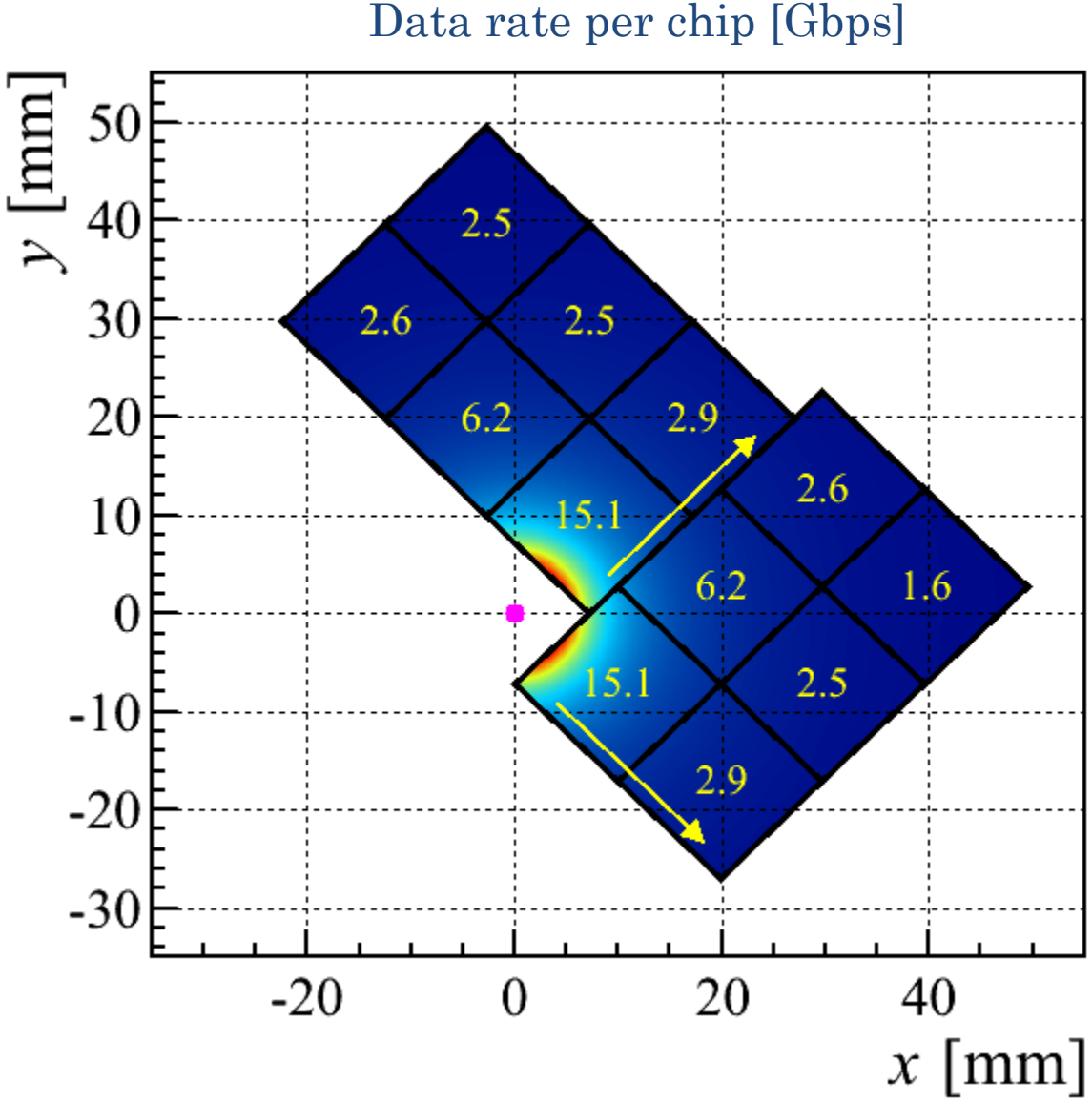




## specifications:

- 2 modules per station
- 1 tile = 1 sensor + 3 ASICs (VeloPix )
- 4 tiles on both sides of the module
- planar silicon sensor , electron collection
- 5.1mm from the beam to the sensor
- 500Mhits/sec/cm$^2$
- 55µm x 55µm pixel size
- 50khits/sec/pixel (~ HL-LHC in 2025)



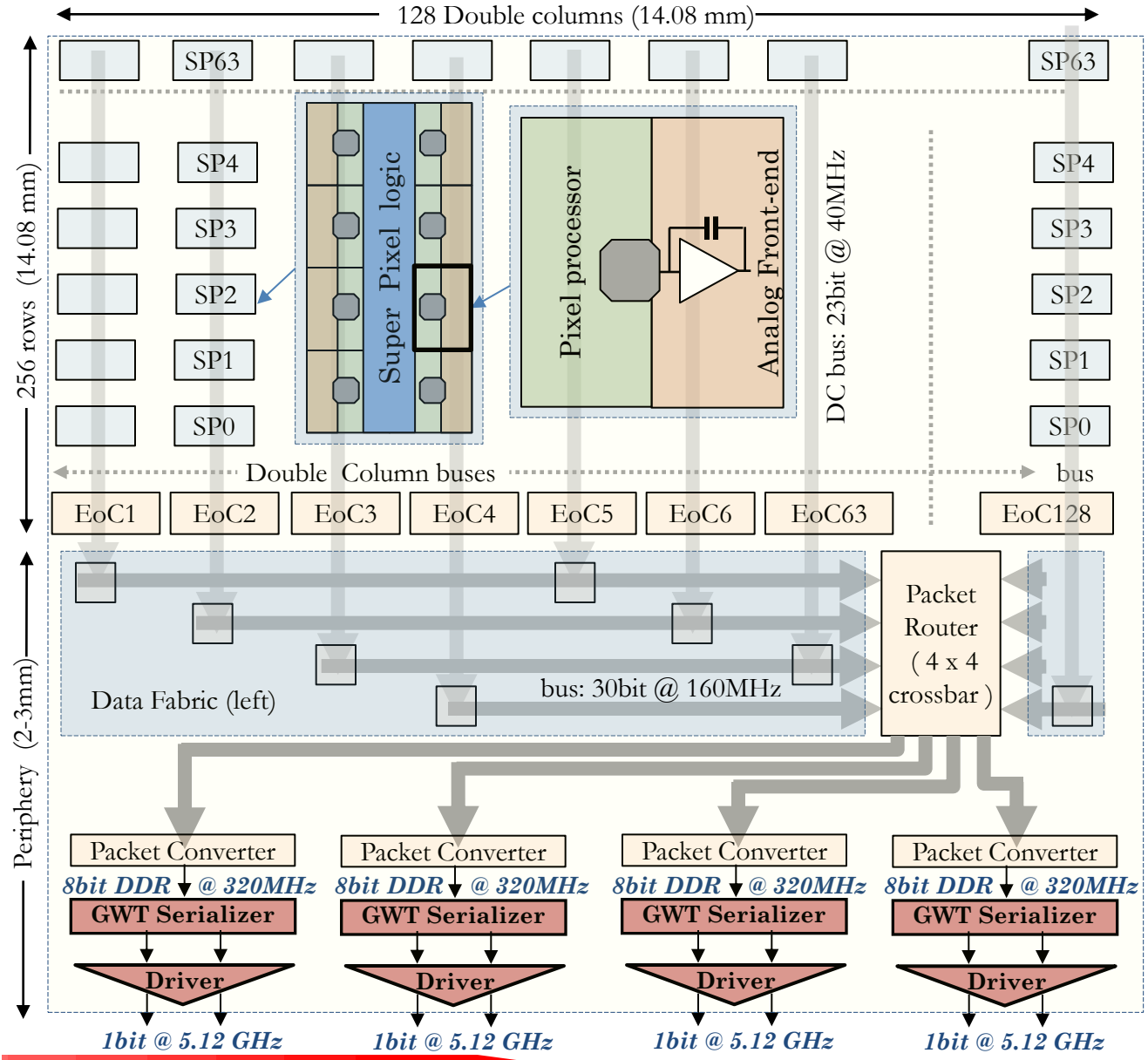
# Data rates and VeloPix




- successor of Timepix3
- pixel size: 55µm x 55µm
- pixels: 65 536 (256 x 256)
- area: 1.4cm x 1.4cm
- binary readout (no ToT)
- resolution/range: 25ns, 9b
- power: < 1.5W/cm$^2$
- up to 400Mrad, SEU tolerant
- technology: 130nm CMOS
- output data rate:
  >15Gbps (5x HL-LHC)

- VELO total : up to **2.9Tbps**
- highly non-uniform
  radiation pattern

# VeloPix readout chip




- analog FE
  pile-up losses < 1.6%

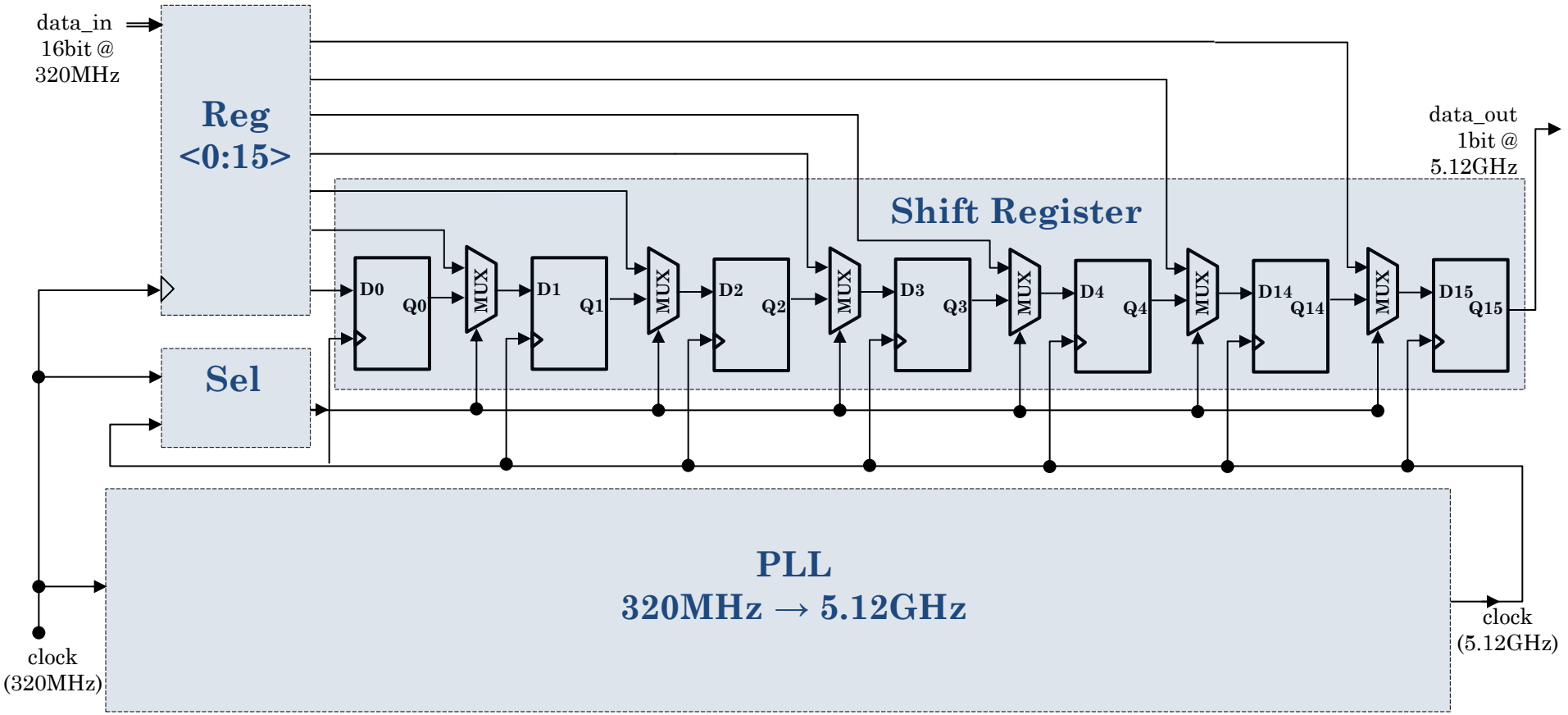
- pixels grouping for sharing BX ID & SP ID to reduce data rate (30%)

- fast and efficient readout architecture (losses < 1%,
  latency < BX ID range)

- data traffic equalization

- output electrical link:
  4 x 5.12Gbps

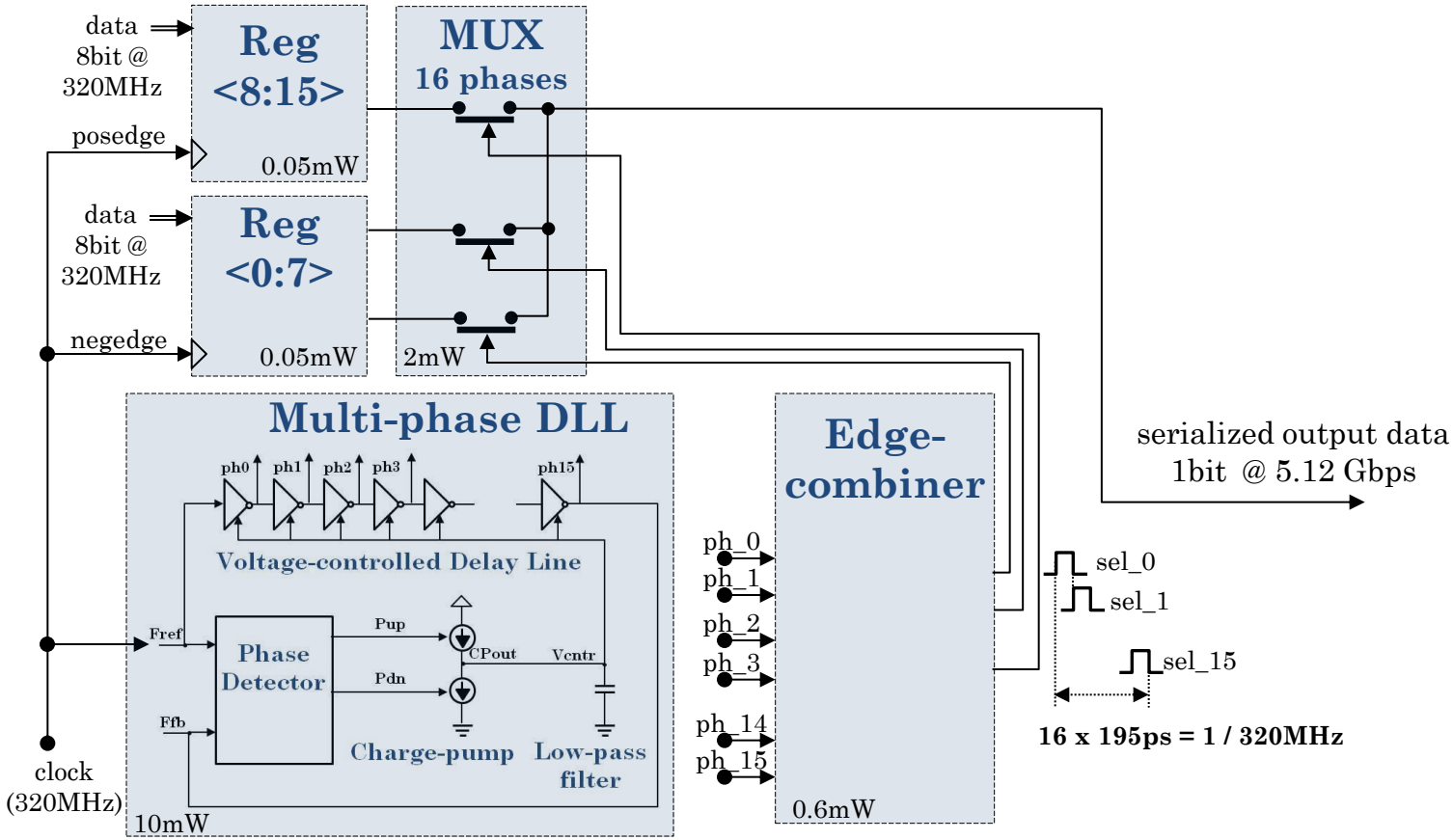
# Conventional Data Serializer (example GBTX)

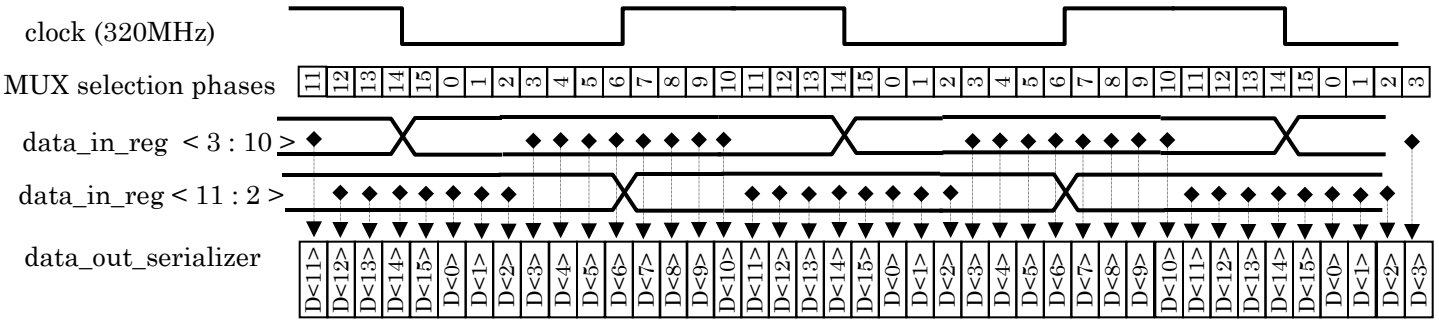



**significant power consumption due to:**

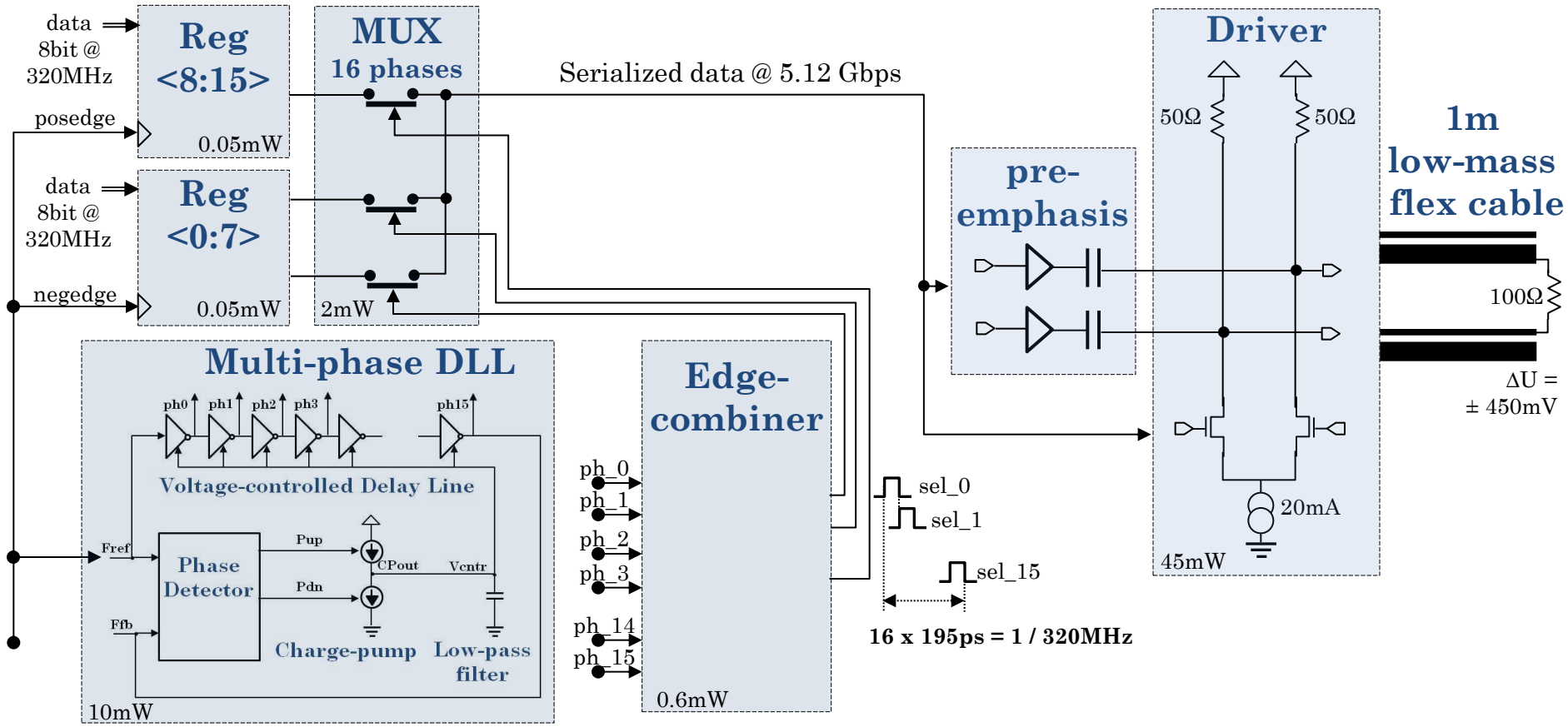
- a shift register driven by a high-frequency clock (5.12GHz)
- on-board PLL to generate the high-frequency clock

# GWT : a low power 5.12 Gbps byte-interleaved serializer / wireline transmitter



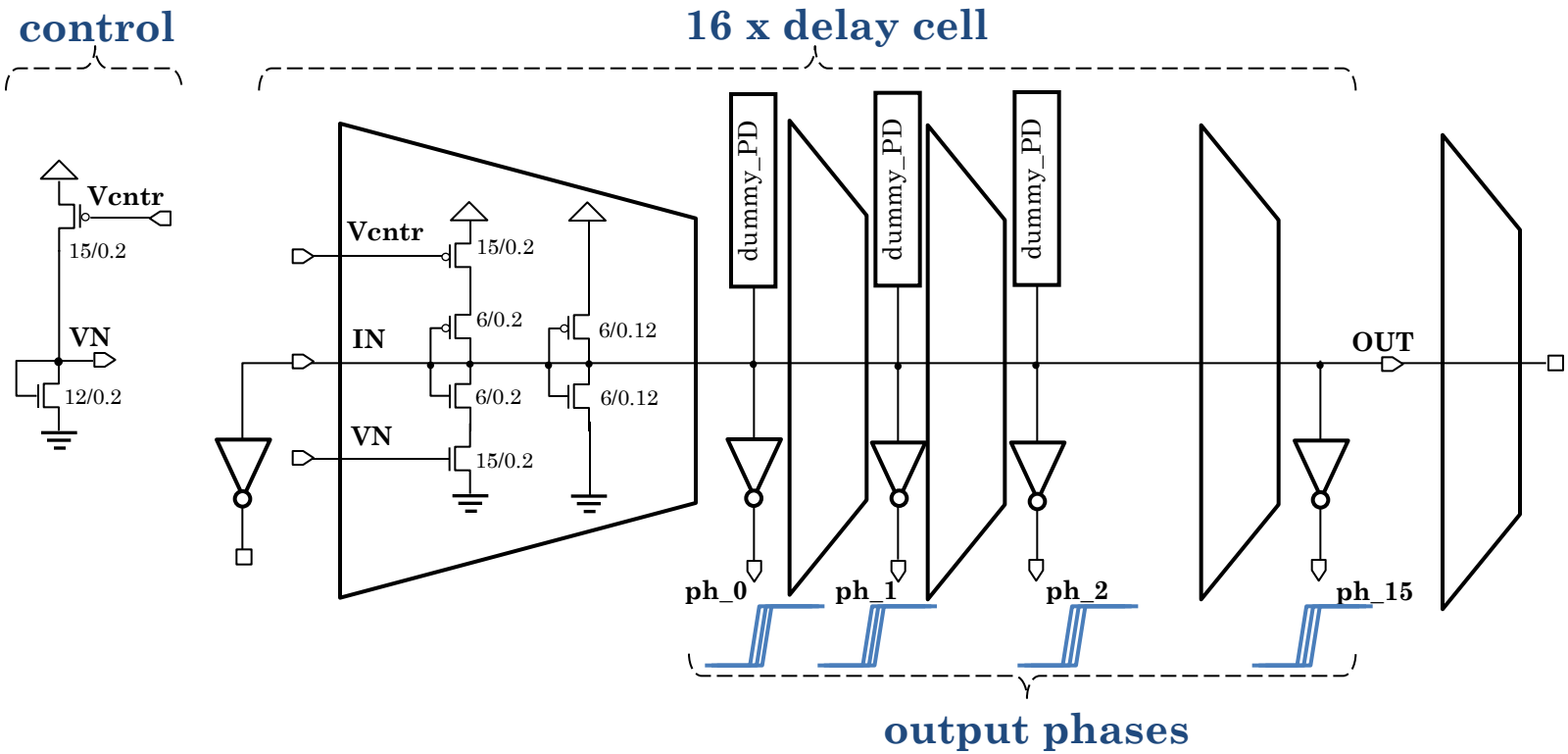



# GWT : a low power 5.12 Gbps byte-interleaved serializer / wireline transmitter



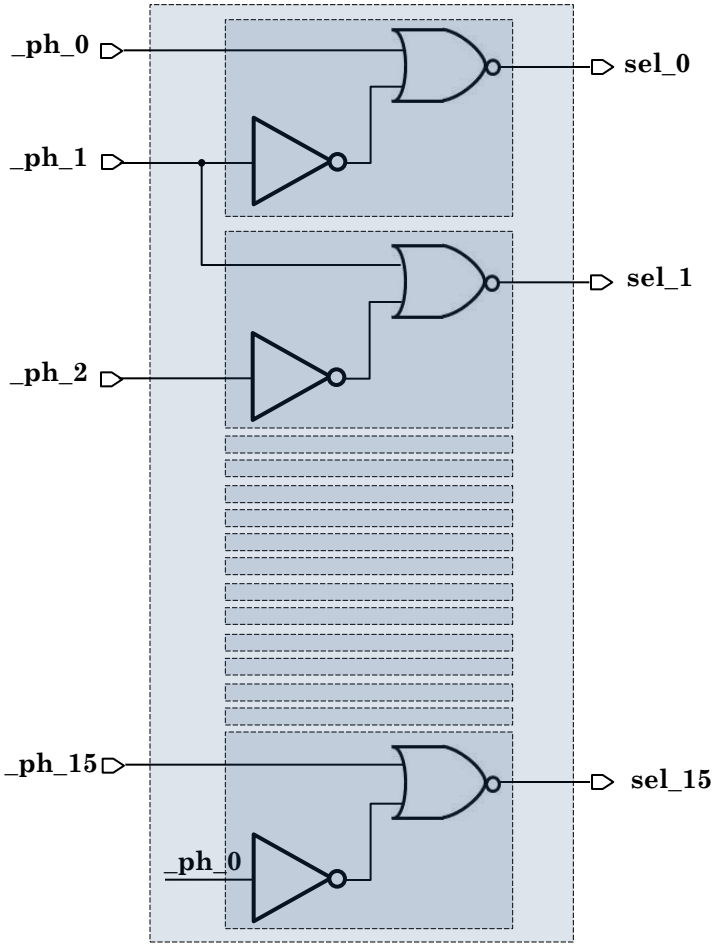

- **low-power topology** : serializer: 15mW , wireline transmitter: 45mW
- **delay-locked loop (DLL) – based topology** :
  - lower phase noise (no jitter accumulation)
  - lower power
  - harmonic (false) locking (solved by design)
  - sensitive to the noise of the reference clock

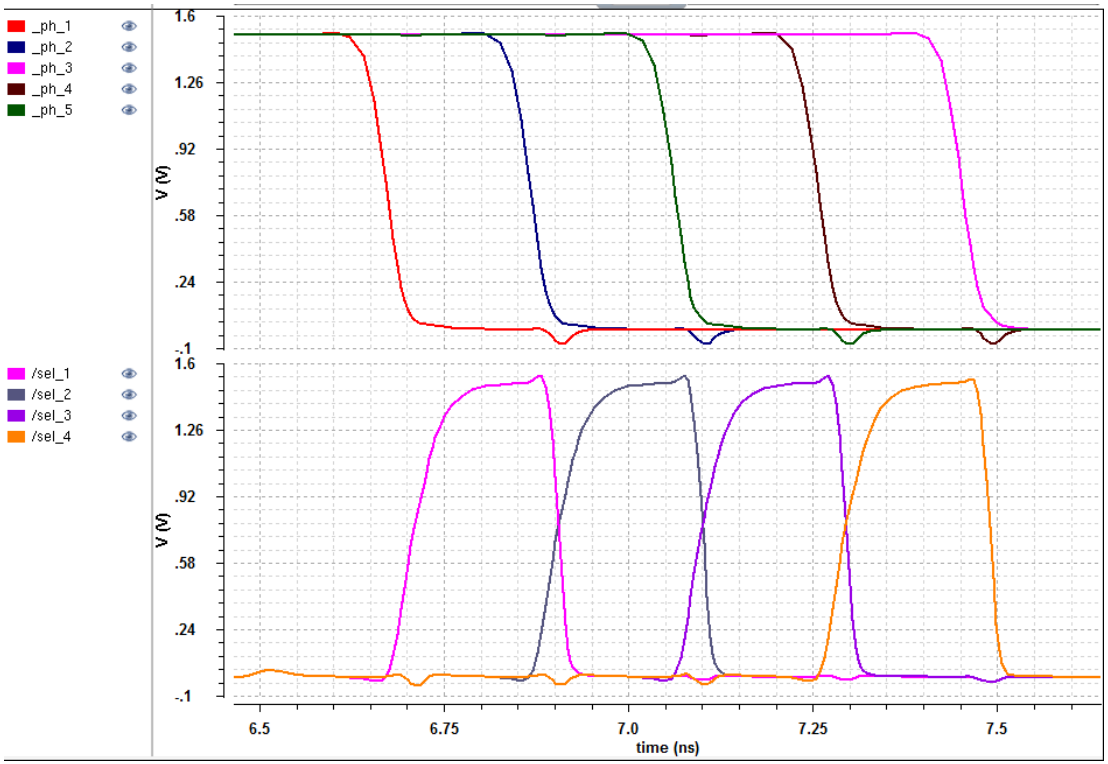
# Voltage-Controlled Delay Line (DLL)




- current-starved delay cells
- full CMOS signals on each output phase
- full clock period delay in the VCDL unlike that in the VCO
- duty cycle breakdown frequency: 160MHz (50% ref. freq.)
- internal time jitter : < 3ps RMS
- output phase mismatch : systematic 10ps p-p, stochastic 30ps p-p
  = 20% of the Unit Interval (UI=195ps)

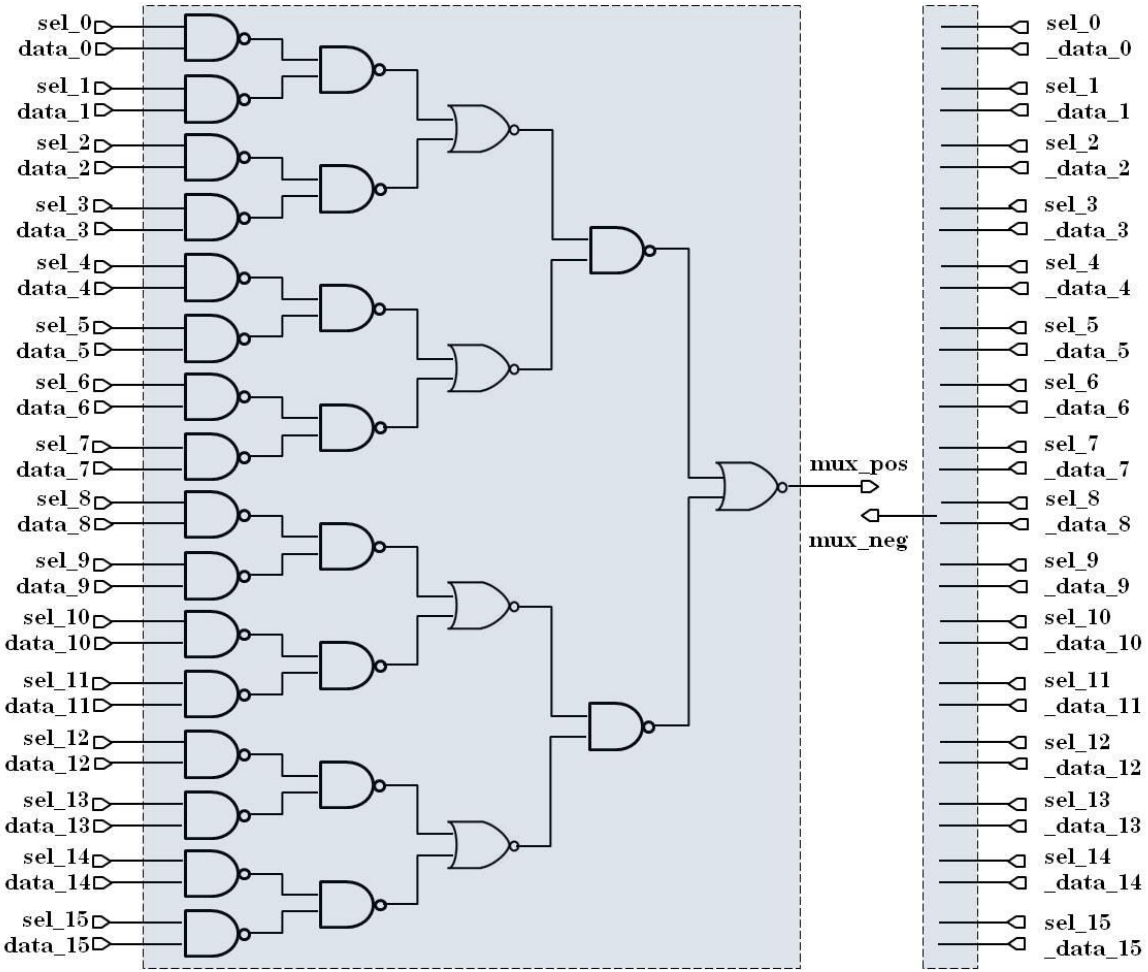
# Edge Combiner circuit

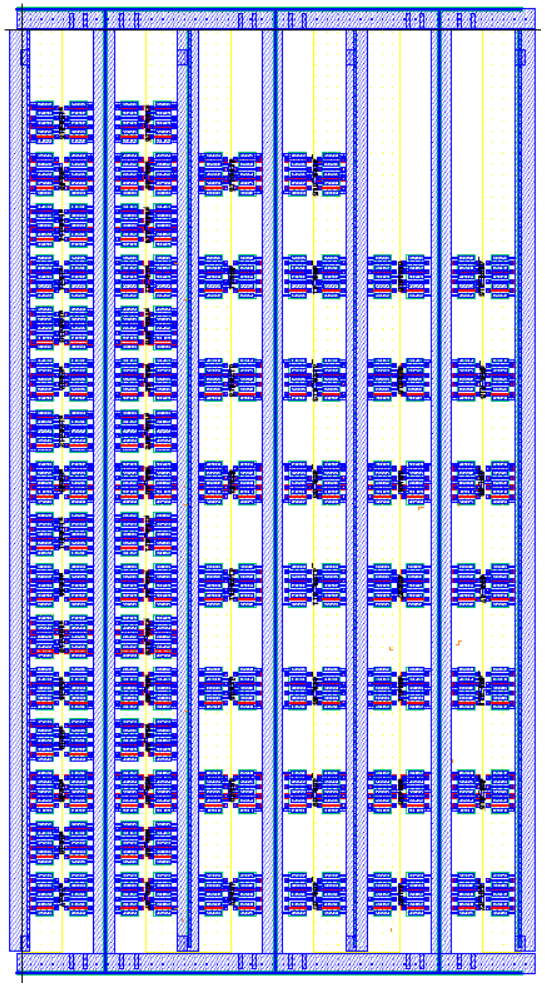



- custom-tailored gates (inv, nor) to get a proper output signals
- output signal mismatch : systematic 16ps p-p, stochastic 32ps p-p ≈ 20% UI

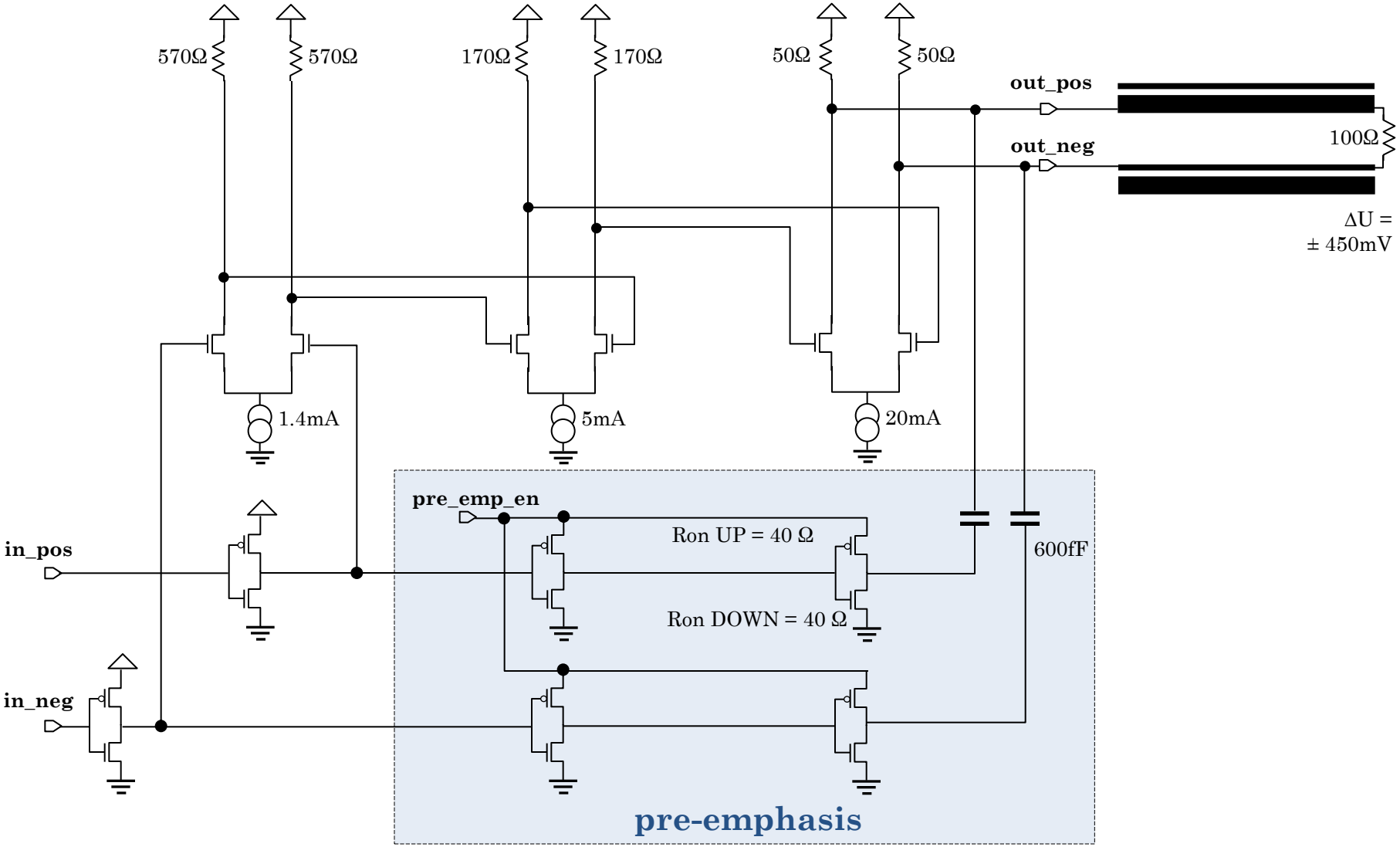
# 16-to-1 Differential Multiplexer



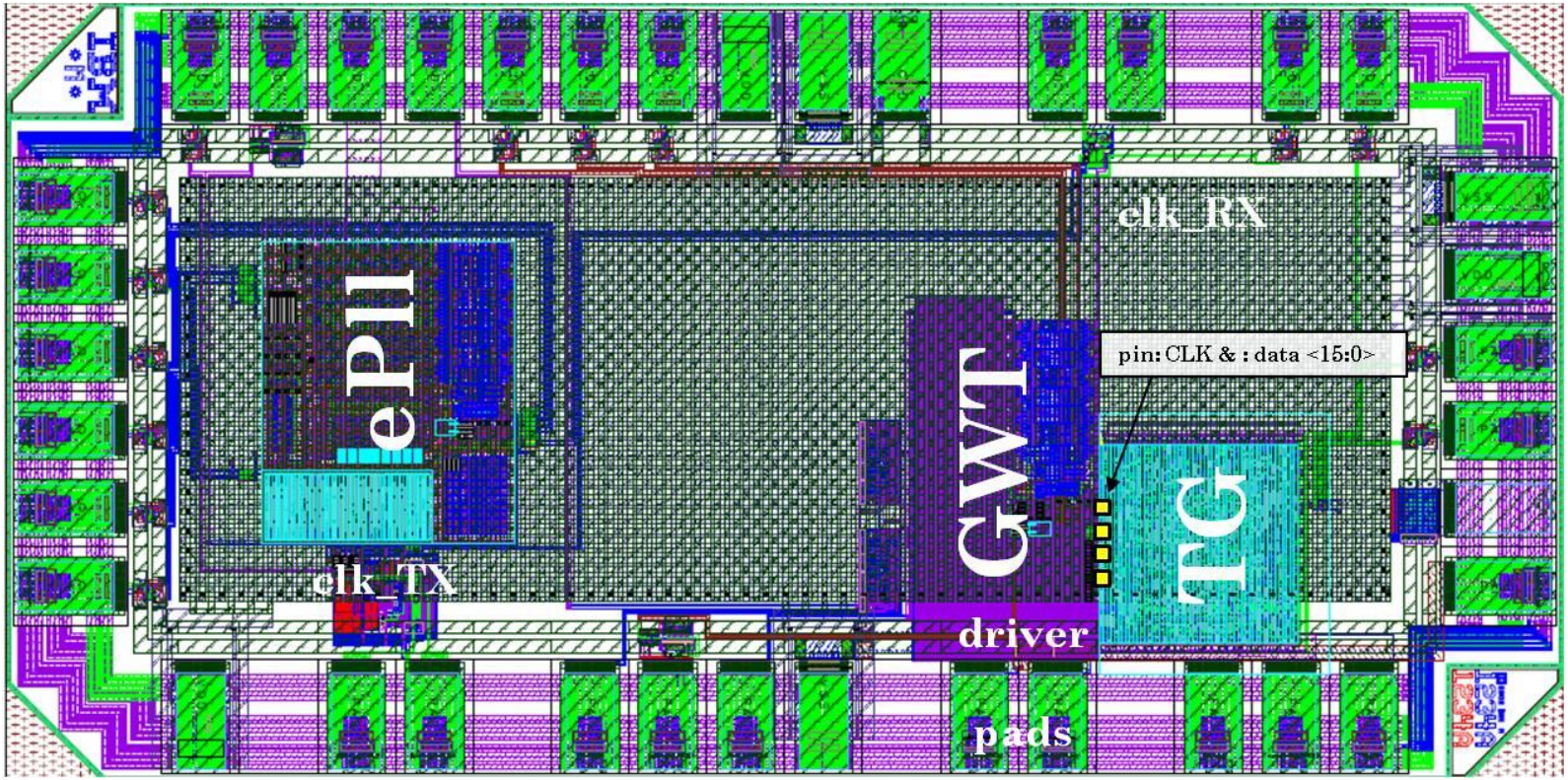
- negligible mismatch of the internal delay (130ps ± 7ps p-p)

# 5.12 Gbps Wireline Transmitter




- high-frequency boosting by a pair of feed-through capacitors (optional)

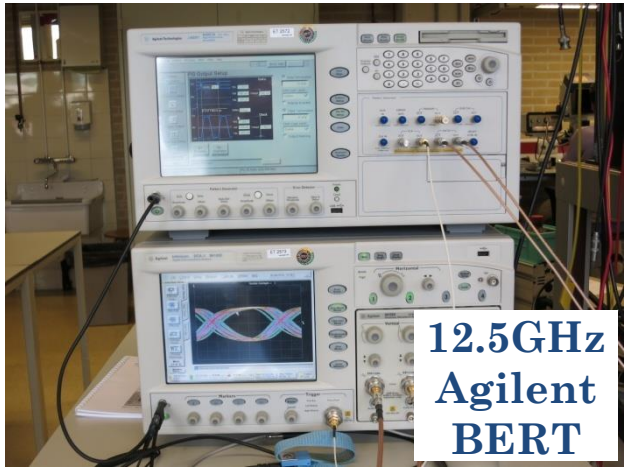
# Velo_GWT test chip

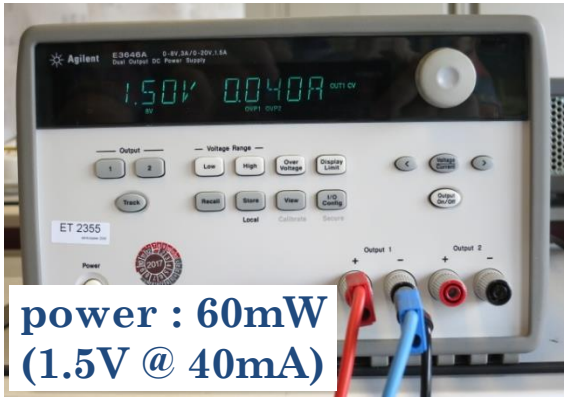


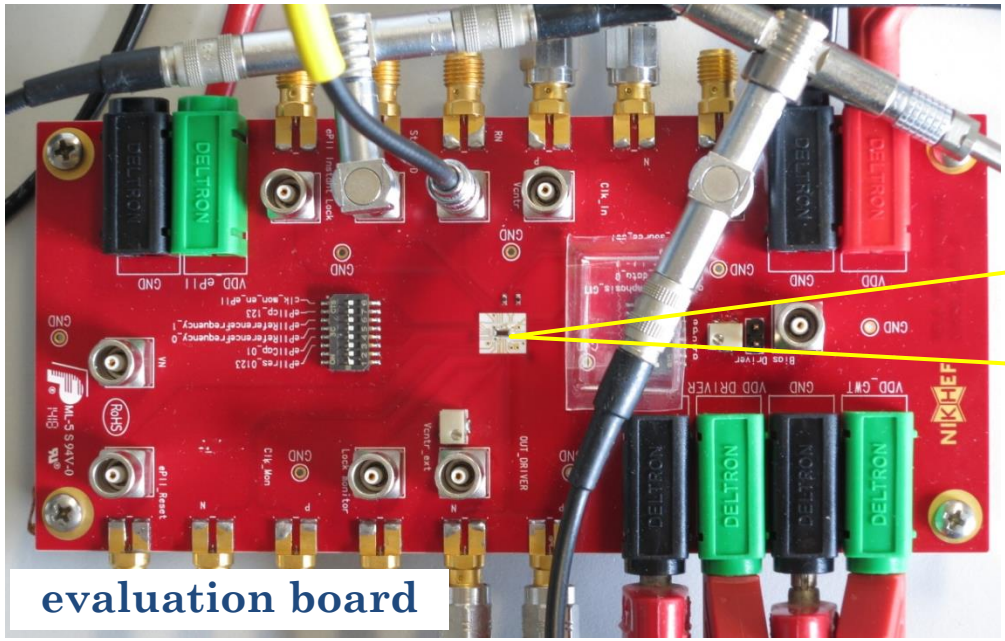

- 1mm x 2mm test chip in MOSIS MPW run (18/02/2014)
- 3-2-3 MA metal stack
- on-chip Test Data Generator (repetitive pattern / PRBS $2^{16}$),
- 320MHz reference clock : external / ePll [1] (on-chip)

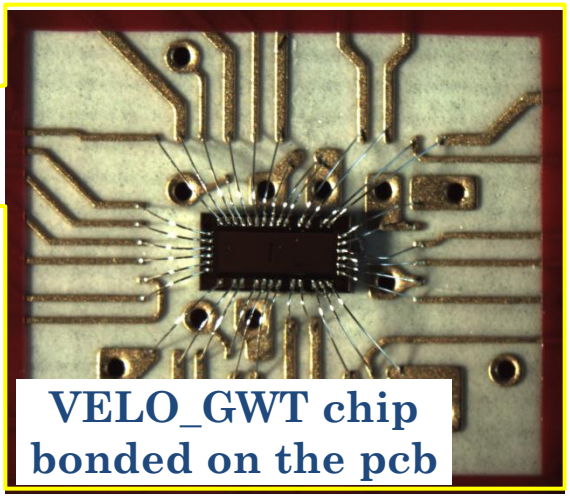
*[1] F. Tavernier "A Radiation-Hard PLL for Frequency Multiplication with Programmable Input Clock and Phase-Selectable Output Signals in 130nm CMOS", TWEPP2012, Oxford, UK*

# Velo_GWT evaluation set-up



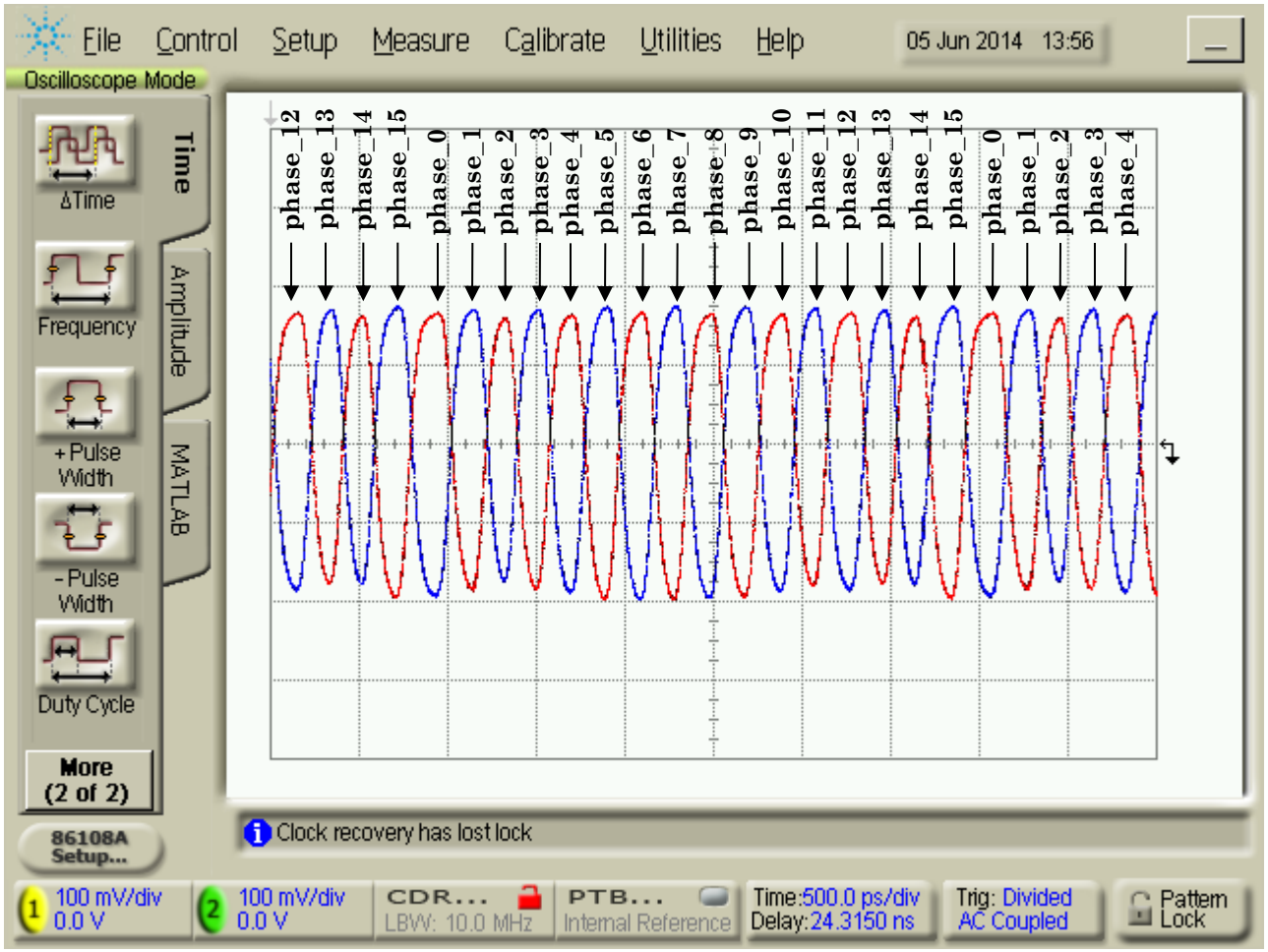



# Phase mismatch measurements

0101010101 data pattern

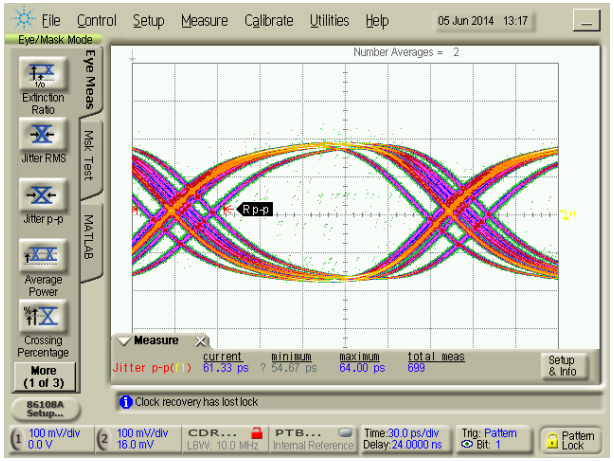
both outputs @ 5.12Gbps, 100mv/div, 500ps/div, clock external 320MHz



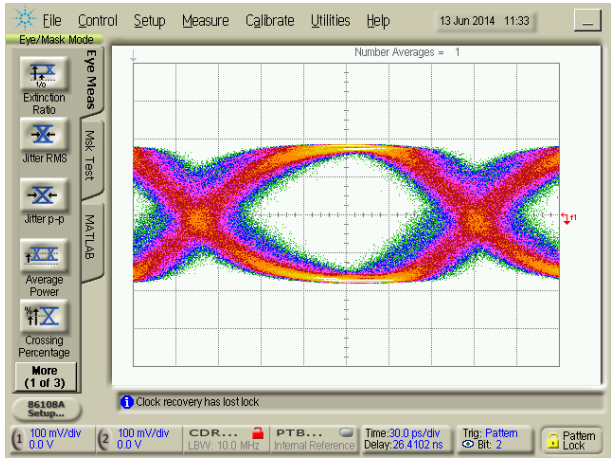

- phase width mismatch : ~ 50ps p-p (25% UI)

# Eye diagram measurements

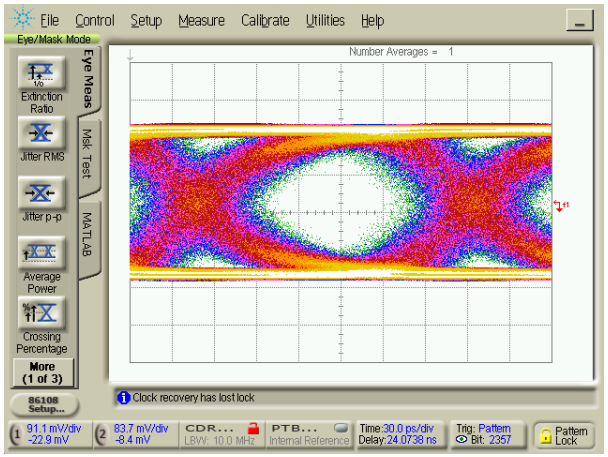
**external** (clean)
ref. clock (320MHz)
**0101010101 pattern**




**ePll** generated (noisy)
ref. clock (320MHz)
**0101010101 pattern**

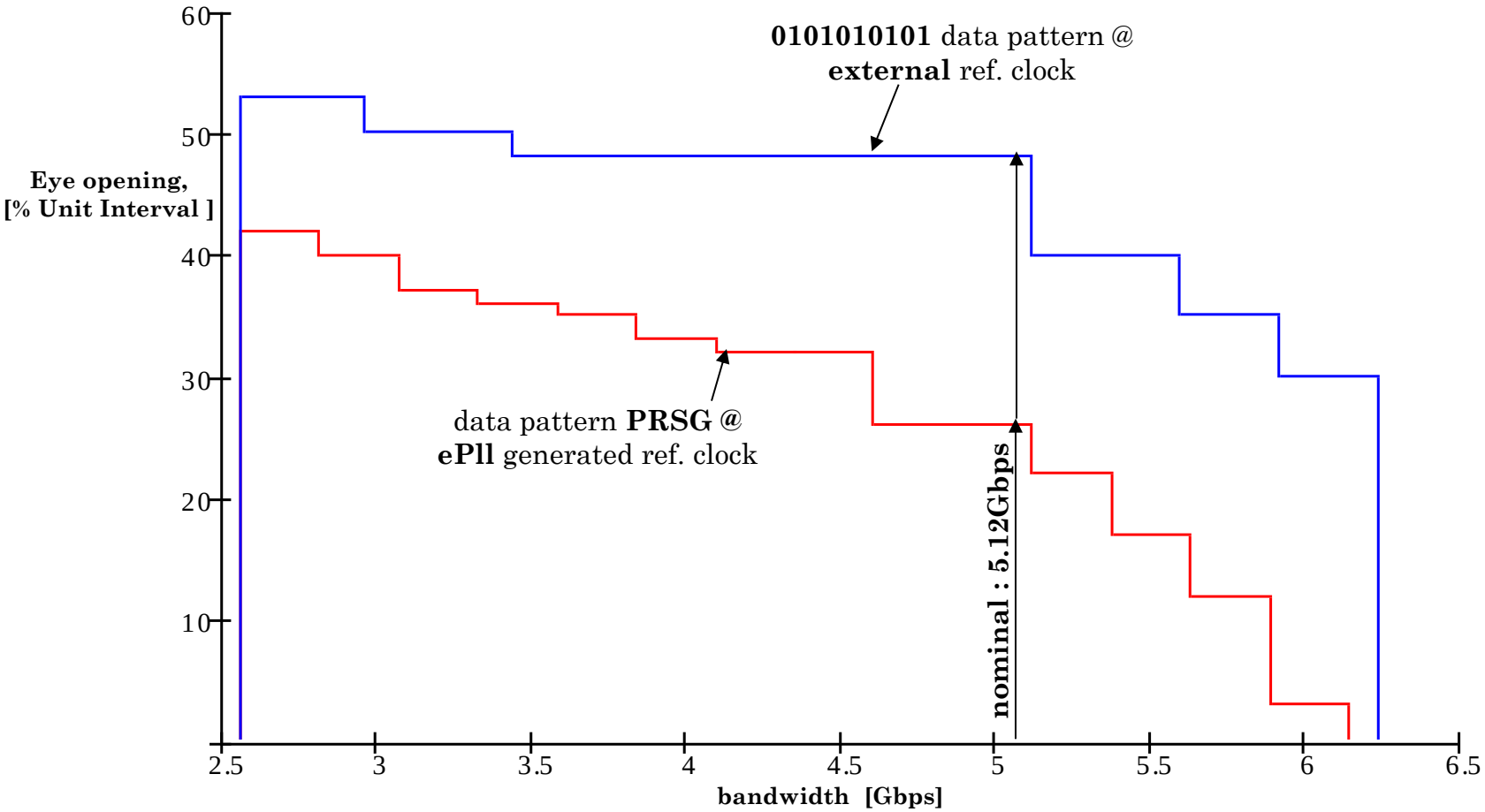



**ePll** generated (noisy)
ref. clock (320MHz)
**PRBS pattern**




- eye diagram opening : ~ 60ps @ ± 200mV (30% UI)
- GWT internal phase noise is low
- severe impact of the jitter on the ref. clock (ePll-generated)

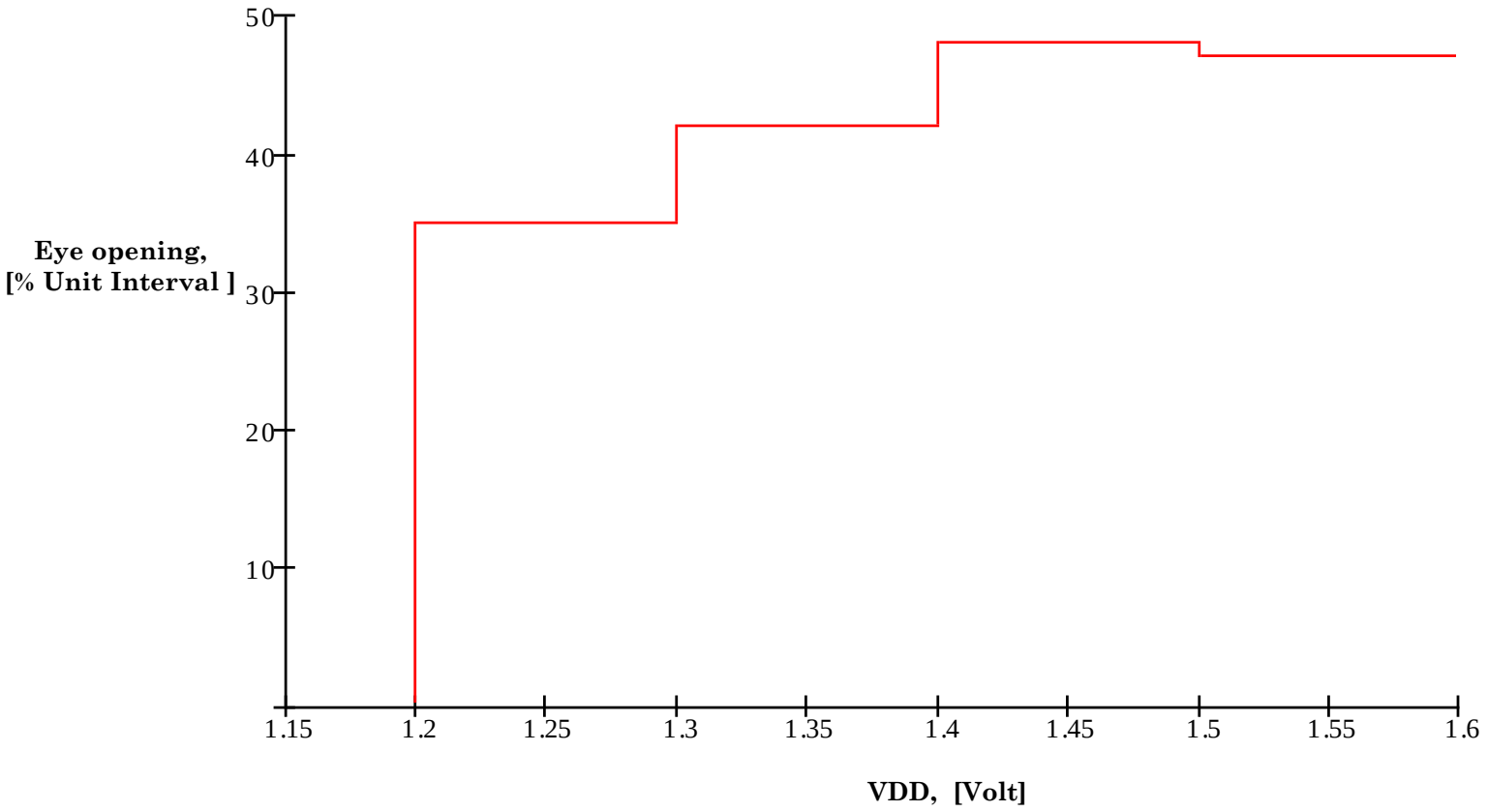
# Operation bandwidth limits




- GWT can operate in range from 2.56Gbps to 6.24Gbps corresponding to the reference clock range 160MHz to 390MHz

# Operation power supply voltage limits

0101010101 data pattern, eye diagram opening ± 200mV




- VDD must not be lower than 1.2V

# Take-aways

- **GWT is a 5.12Gbps Data Serializer and Wireline Driver circuit being developed for VeloPix chip**

- **a shift-register-free topology has been chosen for the serializer to provide low power consumption (15mW) and avoid a high-speed PLL**

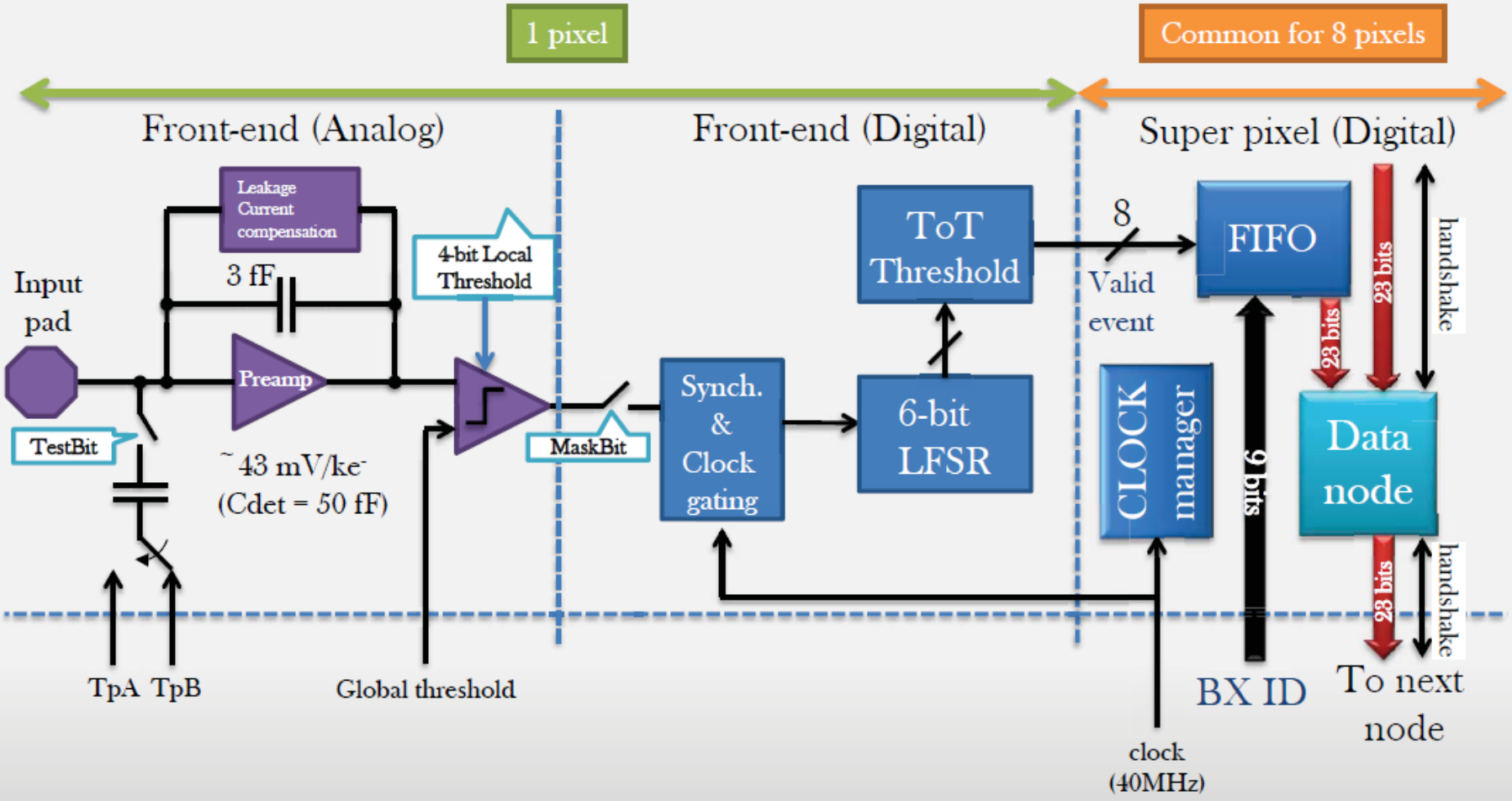
- **four GWT units on each VeloPix will transmit a large amount of data (> 15Gbps) over a 1 meter low-mass copper cable contributing only 10% to the chip power budget ( 240mW = 4 x {15mW + 45mW})**

- **measurements of the prototypes submitted in 130nm technology demonstrate expected results**

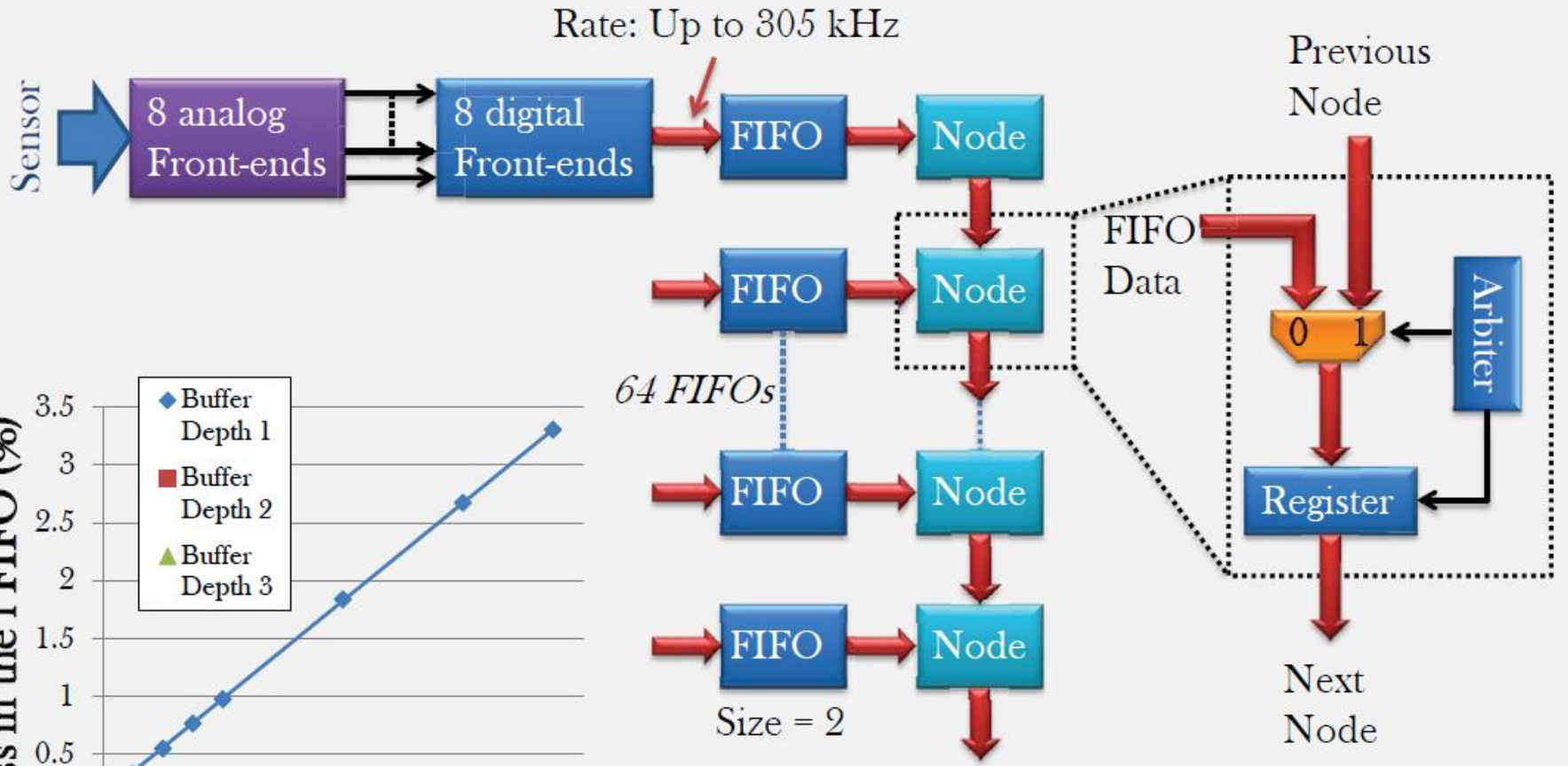
- **the circuit will be re-designed in TSMC 130nm technology**

# Spare slides

# VeloPix Pixel Schematic 3/3

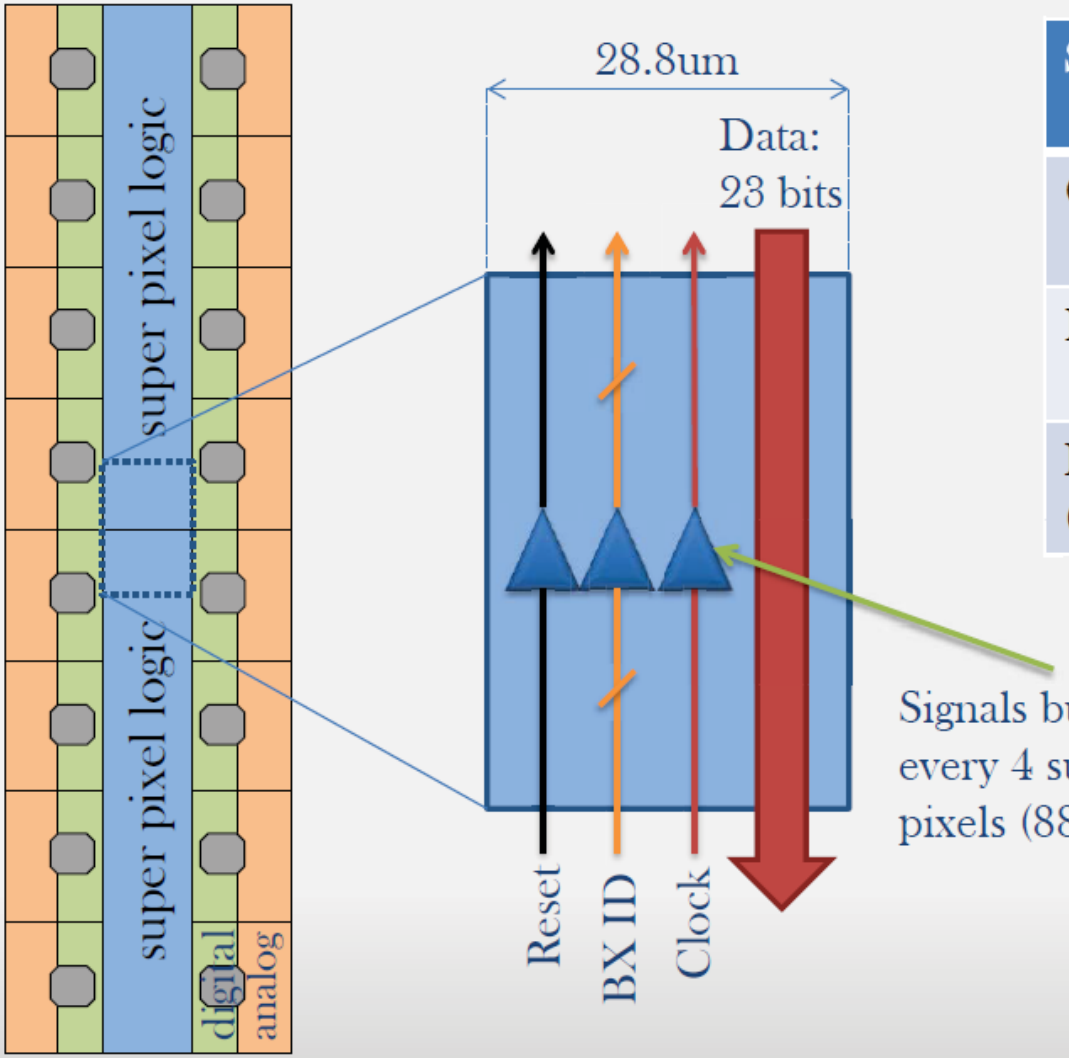


# Double column architecture




See [5] for more details.

# Double column floorplan



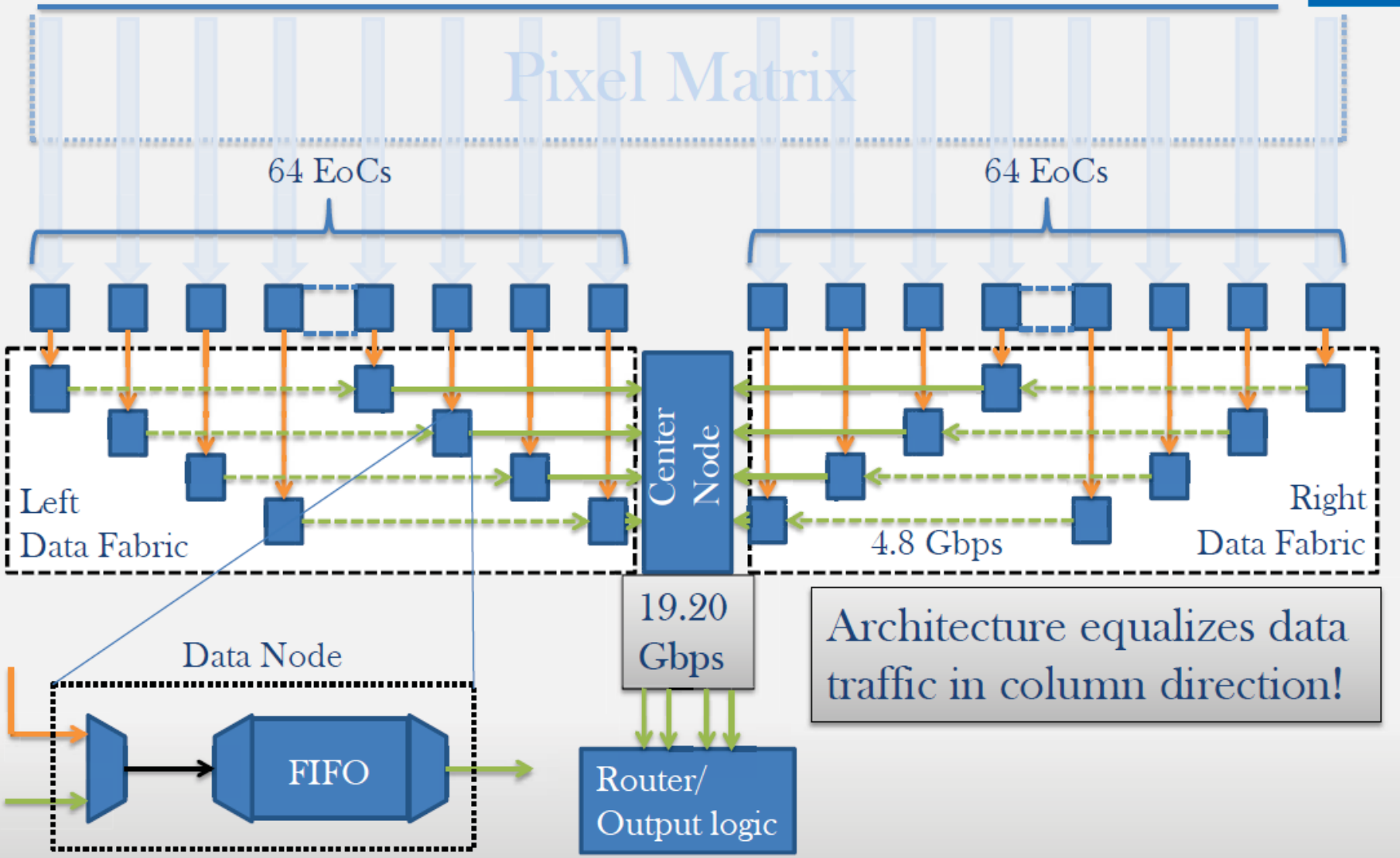

| Signal | Skew (ps) * | Power (mw) * |
|---|---|---|
| Clock | 1670 / 1870 | 0.476 |
| Reset | 7130 / 8540 | N/A |
| BX ID (9 bits) | 8110 / 9950 | 0.273 |

x 128

**< 100mW / chip**

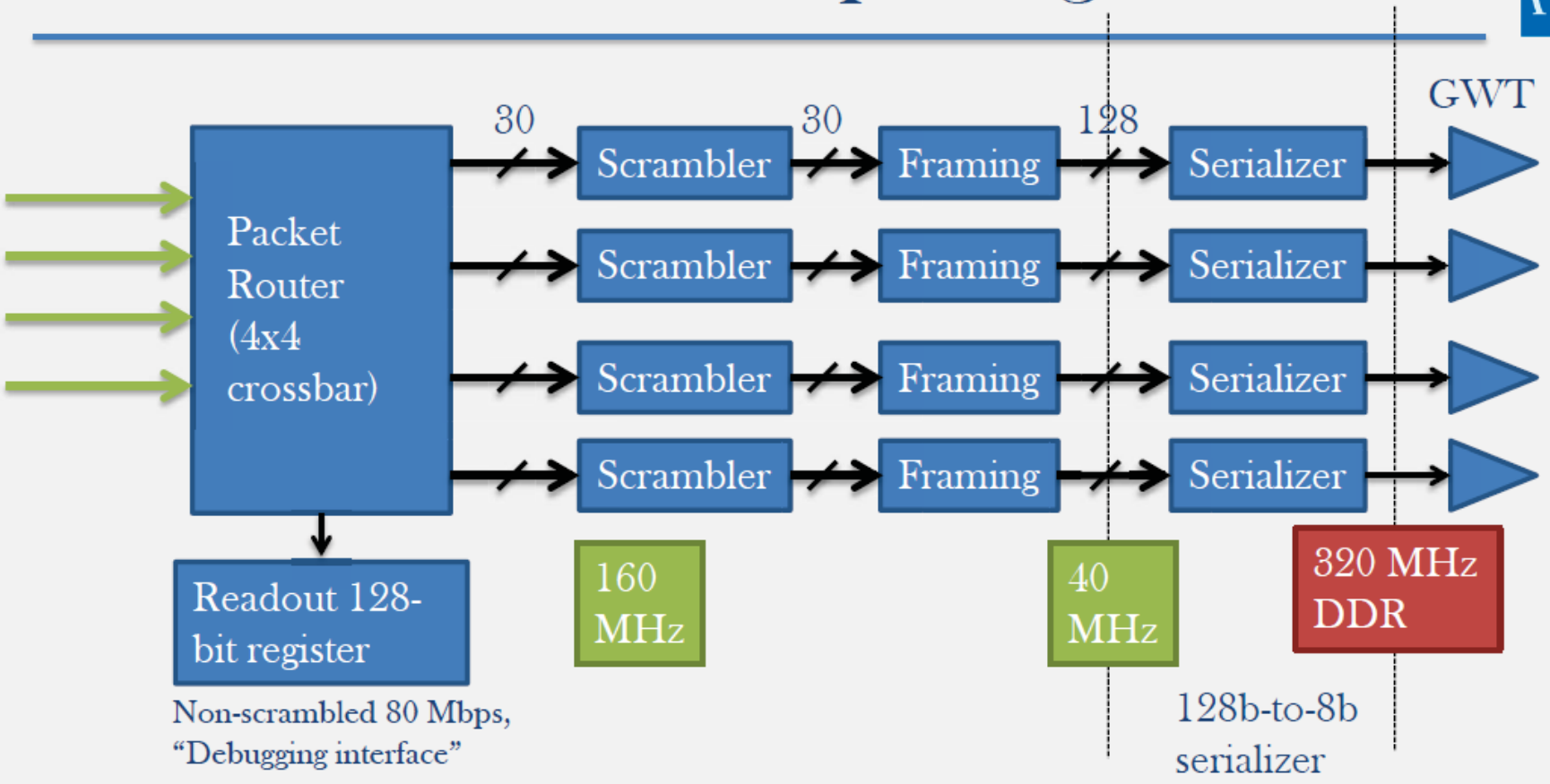
* slow corner SS/1.4V/125C
* fast corner FF/1.6V/-55C

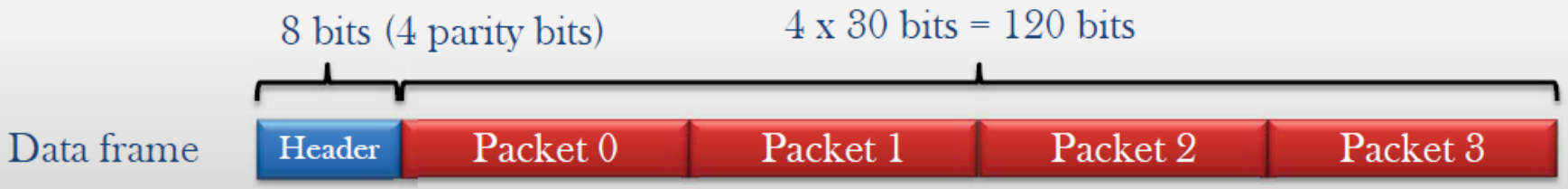
# End-of-Column (EoC) data fabric




Architecture equalizes data traffic in column direction!

# Router/Output logic

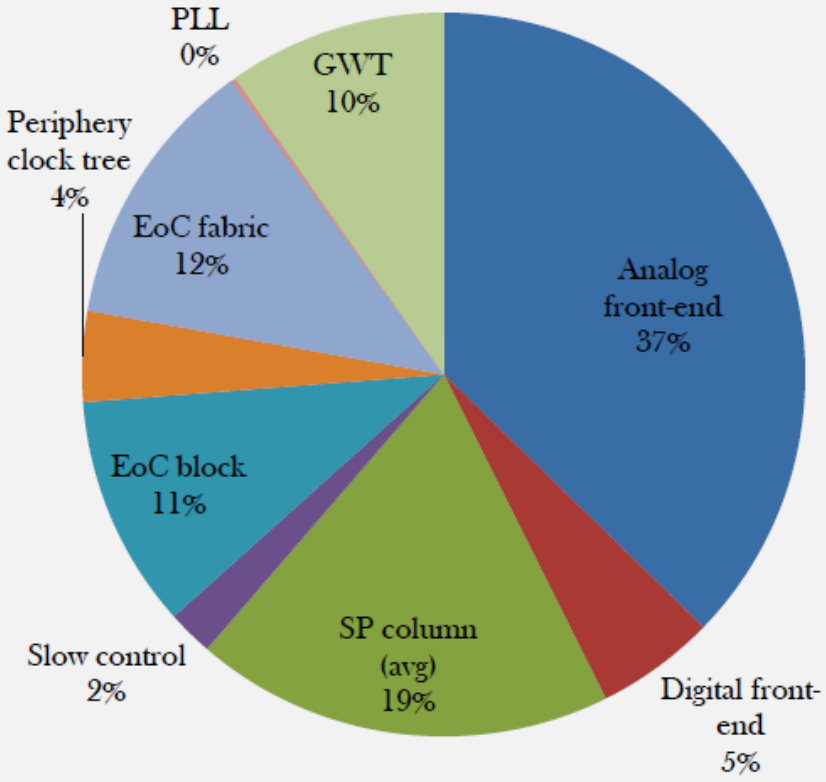


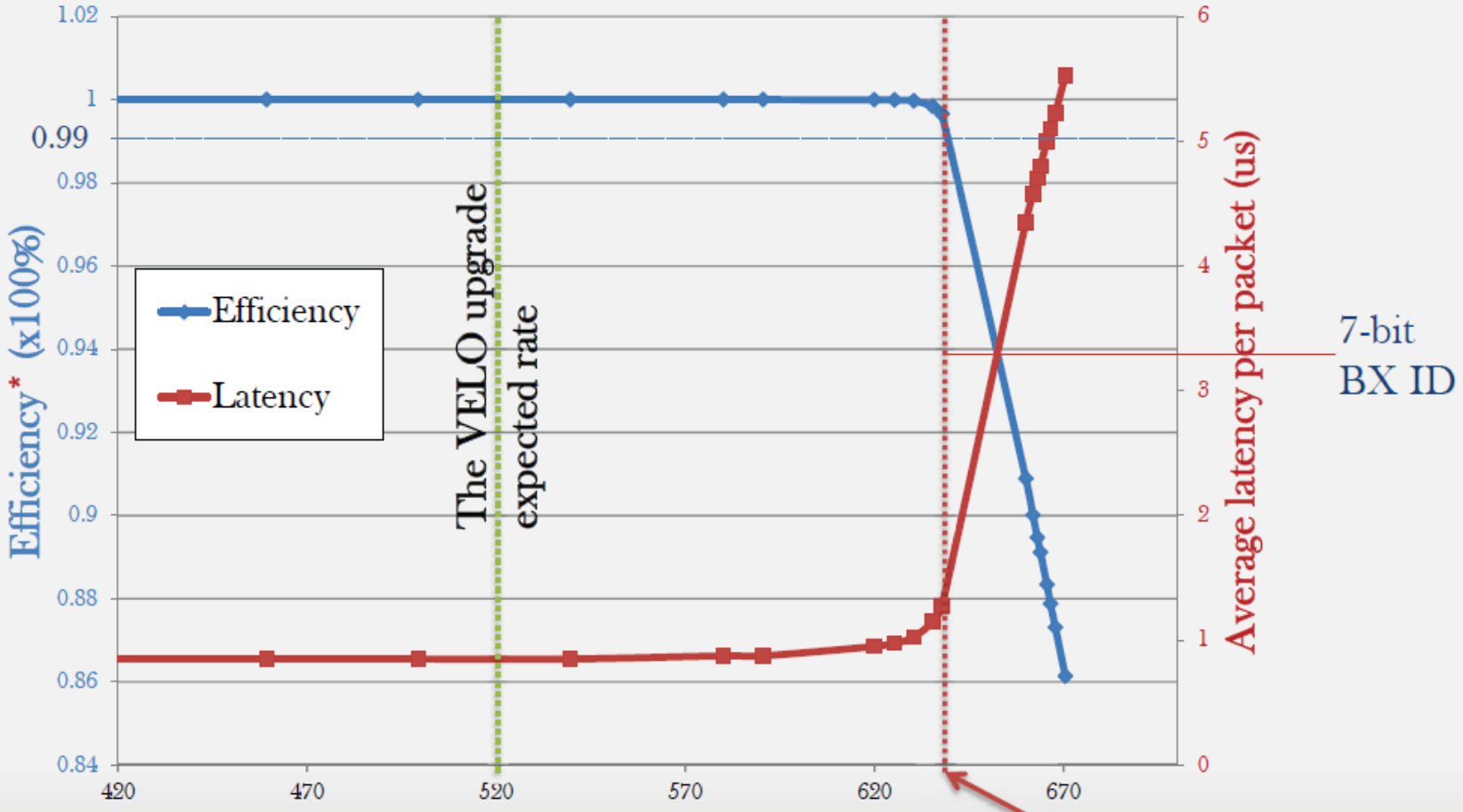
# Summary: Power

| Block | P (mw) | #Blocks | Total power |
|---|---|---|---|
| Analog front-end | 0.014 | 65536 | 917.5 |
| Digital front-end | 0.002 | 65536 | 131.1 |
| SP column (avg) | 3.6 | 128 | 460.8 |
| *Slow control* | *50* | *1* | *50** |
| *EoC block* | *2* | *128* | *256** |
| *Periphery clock tree* | *100* | *1* | *100** |
| *EoC fabric* | *300* | *1* | *300** |
| *PLL* | *5.5* | *1* | *5.5** |
| GWT | 60 | 4 | 240 |
| | | **Total (mW):** | 2460.9 |
| | | **W/cm^2** | 1.09 |

* estimated/budgeted



# Simulation: Data transfer efficiency




*no front-end pile-up taken into account